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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303cct6tr

3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.12 Interrupts and events

3.12.1 Nested vectored interrupt controller (NVIC)

The STM32F303xB/STM32F303xC devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.16 Fast comparators (COMP)

The STM32F303xB/STM32F303xC devices embed seven fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 28: Embedded internal reference voltage on page 62* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined per pair into a window comparator

3.17 Timers and watchdogs

The STM32F303xB/STM32F303xC includes two advanced control timers, up to six general-purpose timers, two basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
Advanced	TIM1, TIM8	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Note: TIM1/8 can have PLL as clock source, and therefore can be clocked at 144 MHz.

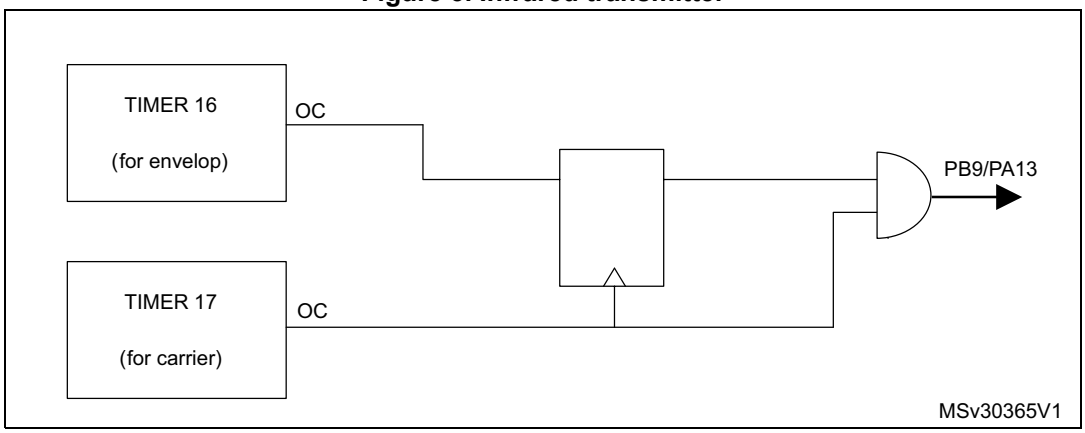
3.25 Infrared Transmitter

The STM32F303xB/STM32F303xC devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.26 Touch sensing controller (TSC)

The STM32F303xB/STM32F303xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

3.27 Development support

3.27.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.27.2 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F303xB/STM32F303xC through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F303xB/STM32F303xC pin definitions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
D6	1	-	-	PE2	I/O	FT	(1)	TRACECK, TIM3_CH1, TSC_G7_IO1, EVENTOUT	-
D7	2	-	-	PE3	I/O	FT	(1)	TRACED0, TIM3_CH2, TSC_G7_IO2, EVENTOUT	-
C8	3	-	-	PE4	I/O	FT	(1)	TRACED1, TIM3_CH3, TSC_G7_IO3, EVENTOUT	-
B9	4	-	-	PE5	I/O	FT	(1)	TRACED2, TIM3_CH4, TSC_G7_IO4, EVENTOUT	-
E7	5	-	-	PE6	I/O	FT	(1)	TRACED3, EVENTOUT	WKUP3, RTC_TAMP3
D8	6	1	1	V_{BAT}	S	-	-	Backup power supply	

Table 14. Alternate functions for port A (continued)

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA12	-	TIM16_CH1	-	-	-	-	TIM1_CH2N	USART1_RTS_DE	COMP2_OUT	CAN_TX	TIM4_CH2	TIM1_ETR	-	USB_DP	EVENTOUT
PA13	SWDIO-JTMS	TIM16_CH1N	-	TSC_G4_IO3	-	IR_OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	-	EVENTOUT
PA14	SWCLK-JTCK	-	-	TSC_G4_IO4	I2C1_SDA	TIM8_CH2	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	TIM8_CH1	-	I2C1_SCL	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_RX	-	TIM1_BKIN	-	-	-	-	EVENTOUT

Table 27. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 32. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	20.05	20.33	20.42	20.50	20.67	20.80	44.2(2)	350	735(2)	µA
		Regulator in low-power mode, all oscillators OFF	7.63	7.77	7.90	8.07	8.17	8.33	30.6(2)	335	720(2)	
	Supply current in Standby mode	LSI ON and IWDG ON	0.80	0.96	1.09	1.23	1.37	1.51	-	-	-	
		LSI OFF and IWDG OFF	0.60	0.74	0.83	0.93	1.02	1.11	5.0(2)	7.8	13.3(2)	

1. Guaranteed by characterization results unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 33. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	µA
			Regulator in low-power mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	
	Supply current in Standby mode		LSI ON and IWDG ON	2.22	2.42	2.59	2.78	3.0	3.24	-	-	-	
			LSI OFF and IWDG OFF	1.69	1.82	1.94	2.08	2.23	2.40	3.5	5.4	9.2	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.44	1.52	1.60	1.71	1.84	1.98	-	-	-	
			LSI OFF and IWDG OFF	0.93	0.95	0.98	1.02	1.08	1.15	-	-	-	

1. Guaranteed by characterization results.

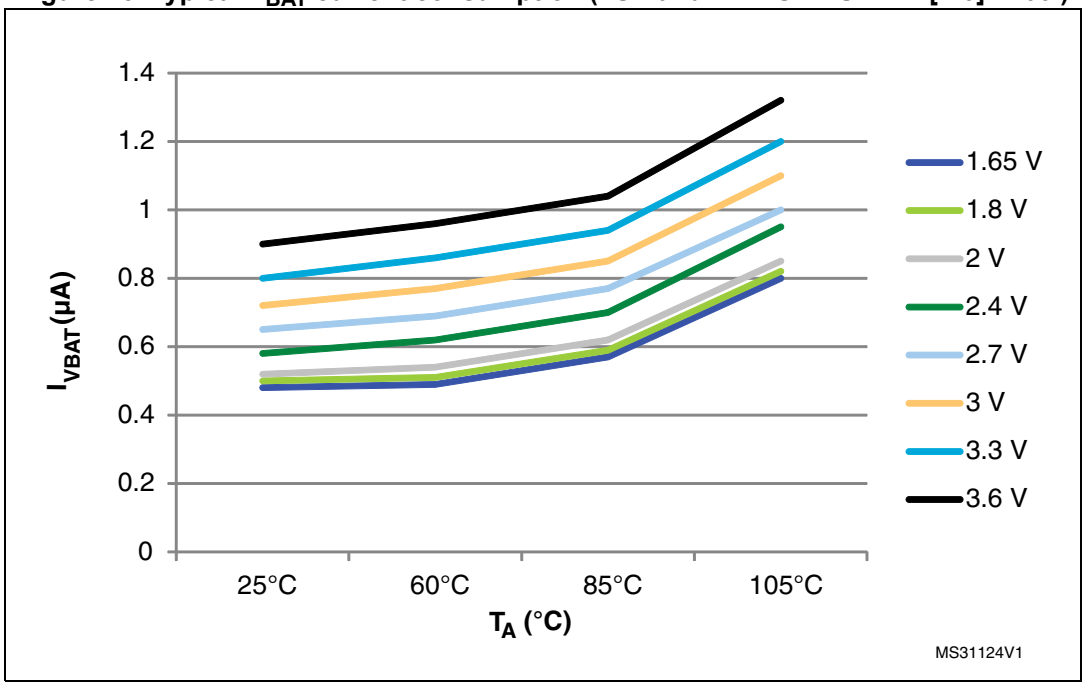
The total consumption is the sum of IDD and IDDA.

Table 34. Typical and maximum current consumption from V_{BAT} supply

Symbol	Para meter	Conditions (1)	Typ @V_{BAT}								Max @V_{BAT} = 3.6 V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 13. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15*

Table 41. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design.

Figure 15. Low-speed external clock source AC timing diagram

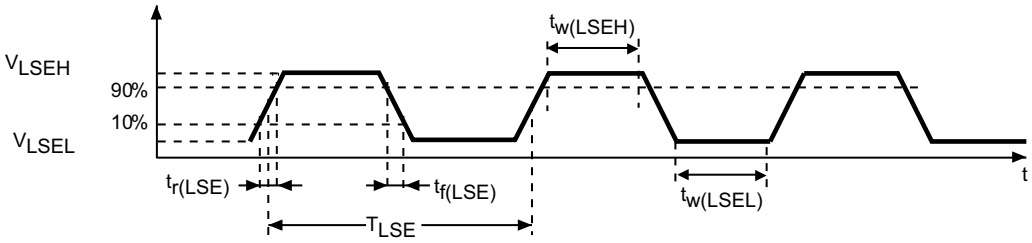
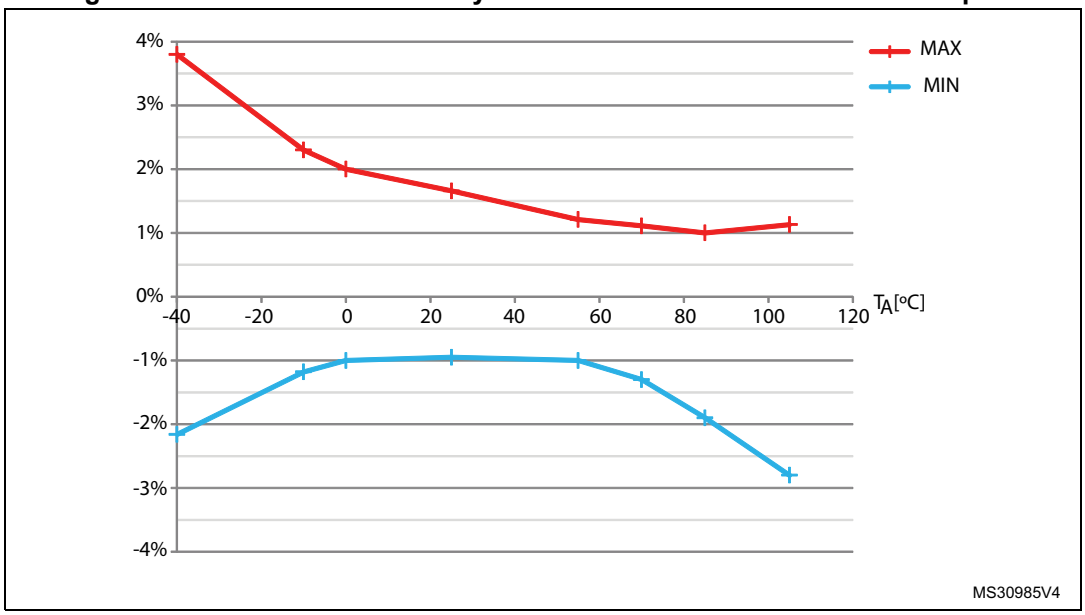


Figure 18. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.

Figure 26. SPI timing diagram - slave mode and CPHA = 0

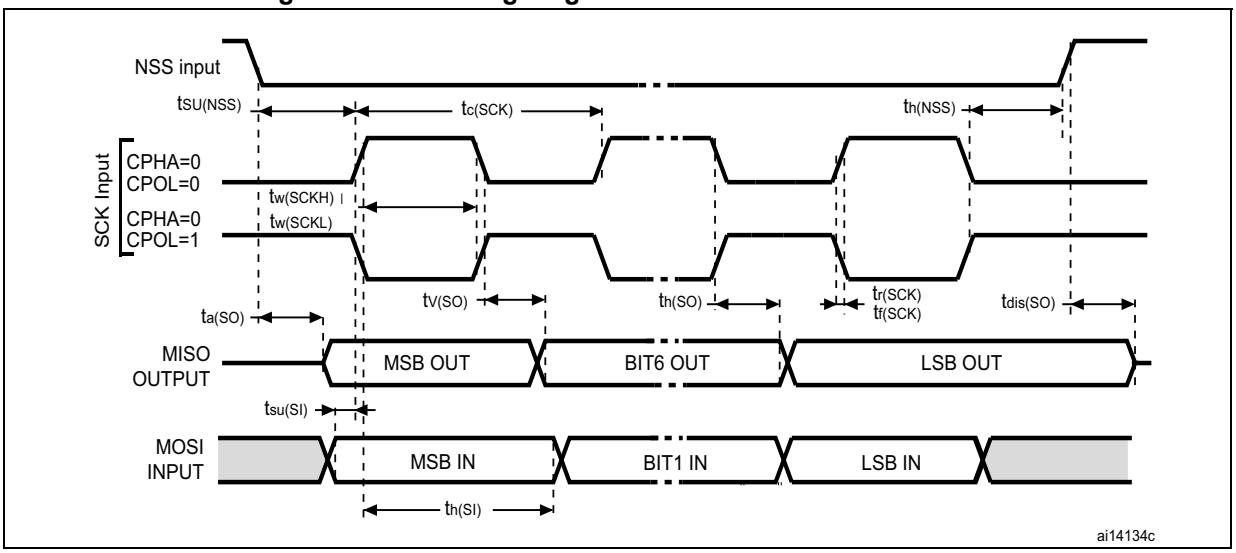
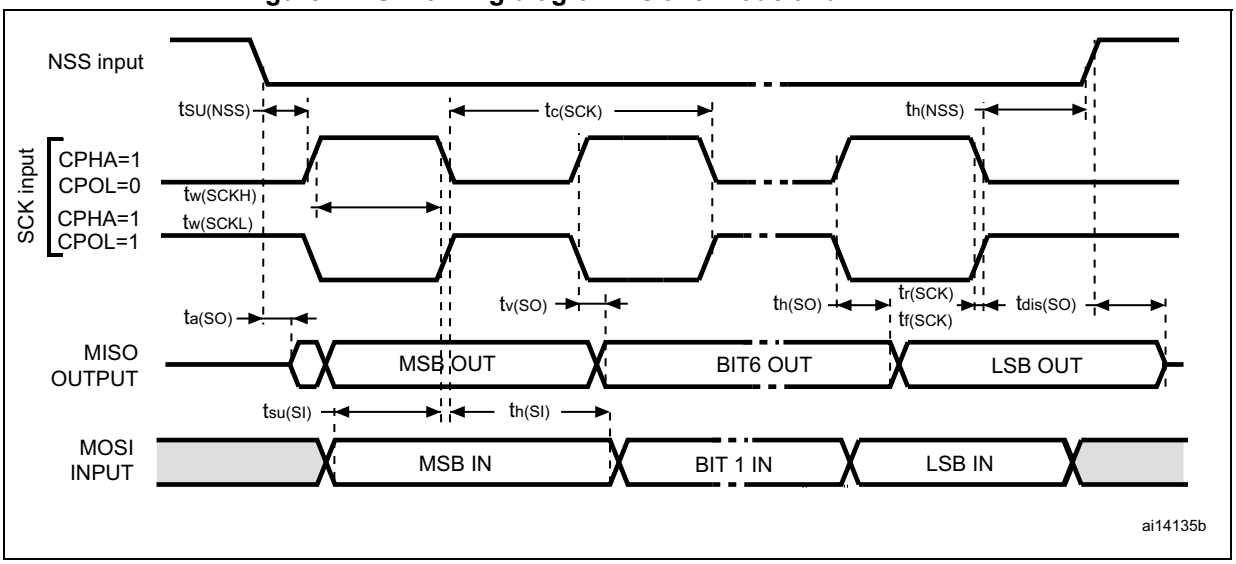


Figure 27. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

USB characteristics

Table 65. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 66. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F303xB/STM32F303xC USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers.

Figure 31. USB timings: definition of data signal rise and fall time

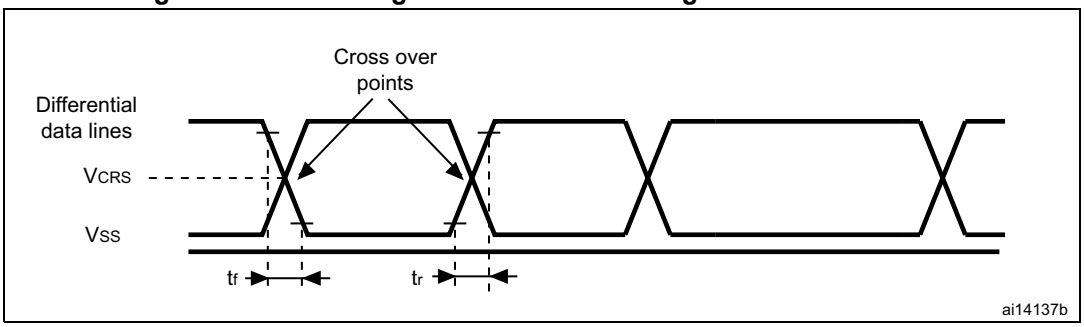


Figure 32. ADC typical current consumption on VDDA pin

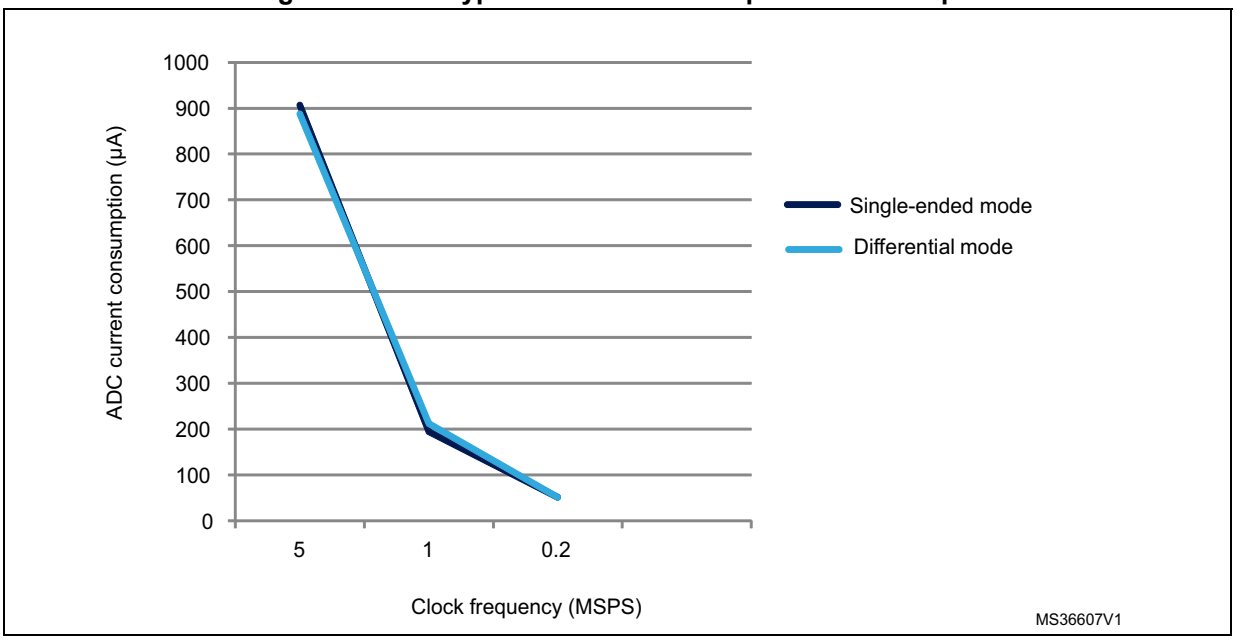
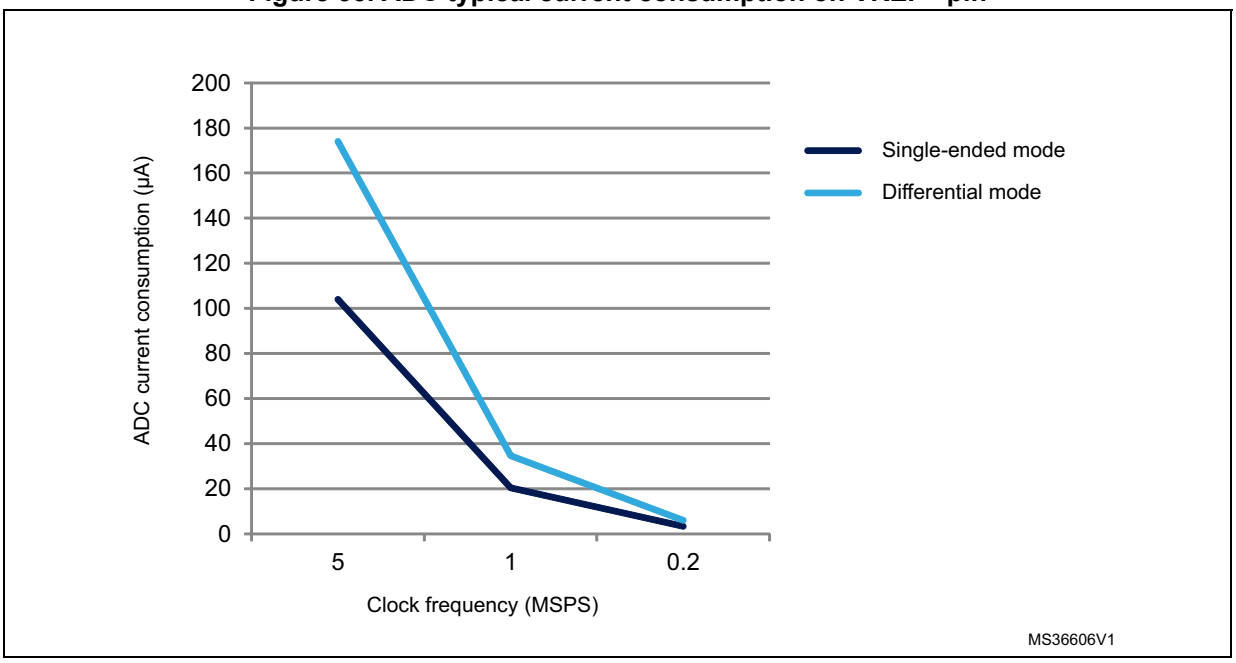


Figure 33. ADC typical current consumption on VREF+ pin



6.3.19 DAC electrical specifications

Table 75. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.4	-	3.6	V
R_{LOAD} (1)	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
R_O (1)	Output impedance	DAC output buffer OFF		-	-	15	kΩ
C_{LOAD} (1)	Capacitive load	DAC output buffer ON		-	-	50	pF
V_{DAC_OUT} (1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V DAC output buffer ON.		0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		-	0.5	V_{DDA} - 1LSB	mV
I_{DDA} (3)	DAC DC current consumption in quiescent mode (Standby mode)(2)	With no load, middle code (0x800) on the input.		-	-	380	µA
		With no load, worst code (0xF1C) on the input.		-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code		-	-	±0.5	LSB
		Given for a 12-bit input code		-	-	±2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code		-	-	±1	LSB
		Given for a 12-bit input code		-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)	-		-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V		-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V		-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code		-	-	±0.5	%
$t_{SETTLING}$ (3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ		-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ		-	-	1	MS/s

6.3.20 Comparator characteristics

Table 76. Comparator characteristics(1)

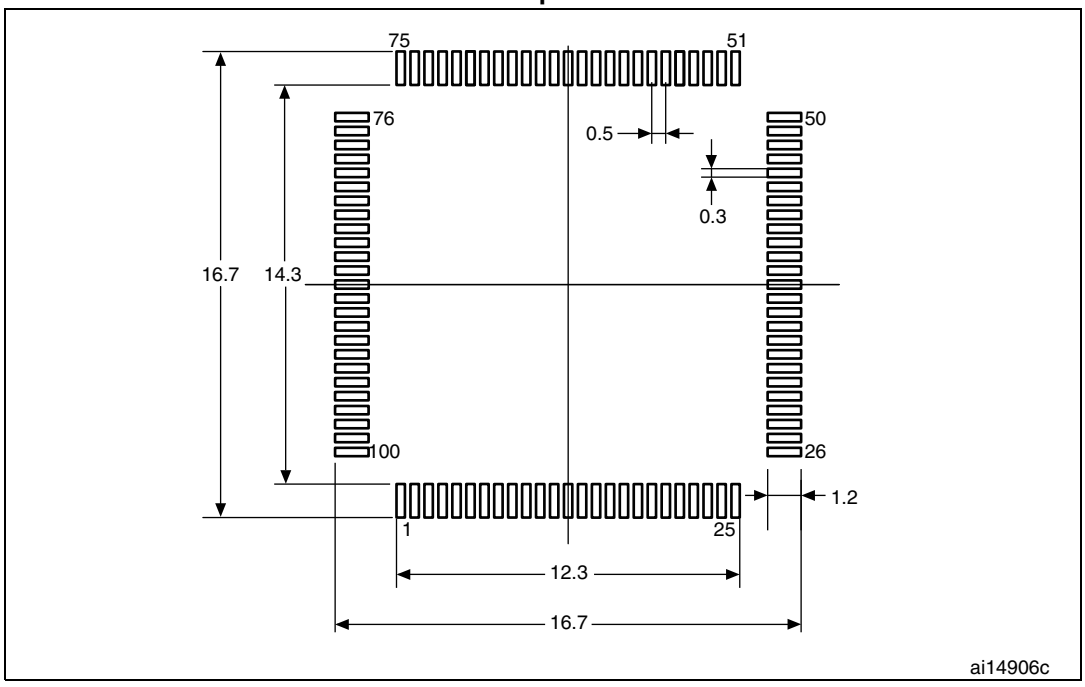
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		-	1.2	-	
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1(2)	s
		Next activations		-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low-power mode		-	2	4.5	µs
		Low-power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low-power mode		-	2	7	µs
		Low-power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low-power mode		-	1.2	1.5	µA
		Low-power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Table 81. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.2	0.0035	-	0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3	-	12.00	-	-	0.4724	-
E	15.80	16.00	16.2	0.622	0.6299	0.6378
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3	-	12.00	-	-	0.4724	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

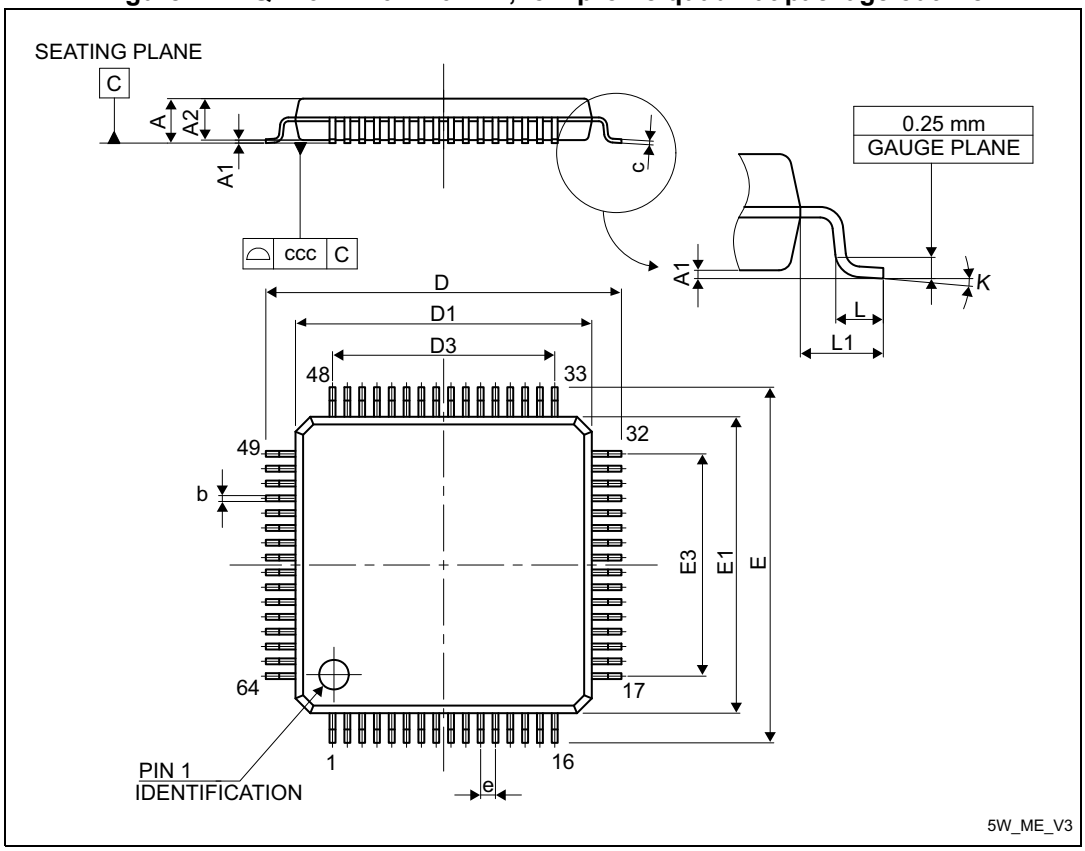
Figure 40. LQFP100 – 14 x 14 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

7.2 LQFP64 – 10 x 10 mm, low-profile quad flat package information

Figure 42. LQFP64 – 10 x 10 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 82. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.0035		0.0079
D	-	12.00	-	-	0.4724	-
D1	-	10.00	-	-	0.3937	-
D3	-	7.50	-	-	0.2953	-
E	-	12.00	-	-	0.4724	-

7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F303xB/STM32F303xC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 61.6 mW:

P_{Dmax} = 175 + 61.6 = 236.6 mW

Thus: P_{Dmax} = 236.6 mW

Using the values obtained in *Table 86* T_{Jmax} is calculated as follows:

– For LQFP64, 45°C/W

T_{Jmax} = 82 °C + (45°C/W × 236.6 mW) = 82 °C + 10.65 °C = 92.65 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

Table 88. Document revision history (continued)

Date	Revision	Changes
17-Apr-2015	11	Updated *Section 7: Package information*: with new package information structure adding 1 sub paragraph for each package. Updated *Figure 41: LQFP100 – 14 x 14 mm, low-profile quad flat package top view example* removing gate mark. Added note for all packages about the device marking orientation: “the following figure gives an example of topside marking orientation versus pin 1 identifier location”. Updated *Table 82: LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data*.
11-Dec-2015	12	Added WLCSP100: – Updated cover page. – Updated *Table 2: STM32F303xB/STM32F303xC family device features and peripheral counts*. – Added *Figure 7: STM32F303xB/STM32F303xC WLCSP100 pinout*. – Updated *Table 13: STM32F303xB/STM32F303xC pin definitions*. – Updated *Table 24: General operating conditions*. – Added *Section 7.4: WLCSP100 - 0.4 mm pitch wafer level chip scale package information*. – Updated *Table 86: Package thermal characteristics*. – Updated *Table 87: Ordering information scheme*. Updated *Figure 4*, *Figure 5*, *Figure 6*, *Table 13* and *Table 22* removing all VDD and VSS indexes. Updated all the notes removing ‘not tested in production’. Updated *Table 68: ADC characteristics* adding V_{REF-} negative voltage reference. Update *Table 21: Voltage characteristics* adding table note 4.