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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303rbt6tr

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3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.12 Interrupts and events

3.12.1 Nested vectored interrupt controller (NVIC)

The STM32F303xB/STM32F303xC devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

Table 13. STM32F303xB/STM32F303xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
J3	52	34	26	PB13	I/O	TTa	(4)	SPI2_SCK,I2S2_CK,USART3_CTS, TIM1_CH1N, TSC_G6_IO3, EVENTOUT	ADC3_IN5, COMP5_INP, OPAMP4_VINP, OPAMP3_VINP
J2	53	35	27	PB14	I/O	TTa	(4)	SPI2_MISO,I2S2ext_SD, USART3_RTS_DE, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4, EVENTOUT	COMP3_INP, ADC4_IN4, OPAMP2_VINP
H4	54	36	28	PB15	I/O	TTa	(4)	SPI2_MOSI, I2S2_SD, TIM1_CH3N, RTC_REFIN, TIM15_CH1N, TIM15_CH2, EVENTOUT	ADC4_IN5, COMP6_INM
-	55	-	-	PD8	I/O	TTa	(1)	USART3_TX, EVENTOUT	ADC4_IN12, OPAMP4_VINM
G4	56	-	-	PD9	I/O	TTa	(1)	USART3_RX, EVENTOUT	ADC4_IN13
H3	57	-	-	PD10	I/O	TTa	(1)	USART3_CK, EVENTOUT	ADC34_IN7, COMP6_INM
H2	58	-	-	PD11	I/O	TTa	(1)	USART3_CTS, EVENTOUT	ADC34_IN8, COMP6_INP, OPAMP4_VINP
H1	59	-	-	PD12	I/O	TTa	(1)	USART3_RTS_DE, TIM4_CH1, TSC_G8_IO1, EVENTOUT	ADC34_IN9, COMP5_INP
G3	60	-	-	PD13	I/O	TTa	(1)	TIM4_CH2, TSC_G8_IO2, EVENTOUT	ADC34_IN10, COMP5_INM
G2	61	-	-	PD14	I/O	TTa	(1)	TIM4_CH3, TSC_G8_IO3, EVENTOUT	COMP3_INP, ADC34_IN11, OPAMP2_VINP
G1	62	-	-	PD15	I/O	TTa	(1)	SPI2_NSS, TIM4_CH4, TSC_G8_IO4, EVENTOUT	COMP3_INM
F4	63	37	-	PC6	I/O	FT	(1)	I2S2_MCK, COMP6_OUT, TIM8_CH1, TIM3_CH1, EVENTOUT	-
F2	64	38	-	PC7	I/O	FT	(1)	I2S3_MCK, TIM8_CH2, TIM3_CH2, COMP5_OUT, EVENTOUT	-
F1	65	39	-	PC8	I/O	FT	(1)	TIM8_CH3, TIM3_CH3, COMP3_OUT, EVENTOUT	-
F3	66	40	-	PC9	I/O	FT	(1)	TIM8_CH4, TIM8_BKIN2,TIM3_CH4, I2S_CKIN, EVENTOUT	-

Table 27. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

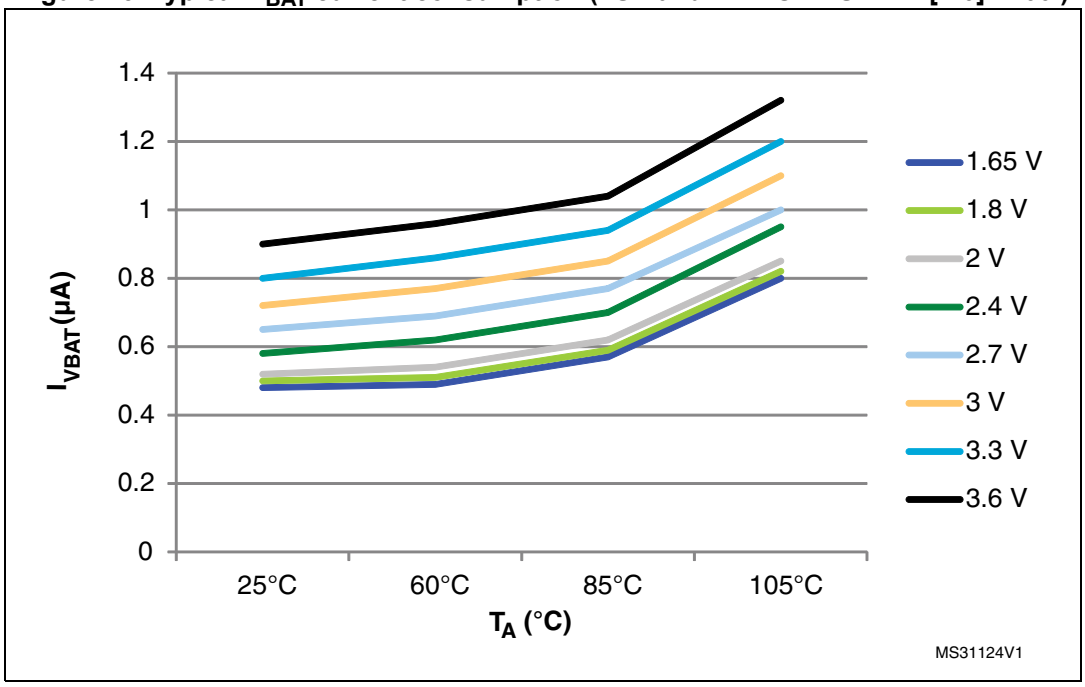
1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 34. Typical and maximum current consumption from V_{BAT} supply

Symbol	Para meter	Conditions (1)	Typ @V_{BAT}								Max @V_{BAT} = 3.6 V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 13. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 35. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	61.3	28.0	mA
			64 MHz	54.8	25.4	
			48 MHz	41.9	19.3	
			32 MHz	28.5	13.3	
			24 MHz	21.8	10.4	
			16 MHz	14.9	7.2	
			8 MHz	7.7	3.9	
			4 MHz	4.5	2.5	
			2 MHz	2.8	1.7	
			1 MHz	1.9	1.3	
			500 kHz	1.4	1.1	
			125 kHz	1.1	0.9	
I_{DDA} (1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	240.3	239.5	µA
			64 MHz	210.9	210.3	
			48 MHz	155.8	155.6	
			32 MHz	105.7	105.6	
			24 MHz	82.1	82.0	
			16 MHz	58.8	58.8	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 36. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	44.1	7.0	mA
			64 MHz	39.7	6.3	
			48 MHz	30.3	4.9	
			32 MHz	20.5	3.5	
			24 MHz	15.4	2.8	
			16 MHz	10.6	2.0	
			8 MHz	5.4	1.1	
			4 MHz	3.2	1.0	
			2 MHz	2.1	0.9	
			1 MHz	1.5	0.8	
			500 kHz	1.2	0.8	
			125 kHz	1.0	0.8	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.7	238.5	µA
			64 MHz	210.5	209.6	
			48 MHz	155.0	155.6	
			32 MHz	105.3	105.2	
			24 MHz	81.9	81.8	
			16 MHz	58.7	58.6	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 43. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=10 medium low driving capability	-	-	1	
		LSEDRV[1:0]=01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]=10 medium low driving capability	8	-	-	
		LSEDRV[1:0]=01 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 52. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 53*.

6.3.17 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev.03 for:

- Standard-mode (Sm) : with a bit rate up to 100 Kbits/s
- Fast-mode (Fm) : with a bit rate up to 400 Kbits/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1Mbits/s

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

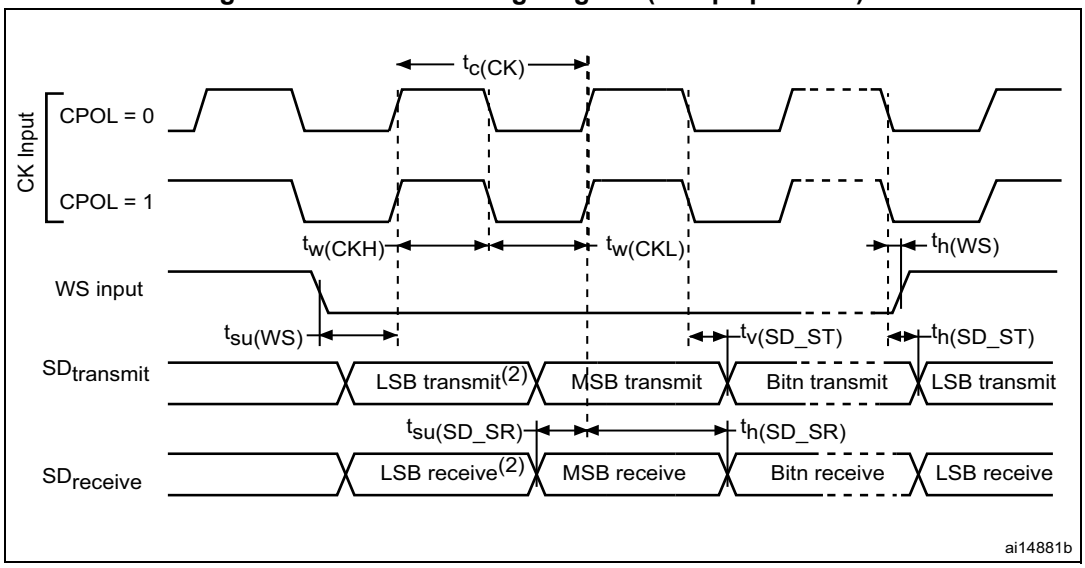
The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics*.

All I²C I/Os embed an analog filter. refer to the *Table 62: I2C analog filter characteristics*.

Table 61. I2C timings specification (see I2C specification, rev.03, June 2007)(1)

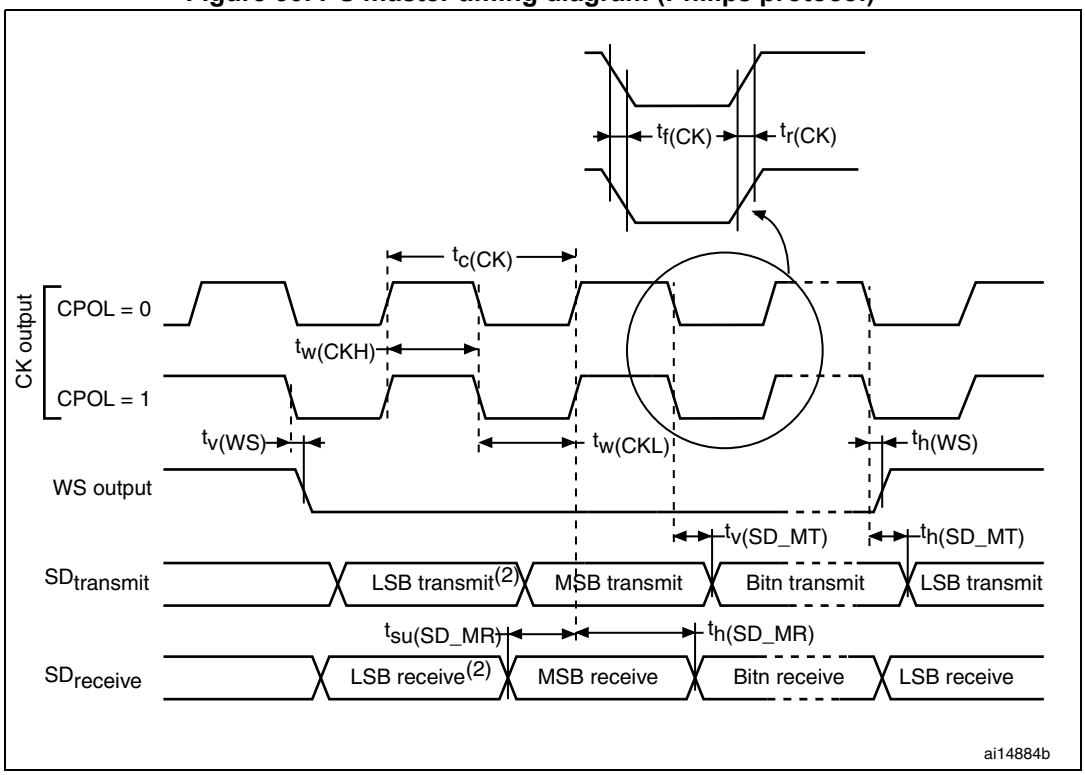
Symbol	Parameter	Standard mode		Fast mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4		0.6		0.26	-	µs
t_r	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
t_f	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD:STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26		µs
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF
t_{SP}	Pulse width of spikes that are suppressed by the analog filter for Standard and Fast mode	0	50(3)	0	50(3)	-	-	ns

Figure 29. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 30. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 71. ADC accuracy, 100-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2 V ≤ V_{DDA} , V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single Ended	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
ENOB (5)	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.2	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	

Table 72. ADC accuracy - limited test conditions, 64-pin packages(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

6.3.19 DAC electrical specifications

Table 75. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.4	-	3.6	V
R_{LOAD} (1)	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
R_O (1)	Output impedance	DAC output buffer OFF		-	-	15	kΩ
C_{LOAD} (1)	Capacitive load	DAC output buffer ON		-	-	50	pF
V_{DAC_OUT} (1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V DAC output buffer ON.		0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		-	0.5	V_{DDA} - 1LSB	mV
I_{DDA} (3)	DAC DC current consumption in quiescent mode (Standby mode)(2)	With no load, middle code (0x800) on the input.		-	-	380	µA
		With no load, worst code (0xF1C) on the input.		-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code		-	-	±0.5	LSB
		Given for a 12-bit input code		-	-	±2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code		-	-	±1	LSB
		Given for a 12-bit input code		-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)	-		-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V		-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V		-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code		-	-	±0.5	%
$t_{SETTLING}$ (3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ		-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ		-	-	1	MS/s

6.3.20 Comparator characteristics

Table 76. Comparator characteristics(1)

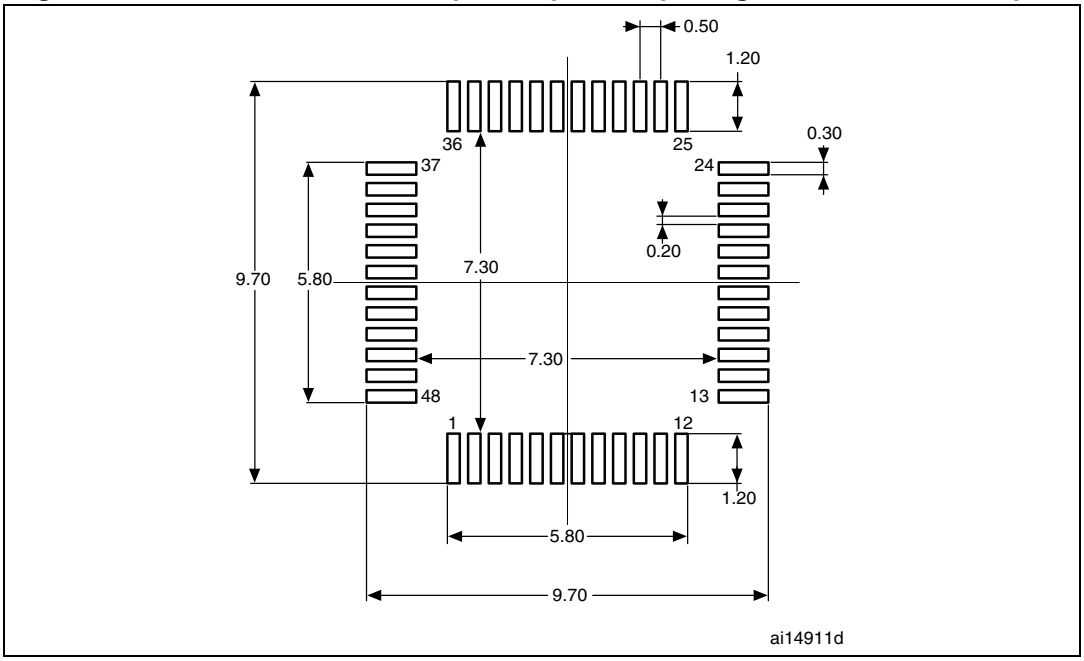
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		-	1.2	-	
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1(2)	s
		Next activations		-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low-power mode		-	2	4.5	µs
		Low-power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low-power mode		-	2	7	µs
		Low-power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low-power mode		-	1.2	1.5	µA
		Low-power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3	-	5.50	-	-	0.2165	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

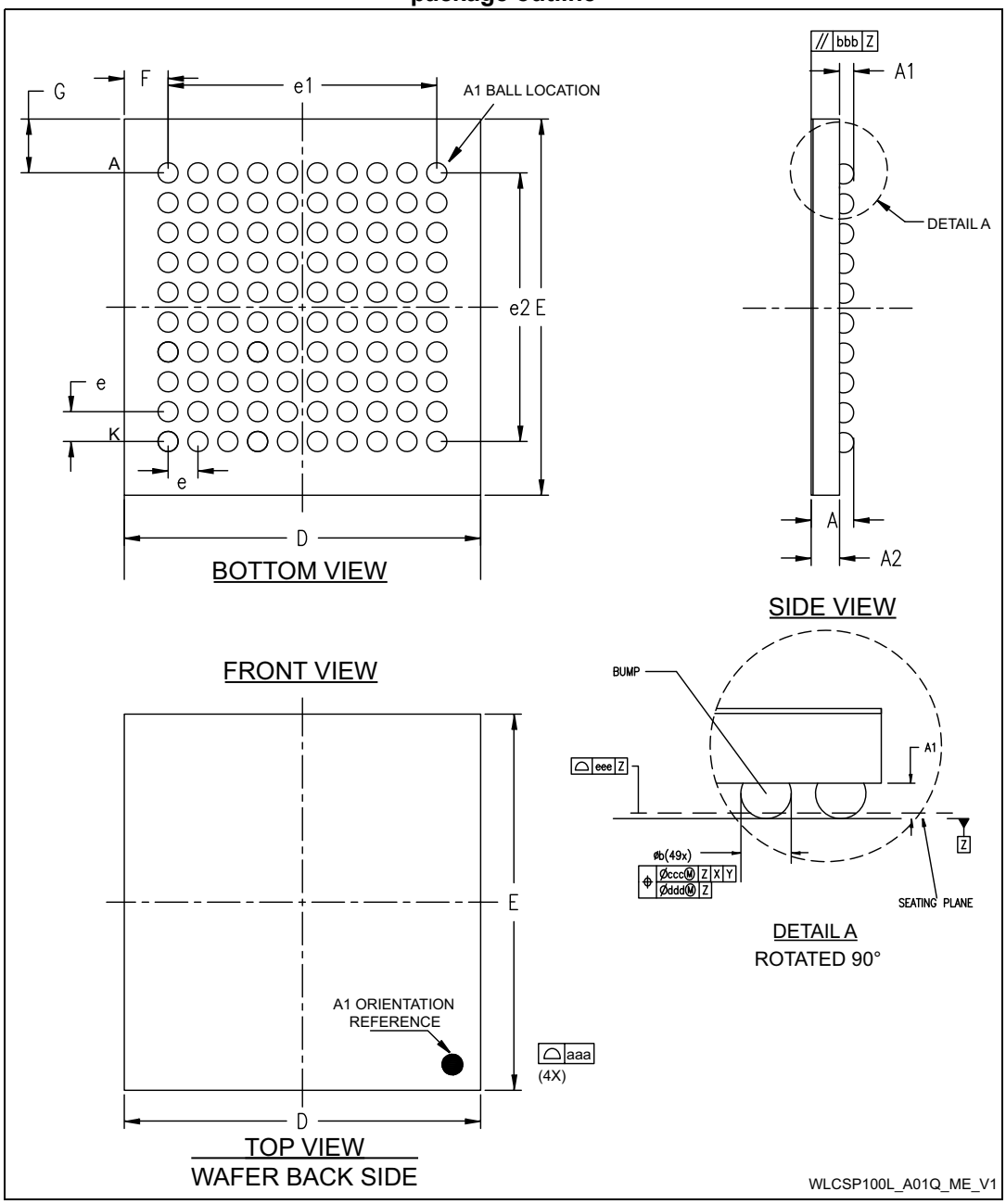
Figure 46. LQFP48 - 7 x 7 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

7.4 WLCSP100 - 0.4 mm pitch wafer level chip scale package information

Figure 48.WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Figure 49. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint

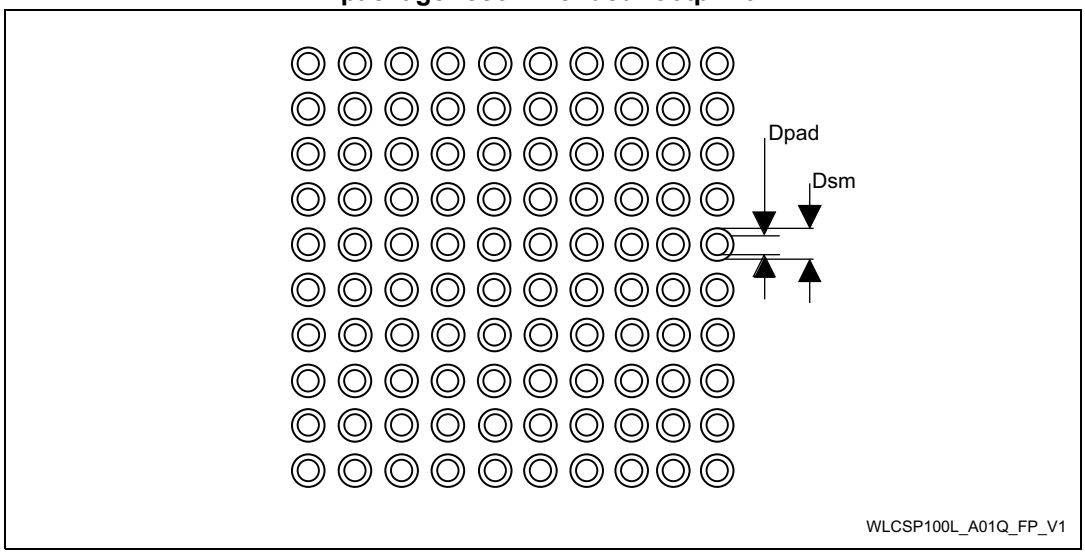


Table 85. WLCSP100 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

8 Ordering information

Table 87. Ordering information scheme

Example: STM32 F 303 R B T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

303 = STM32F303xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 88. Document revision history (continued)

Date	Revision	Changes
06-May-2016	13	Updated *Table 43: LSE oscillator characteristics (fLSE = 32.768 kHz)* LSEDRV[1:0] bits. Updated *Table 28: Embedded internal reference voltage* V_{REFINT} internal reference voltage (min and typ values). Updated *Figure 5: STM32F303xB/STM32F303xC LQFP64 pinout* replacing VSS by PF4. Updated *Table 51: ESD absolute maximum ratings* ESD CDM at class 3 and 4 including WLCSP100 package information. Updated *Table 13: STM32F303xB/STM32F303xC pin definitions*: – Adding ‘digital power supply’ in the Pin function column at the line corresponding to K8/28/19 pins. – Adding VSS digital ground line with WLCSP100 K9 and K10 pins connected. – Replacing in VDD line for WLCSP100: ‘A10, B10’ by ‘A9, A10, B10, B8’. Updated *Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port*. Updated *Table 77: Operational amplifier characteristics* high saturation and low saturation voltages. Updated *Table 13: STM32F303xB/STM32F303xC pin definitions* adding note ‘Fast ADC channel’ for ADCx_IN1..5. Updated *Table 75: DAC characteristics* resistive load. Updated *Table 68: ADC characteristics* adding CMIR parameter and modifying tSTAB parameter characteristics.