**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 22x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303rbt7tr |

# Contents

### 3.7.4 Low-power modes

The STM32F303xB/STM32F303xC supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

*Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

**Table 4. STM32F303xB/STM32F303xC peripheral interconnect matrix**

| Interconnect source | Interconnect destination | Interconnect action |
|---|---|---|
| TIMx | TIMx | Timers synchronization or chaining |
| | ADCx<br>DAC1 | Conversion triggers |
| | DMA | Memory to memory transfer trigger |
| | Compx | Comparator output blanking |
| COMPx | TIMx | Timer input: OCREF_CLR input, input capture |
| ADCx | TIMx | Timer triggered by analog watchdog |

## 3.22 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI1, SPI2 and SPI3.

**Table 9. STM32F303xB/STM32F303xC SPI/I2S implementation**

| SPI features(1) | SPI1 | SPI2 | SPI3 |
|---|---|---|---|
| Hardware CRC calculation | X | X | X |
| Rx/Tx FIFO | X | X | X |
| NSS pulse mode | X | X | X |
| I2S mode | - | X | X |
| TI mode | X | X | X |

1. **X = supported.**

## 3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

## 3.24 Universal serial bus (USB)

The STM32F303xB/STM32F303xC devices embed an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator). The USB has a dedicated 512-bytes SRAM memory for data transmission and reception.

Table 13. STM32F303xB/STM32F303xC pin definitions (continued)

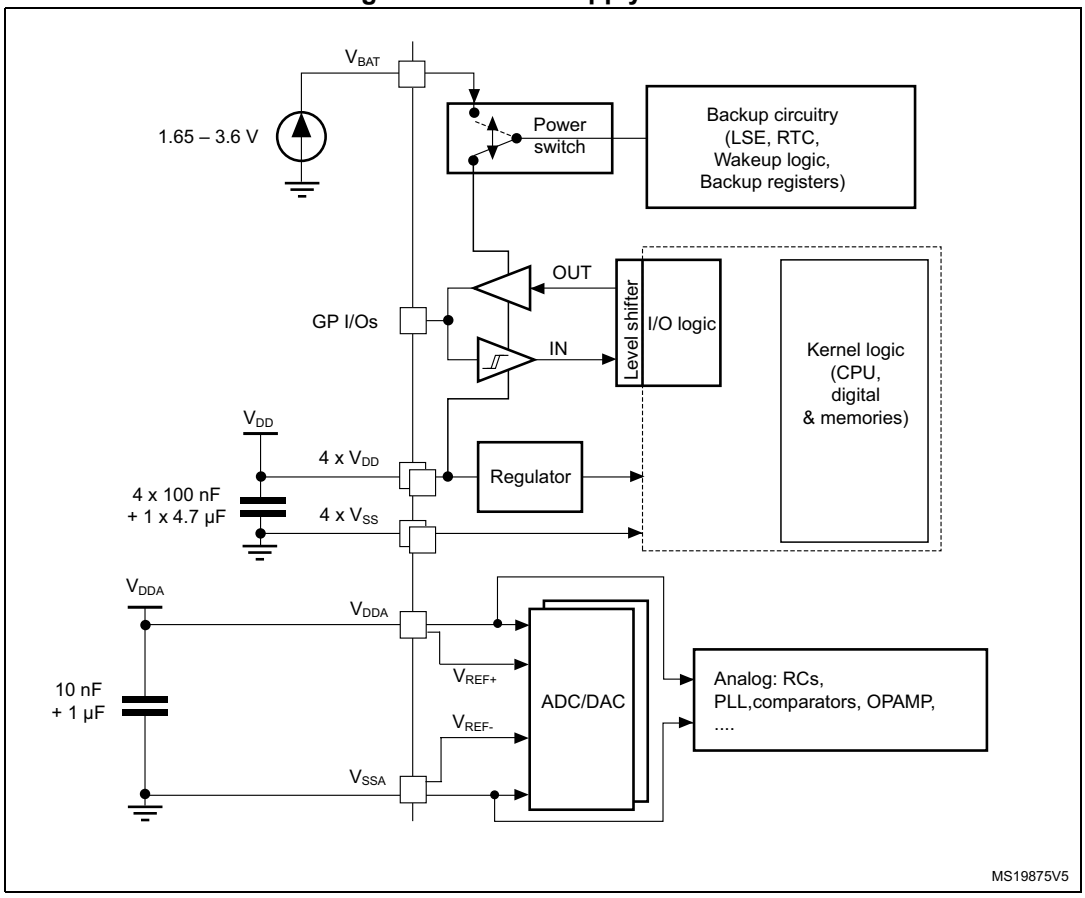
| Pin number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| WLCSP100 | LQFP100 | LQFP64 | LQFP48 | | | | | Alternate functions | Additional functions |
| B2 | 77 | 50 | 38 | PA15 | I/O | FTf | - | I2C1_SCL, SPI1_NSS, SPI3_NSS, I2S3_WS, JTDI, USART2_RX, TIM1_BKIN, TIM2_CH1_ETR, TIM8_CH1, EVENTOUT | - |
| E4 | 78 | 51 | - | PC10 | I/O | FT | (1) | SPI3_SCK, I2S3_CK, USART3_TX, UART4_TX, TIM8_CH1N, EVENTOUT | - |
| D3 | 79 | 52 | - | PC11 | I/O | FT | (1) | SPI3_MISO, I2S3ext_SD, USART3_RX, UART4_RX, TIM8_CH2N, EVENTOUT | - |
| A3 | 80 | 53 | - | PC12 | I/O | FT | (1) | SPI3_MOSI, I2S3_SD, USART3_CK, UART5_TX, TIM8_CH3N, EVENTOUT | - |
| B3 | 81 | - | - | PD0 | I/O | FT | (1) | CAN_RX, EVENTOUT | - |
| C3 | 82 | - | - | PD1 | I/O | FT | (1) | CAN_TX, TIM8_CH4, TIM8_BKIN2,EVENTOUT | - |
| A4 | 83 | 54 | - | PD2 | I/O | FT | (1) | UART5_RX, TIM3_ETR, TIM8_BKIN, EVENTOUT | - |
| B4 | 84 | - | - | PD3 | I/O | FT | (1) | USART2_CTS, TIM2_CH1_ETR, EVENTOUT | - |
| C4 | 85 | - | - | PD4 | I/O | FT | (1) | USART2_RTS_DE, TIM2_CH2, EVENTOUT | - |
| - | 86 | - | - | PD5 | I/O | FT | (1) | USART2_TX, EVENTOUT | - |
| - | 87 | - | - | PD6 | I/O | FT | (1) | USART2_RX, TIM2_CH4, EVENTOUT | - |
| D4 | 88 | - | - | PD7 | I/O | FT | (1) | USART2_CK, TIM2_CH3, EVENTOUT | - |
| A5 | 89 | 55 | 39 | PB3 | I/O | FT | - | SPI3_SCK, I2S3_CK, SPI1_SCK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM8_CH1N, TSC_G5_IO1, JTDO-TRACESWO, EVENTOUT | - |

**Table 16. Alternate functions for port C**

| Port & Pin Name | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|
| PC0 | EVENTOUT | - | - | - | - | - | - |
| PC1 | EVENTOUT | - | - | - | - | - | - |
| PC2 | EVENTOUT | - | COMP7_OUT | - | - | - | - |
| PC3 | EVENTOUT | - | - | - | - | TIM1_BKIN2 | - |
| PC4 | EVENTOUT | - | - | - | - | - | USART1_TX |
| PC5 | EVENTOUT | - | TSC_G3_IO1 | - | - | - | USART1_RX |
| PC6 | EVENTOUT | TIM3_CH1 | - | TIM8_CH1 | - | I2S2_MCK | COMP6_OUT |
| PC7 | EVENTOUT | TIM3_CH2 | - | TIM8_CH2 | - | I2S3_MCK | COMP5_OUT |
| PC8 | EVENTOUT | TIM3_CH3 | - | TIM8_CH3 | - | - | COMP3_OUT |
| PC9 | EVENTOUT | TIM3_CH4 | - | TIM8_CH4 | I2S_CKIN | TIM8_BKIN2 | - |
| PC10 | EVENTOUT | - | - | TIM8_CH1N | UART4_TX | SPI3_SCK, I2S3_CK | USART3_TX |
| PC11 | EVENTOUT | - | - | TIM8_CH2N | UART4_RX | SPI3_MISO, I2S3ext_SD | USART3_RX |
| PC12 | EVENTOUT | - | - | TIM8_CH3N | UART5_TX | SPI3_MOSI, I2S3_SD | USART3_CK |
| PC13 | - | - | - | TIM1_CH1N | - | - | - |
| PC14 | - | - | - | - | - | - | - |
| PC15 | - | - | - | - | - | - | - |

### 6.1.6 Power supply scheme

**Figure 11. Power supply scheme**

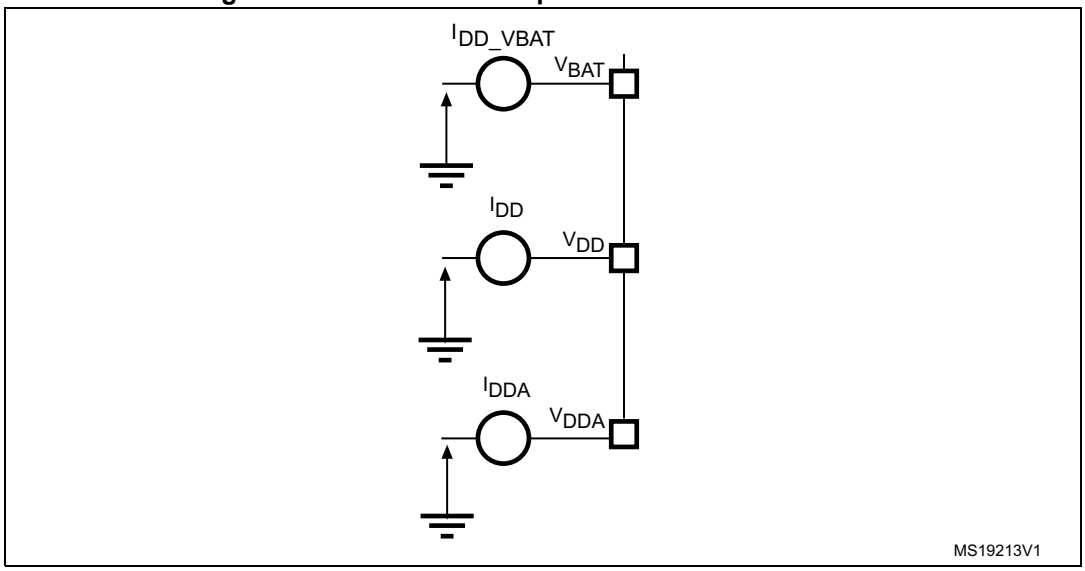



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

### 6.1.7 Current consumption measurement

**Figure 12. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

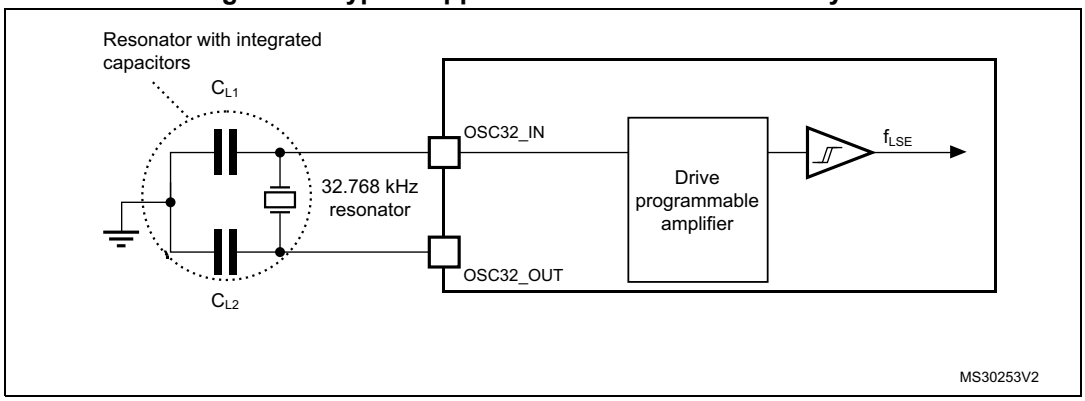
Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics*, and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 21. Voltage characteristics(1)**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{BAT}$ and $V_{DD}$) | -0.3 | 4.0 | V |
| $V_{DD}$–$V_{DDA}$ | Allowed voltage difference for $V_{DD} > V_{DDA}$ | - | 0.4 | |
| $V_{REF+}$–$V_{DDA}$(2) | Allowed voltage difference for $V_{REF+} > V_{DDA}$ | - | 0.4 | |
| $V_{IN}$(3) | Input voltage on FT and FTf pins | $V_{SS}$ –0.3 | $V_{DD}$ + 4.0 | |
| | Input voltage on TTa pins | $V_{SS}$ –0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ –0.3 | 4.0 | |
| | Input voltage on Boot0 pin | 0 | 9 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins(4) | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.12: Electrical sensitivity characteristics* | | - |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between $V_{DDA}$ and $V_{DD}$:
$V_{DDA}$ must power on before or at the same time as $V_{DD}$ in the power up sequence.
$V_{DDA}$ must be greater than or equal to $V_{DD}$.

**Figure 17. Typical application with a 32.768 kHz crystal**




*Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

## 6.3.8 Internal clock source characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

### High-speed internal (HSI) RC oscillator

**Table 44. HSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 8 | - | MHz |
| TRIM | HSI user trimming step | - | - | - | 1(2) | % |
| $DuCy_{(HSI)}$ | Duty cycle | - | 45(2) | - | 55(2) | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | $T_A$ = -40 to 105°C | -2.8(3) | - | 3.8(3) | % |
| | | $T_A$ = -10 to 85°C | -1.9(3) | - | 2.3(3) | |
| | | $T_A$ = 0 to 85°C | -1.9(3) | - | 2(3) | |
| | | $T_A$ = 0 to 70°C | -1.3(3) | - | 2(3) | |
| | | $T_A$ = 0 to 55°C | -1(3) | - | 2(3) | |
| | | $T_A$ = 25°C(4) | -1 | - | 1 | |
| $t_{su(HSI)}$ | HSI oscillator startup time | - | 1(2) | - | 2(2) | µs |
| $I_{DDA(HSI)}$ | HSI oscillator power consumption | - | - | 80 | 100(2) | µA |

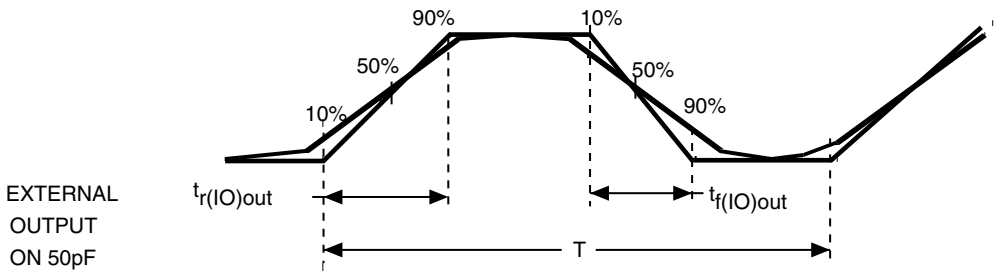
1. $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

**Table 53. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 | – 0 | NA | mA |
| | Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5, PB2 with induced leakage current on other pins from this group less than -50 µA | – 5 | - | |
| | Injected current on PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than -50 µA | – 5 | - | |
| | Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5, PB2, PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than 400 µA | - | +5 | |
| | Injected current on any other FT and FTf pins | – 5 | NA | |
| | Injected current on any other pins | – 5 | +5 | |

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

**Figure 23. I/O AC characteristics definition**




Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

ai14131c

## 6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 57. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | - | - | - | $0.3V_{DD}$+ 0.07(1) | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | - | $0.445V_{DD}$+ 0.398(1) | - | - | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $V_{F(NRST)}$(1) | NRST Input filtered pulse | - | - | - | 100(1) | ns |
| $V_{NF(NRST)}$(1) | NRST Input not filtered pulse | - | 500(1) | - | - | ns |

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

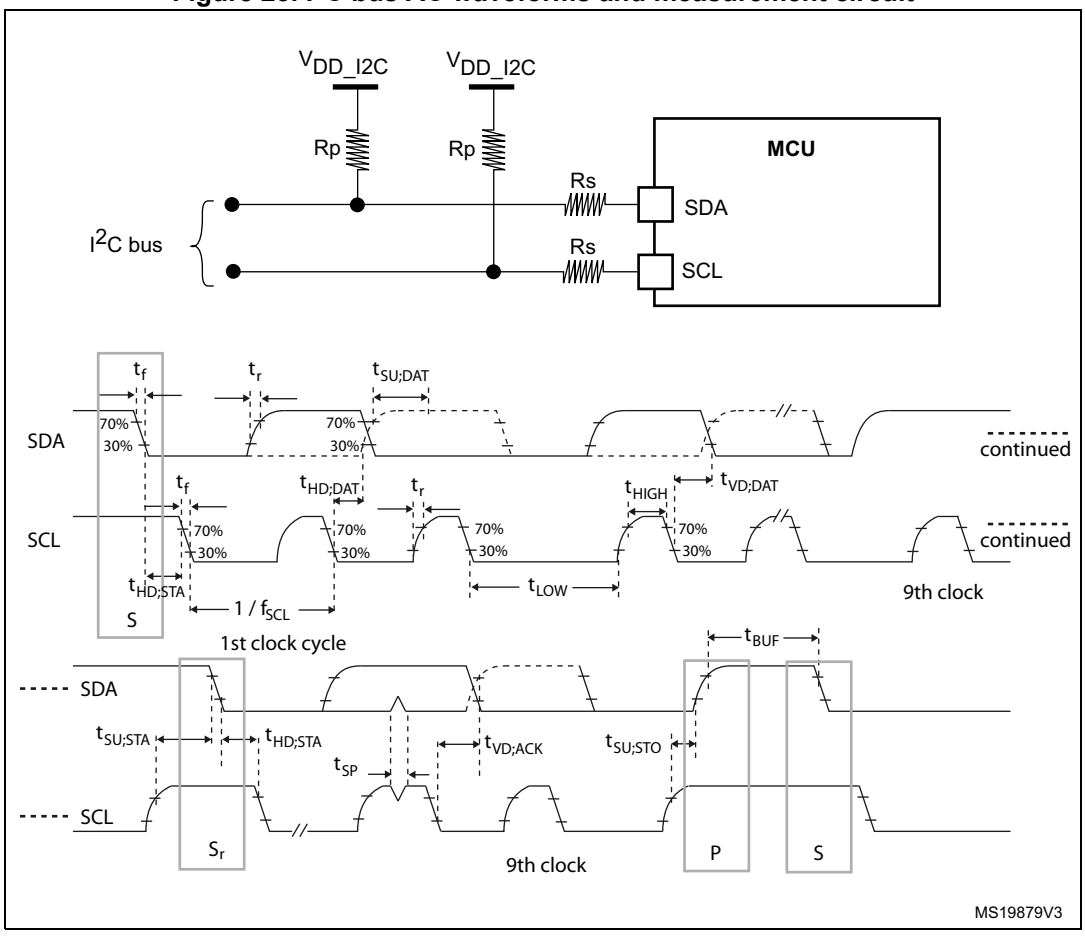
1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to the RM0316 reference manual).
2. The maximum tHD;DAT could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of tVD;DAT or tVD;ACK by a transition time.
3. The minimum width of the spikes filtered by the analog filter is above $t_{SP}$(max).

**Table 62. I2C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Pulse width of spikes that are suppressed by the analog filter | 50 | 260 | ns |

1. Guaranteed by design.

**Figure 25. I²C bus AC waveforms and measurement circuit**




1. Rs: Series protection resistors, Rp: Pull-up resistors, VDD_I2C: I2C bus supply.

**Table 67. USB: Full-speed electrical characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Driver characteristics** | | | | | | |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | - | 20 | ns |
| $t_f$ | Fall time(2) | $C_L$ = 50 pF | 4 | - | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | - | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | - | 1.3 | - | 2.0 | V |
| Output driver Impedance(3) | $Z_{DRV}$ | driving high and low | 28 | 40 | 44 | Ω |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

### CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

### 6.3.19 DAC electrical specifications

**Table 75. DAC characteristics**

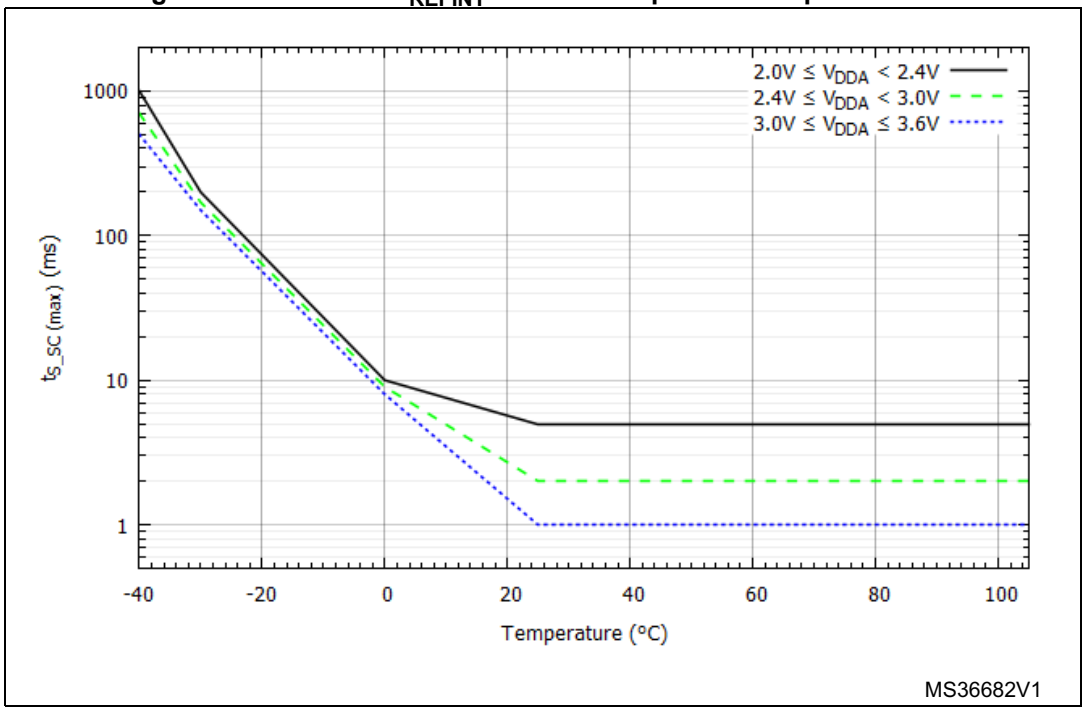
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 2.4 | - | 3.6 | V |
| $R_{LOAD}$ (1) | Resistive load | DAC output buffer ON | Connected to $V_{SSA}$ | 5 | - | - | kΩ |
| | | | Connected to $V_{DDA}$ | 25 | - | - | |
| $R_O$ (1) | Output impedance | DAC output buffer OFF | | - | - | 15 | kΩ |
| $C_{LOAD}$ (1) | Capacitive load | DAC output buffer ON | | - | - | 50 | pF |
| $V_{DAC\_OUT}$ (1) | Voltage on DAC_OUT output | Corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA}$ = 3.6 V and (0x155) and (0xEAB) at $V_{DDA}$ = 2.4 V DAC output buffer ON. | | 0.2 | - | $V_{DDA}$ – 0.2 | V |
| | | DAC output buffer OFF | | - | 0.5 | $V_{DDA}$ - 1LSB | mV |
| $I_{DDA}$ (3) | DAC DC current consumption in quiescent mode (Standby mode)(2) | With no load, middle code (0x800) on the input. | | - | - | 380 | µA |
| | | With no load, worst code (0xF1C) on the input. | | - | - | 480 | µA |
| DNL(3) | Differential non linearity Difference between two consecutive code-1LSB) | Given for a 10-bit input code | | - | - | ±0.5 | LSB |
| | | Given for a 12-bit input code | | - | - | ±2 | LSB |
| INL(3) | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095) | Given for a 10-bit input code | | - | - | ±1 | LSB |
| | | Given for a 12-bit input code | | - | - | ±4 | LSB |
| Offset(3) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}$/2) | - | | - | - | ±10 | mV |
| | | Given for a 10-bit input code at $V_{DDA}$ = 3.6 V | | - | - | ±3 | LSB |
| | | Given for a 12-bit input code at $V_{DDA}$ = 3.6 V | | - | - | ±12 | LSB |
| Gain error(3) | Gain error | Given for a 12-bit input code | | - | - | ±0.5 | % |
| $t_{SETTLING}$ (3) | Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | $C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ | | - | 3 | 4 | µs |
| Update rate(3) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | $C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ | | - | - | 1 | MS/s |

**Table 76. Comparator characteristics(1) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Comparator hysteresis | No hysteresis (COMPxHYST[1:0]=00) | - | - | 0 | - | mV |
| | | Low hysteresis (COMPxHYST[1:0]=01) | High speed mode | 3 | 8 | 13 | |
| | | | All other power modes | 5 | | 10 | |
| | | Medium hysteresis (COMPxHYST[1:0]=10) | High speed mode | 7 | 15 | 26 | |
| | | | All other power modes | 9 | | 19 | |
| | | High hysteresis (COMPxHYST[1:0]=11) | High speed mode | 18 | 31 | 49 | |
| | | | All other power modes | 19 | | 40 | |

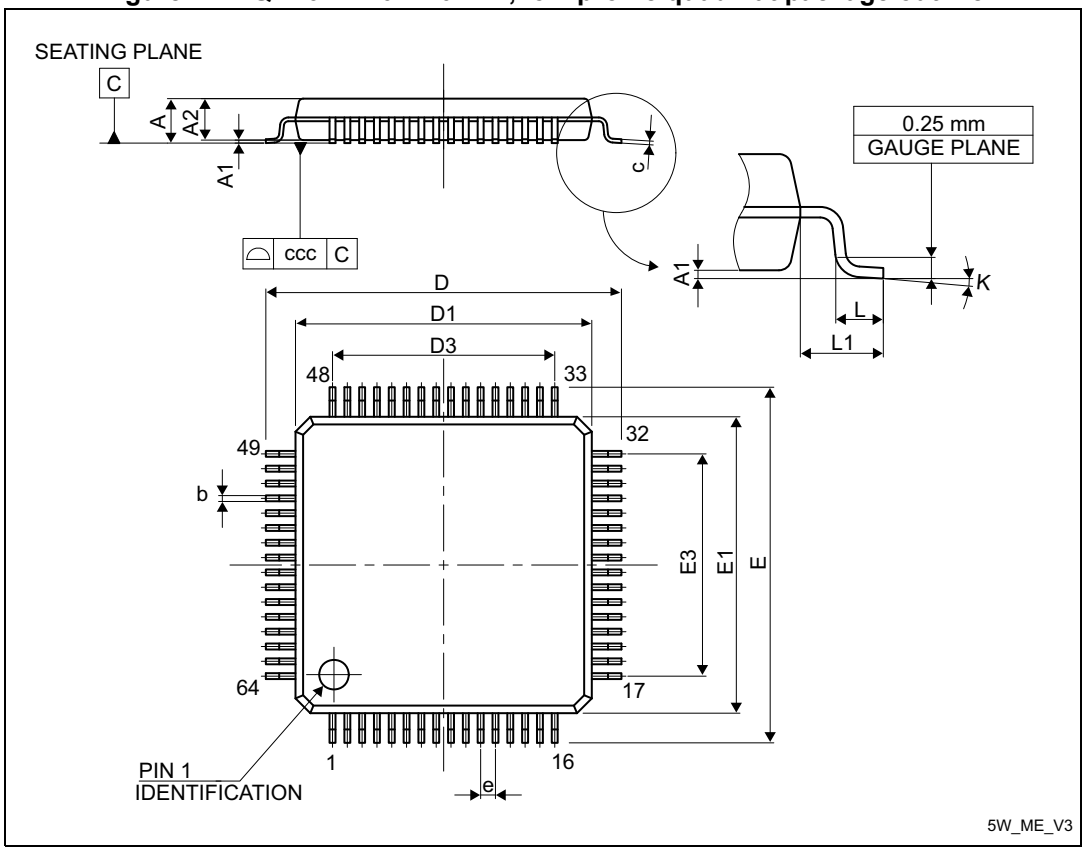
1. Data guaranteed by design.
2. For more details and conditions, see *Figure 37* Maximum $V_{REFINT}$ scaler startup time from power down.

**Figure 37. Maximum $V_{REFINT}$ scaler startup time from power down**



## 7.2 LQFP64 – 10 x 10 mm, low-profile quad flat package information

**Figure 42. LQFP64 – 10 x 10 mm, low-profile quad flat package outline**




1. Drawing is not to scale.

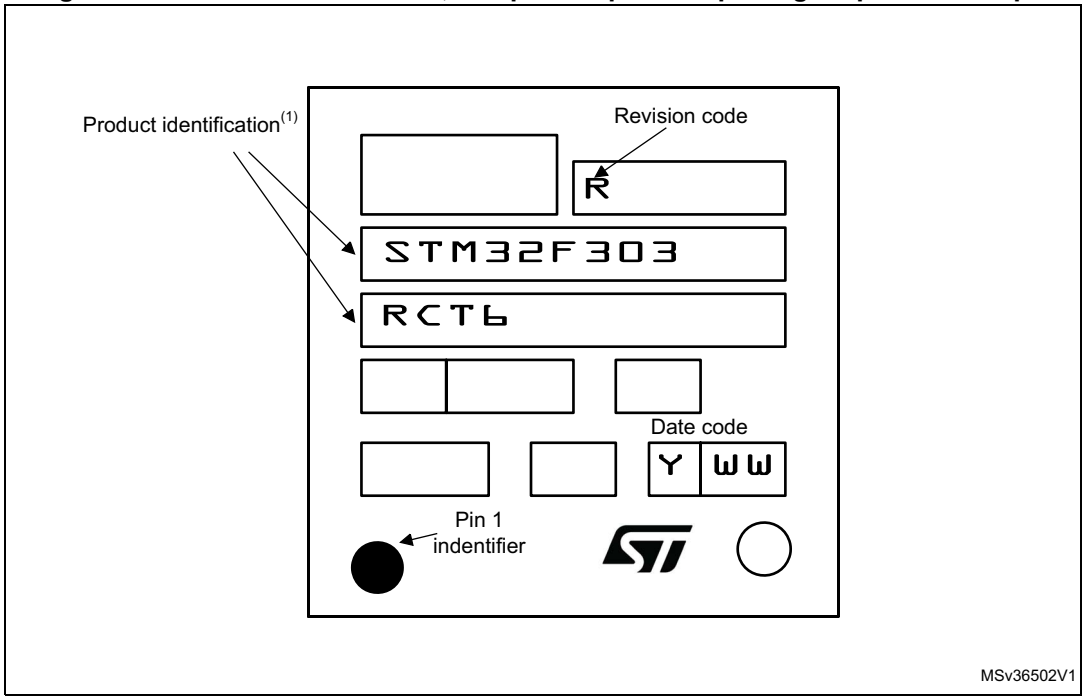
**Table 82. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 0.0630 |
| A1 | 0.05 | - | 0.15 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | - | 0.20 | 0.0035 | | 0.0079 |
| D | - | 12.00 | - | - | 0.4724 | - |
| D1 | - | 10.00 | - | - | 0.3937 | - |
| D3 | - | 7.50 | - | - | 0.2953 | - |
| E | - | 12.00 | - | - | 0.4724 | - |

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

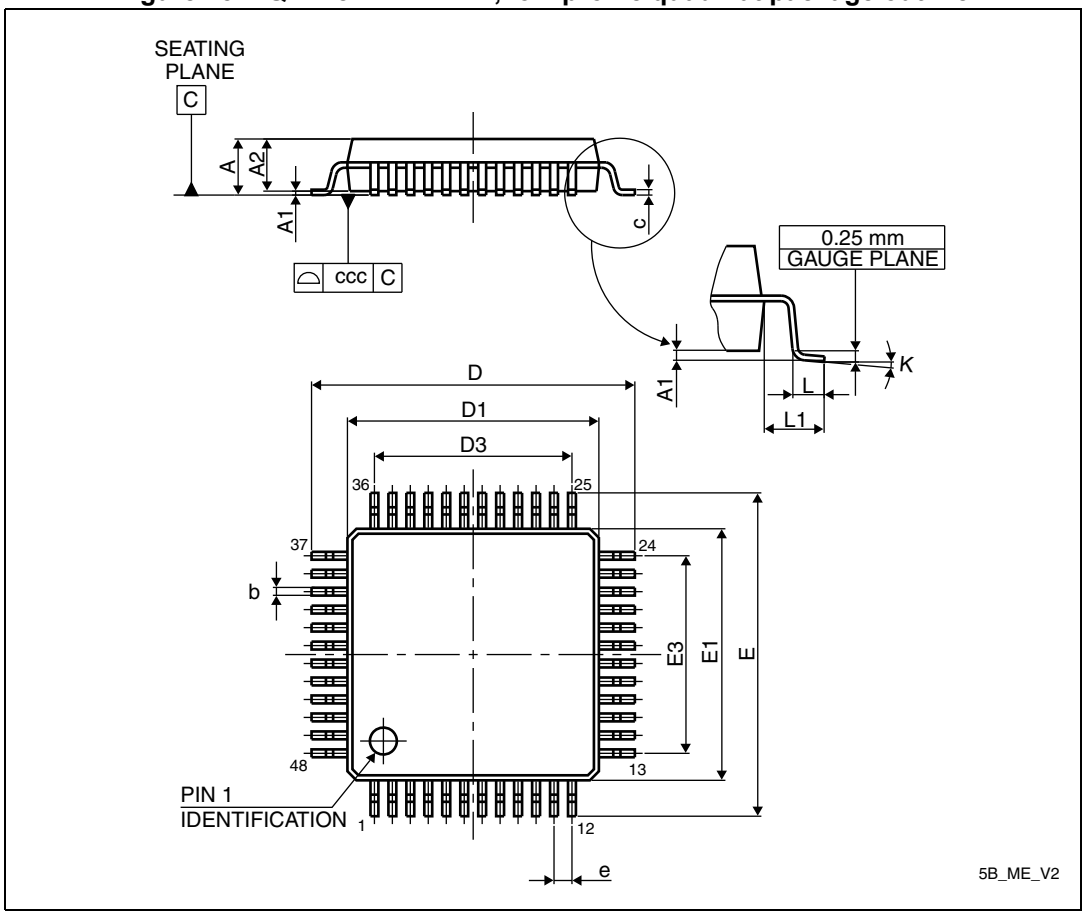
**Figure 44. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.3 LQFP48 – 7 x 7 mm, low-profile quad flat package information

**Figure 45. LQFP48 – 7 x 7 mm, low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 0.0630 |
| A1 | 0.05 | - | 0.15 | 0.0020 | - | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | - | 0.20 | 0.0035 | - | 0.0079 |
| D | 8.80 | 9.00 | 9.20 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.80 | 7.00 | 7.20 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.50 | - | - | 0.2165 | - |
| E | 8.80 | 9.00 | 9.20 | 0.3465 | 0.3543 | 0.3622 |

**Table 88. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 08-Jan-2013 | 5 | Updated $V_{hys}$ and $I_{lkg}$ in *Table 54: I/O static characteristics*.<br>Updated $V_{IL(NRST)}$, $V_{IH(NRST)}$, and $V_{NF(NRST)}$ in *Table 57: NRST pin characteristics*.<br>Updated *Table 70: ADC accuracy - limited test conditions, 100-pin packages* and *Table 64: ADC accuracy - limited test conditions 2)*. |
| 24-Jun-2013 | 6 | Replaced Cortex-M4F with Cortex M4 with FPU<br>Updated Core, Memories and SPI bullet points in *Features*<br>Removed 8KB CCM SRAM from STM32F302xx devices, updated *Figure 2: STM32F303xB/STM32F303xC block diagram* and *Table 3: STM32F303xx family device features and peripheral counts*<br>Updated *Section 3.4: Embedded SRAM*<br>Added VREF+ in *Section 3.14: Digital-to-analog converter (DAC)*<br>Removed DMA support for UART5 in *Table 11: USART features*<br>Added 'reference clock detection' bullet in *Section 3.18: Real-time clock (RTC) and backup registers*<br>Added paragraph 'The touch sensing controller is fully...' in *Section 3.26: Touch sensing controller (TSC)*<br>Updated *Comparison of I2C analog and digital filters*<br>Updated *Section 3.10: General-purpose input/outputs (GPIOs)*<br>Added 'EVENTOUT' in *Table 16: STM32F302xB/STM32F302xC pin definitions* and added note to 'VREF+' pin<br>Updated $\Sigma I_{VDD}$ in *Table 22: Current characteristics* and *Output driving current*<br>Updated *Table 61: I2C timings specification (see I2C specification, rev.03, June 2007)* and *Figure 25: I2C bus AC waveforms and measurement circuit*<br>Added VREF+ row to *Table 68: ADC characteristics*, replaced VDDA with VREF+, updated $t_{conv}$ and added note to 'conversion voltage range<br>Added VREF+ row to *Table 75: DAC characteristics* and replaced VDDA with VREF+<br>Added 'PGA BW' and 'en' in *Table 77: Operational amplifier characteristics* |
| 13-Nov-2013 | 7 | Removed STM32F302xB/STM32F302xC products (now in a separate datasheet).<br>Added I2S feature for SPI2 and SPI3<br>Added $t_{SP}$ to *Table 61: I2C timings specification (see I2C specification, rev.03, June 2007)*.<br>Renamed $t_{SP}$ to $t_{AN}$ in*Table 62: I2C analog filter characteristics*.<br>Added $t_{STAB}$ in *Table 68: ADC characteristics*<br>Renamed $V_{OPAMPx}$ to $_{VREFOPAMPx}$<br>Updated *Table 71: ADC accuracy, 100-pin packages*.<br>Updated ADC channel names in *Section 3.13.1*, *Section 3.13.2* and *Section 3.13.3*. |

**Table 88. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 18-Apr-2014 | 8 | Updated *Table 50: EMI characteristics* conditions :3.3v replaced by 3.6V.<br>Updated *Section 6.3.17: Communications interfaces* $I^2C$ interface.<br>Updated *Table 77: Operational amplifier characteristics* adding TS_OPAMP_VOUT row.<br>Updated *Section 3.13: Fast analog-to-digital converter (ADC)*.<br>updated ARM and Cortex trademark.<br>Updated *Table 32: Typical and maximum VDD consumption in Stop and Standby modes* with Max value at 85°C and 105°C.<br>Updated *Table 70: ADC accuracy - limited test conditions, 100-pin packages* and *Table 71: ADC accuracy, 100-pin packages* for 100-pin package.<br>Added *Table 72: ADC accuracy - limited test conditions, 64-pin packages* and *Table 73: ADC accuracy, 64-pin packages*for 64-pin package.<br>Added *Table 74: ADC accuracy at 1MSPS* for 1MSPS sampling frequency.<br>Updated *Table 63: SPI characteristics*.<br>Updated *Table 75: DAC characteristics*. |
| 09-Dec-2014 | 9 | Updated core description in cover page.<br>Updated HSI characteristics *Table 44: HSI oscillator characteristics* and *Figure 18: HSI oscillator accuracy characterization results for soldered parts*.<br>Updated *Table 58: TIMx characteristics*.<br>Updated *Table 16: STM32F302xB/STM32F302xC pin definitions* adding note for I/Os featuring an analog output function (DAC_OUT,OPAMP_OUT).<br>Updated *Table 68: ADC characteristics* adding IDDA & IREF consumptions.<br>Added *Figure 32: ADC typical current consumption on VDDA pin* and *Figure 33: ADC typical current consumption on VREF+ pin*.<br>Added *Section 3.8: Interconnect matrix*.<br>Updated *Figure 5: Clock tree*.<br>Added note after *Table 32: Typical and maximum VDD consumption in Stop and Standby modes*.<br>Updated *Section : In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.* with new LQFP100, LQFP64, LQFP48 package marking.<br>Updated *Table 16: STM32F302xB/STM32F302xC pin definitions* and alternate functions tables replacing usart_rts by usart_rts_de. |
| 29-Jan-2015 | 10 | Updated *Section 6.3.20: Comparator characteristics* modifying ts_sc characteristics in *Table 76* and adding *Figure 37: Maximum VREFINT scaler startup time from power down*.<br>Updated $I_{DD}$ data in *Table 42: HSE oscillator characteristics*. |

**Table 88. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 17-Apr-2015 | 11 | Updated *Section 7: Package information*: with new package information structure adding 1 sub paragraph for each package.<br>Updated *Figure 41: LQFP100 – 14 x 14 mm, low-profile quad flat package top view example* removing gate mark.<br>Added note for all packages about the device marking orientation: “the following figure gives an example of topside marking orientation versus pin 1 identifier location”.<br>Updated *Table 82: LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data*. |
| 11-Dec-2015 | 12 | Added WLCSP100:<br>– Updated cover page.<br>– Updated *Table 2: STM32F303xB/STM32F303xC family device features and peripheral counts*.<br>– Added *Figure 7: STM32F303xB/STM32F303xC WLCSP100 pinout*.<br>– Updated *Table 13: STM32F303xB/STM32F303xC pin definitions*.<br>– Updated *Table 24: General operating conditions*.<br>– Added *Section 7.4: WLCSP100 - 0.4 mm pitch wafer level chip scale package information*.<br>– Updated *Table 86: Package thermal characteristics*.<br>– Updated *Table 87: Ordering information scheme*.<br>Updated *Figure 4*, *Figure 5*, *Figure 6*, *Table 13* and *Table 22* removing all VDD and VSS indexes.<br>Updated all the notes removing ‘not tested in production’.<br>Updated *Table 68: ADC characteristics* adding $V_{REF-}$ negative voltage reference.<br>Update *Table 21: Voltage characteristics* adding table note 4. |