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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303rct6

3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.12 Interrupts and events

3.12.1 Nested vectored interrupt controller (NVIC)

The STM32F303xB/STM32F303xC devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.1 Advanced timers (TIM1, TIM8)

The advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.17.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.17.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F303xB/STM32F303xC (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

  These are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.17.3 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F303xB/STM32F303xC pin definitions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
D6	1	-	-	PE2	I/O	FT	(1)	TRACECK, TIM3_CH1, TSC_G7_IO1, EVENTOUT	-
D7	2	-	-	PE3	I/O	FT	(1)	TRACED0, TIM3_CH2, TSC_G7_IO2, EVENTOUT	-
C8	3	-	-	PE4	I/O	FT	(1)	TRACED1, TIM3_CH3, TSC_G7_IO3, EVENTOUT	-
B9	4	-	-	PE5	I/O	FT	(1)	TRACED2, TIM3_CH4, TSC_G7_IO4, EVENTOUT	-
E7	5	-	-	PE6	I/O	FT	(1)	TRACED3, EVENTOUT	WKUP3, RTC_TAMP3
D8	6	1	1	V_{BAT}	S	-	-	Backup power supply	

1. Function availability depends on the chosen device.
   When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).

   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0316 reference manual.
3. The VREF+ functionality is available only on the 100 pin package. On the 64-pin and 48-pin packages, the VREF+ is internally connected to VDDA.
4. Fast ADC channel.
5. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 20. STM32F303xB/STM32F303xC memory map, peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0x5000 0400 - 0x5000 07FF	1 K	ADC3 - ADC4
	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	TIM8
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

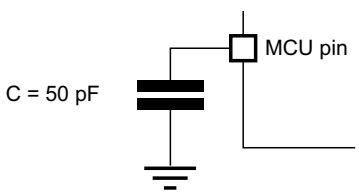


Figure 10. Pin input voltage

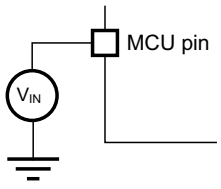
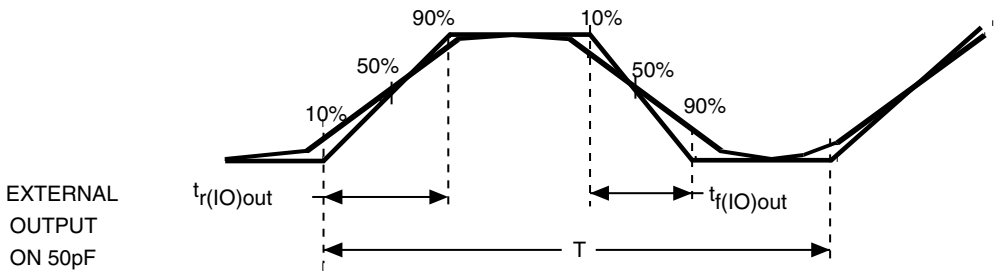


Table 27. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 23. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

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6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$+ 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}$+ 0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500(1)	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 64. I^2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master data: 16 bits, audio freq=48 kHz	1.496	1.503	MHz
		Slave	0	12.288	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 30 pF	-	8	ns
$t_{w(CKH)}$	I^2S clock high time	Master f_{PCLK}= 36 MHz, audio frequency = 48 kHz	331	-	
$t_{w(CKL)}$	I^2S clock low time		332	-	
$t_{v(WS)}$	WS valid time	Master mode	4	-	
$t_{h(WS)}$	WS hold time	Master mode	4	-	
$t_{su(WS)}$	WS setup time	Slave mode	4	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
Duty Cycle	I^2S slave input clock duty cycle	Slave mode	30	70	%
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	9	-	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	29	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	12	-	
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	3	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2	-	

1. Guaranteed by characterization results.

USB characteristics

Table 65. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 66. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F303xB/STM32F303xC USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers.

Figure 31. USB timings: definition of data signal rise and fall time

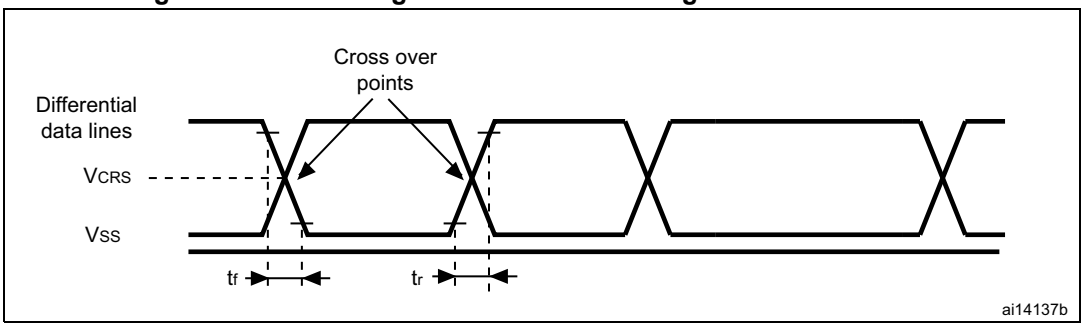


Figure 32. ADC typical current consumption on VDDA pin

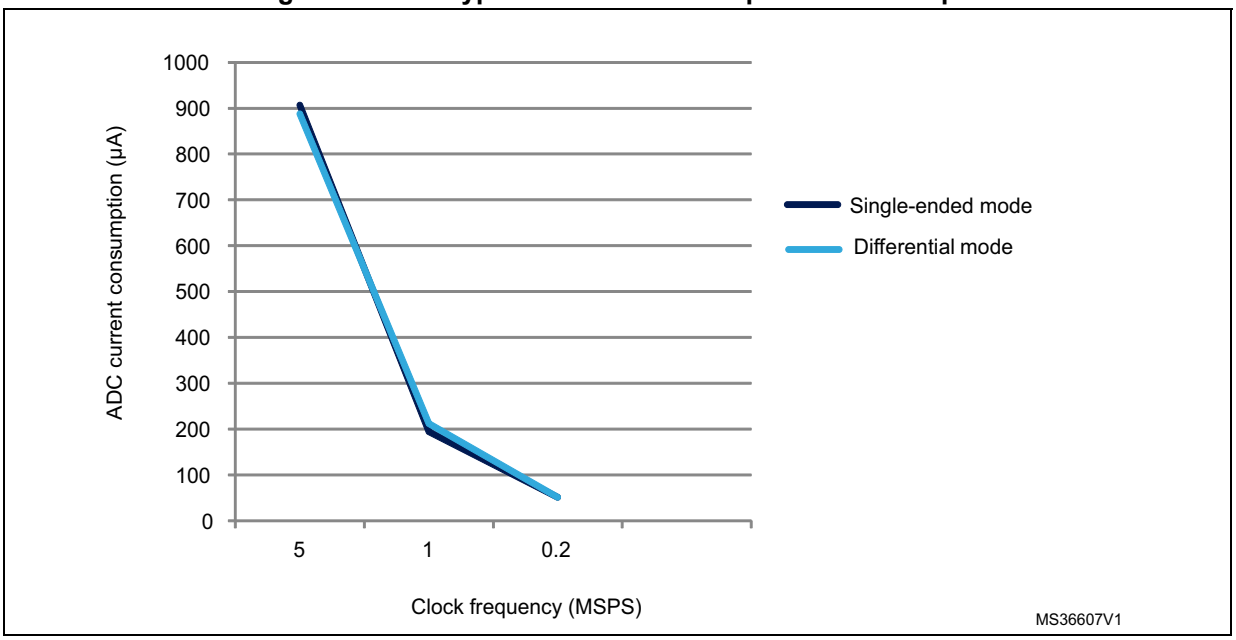


Figure 33. ADC typical current consumption on VREF+ pin

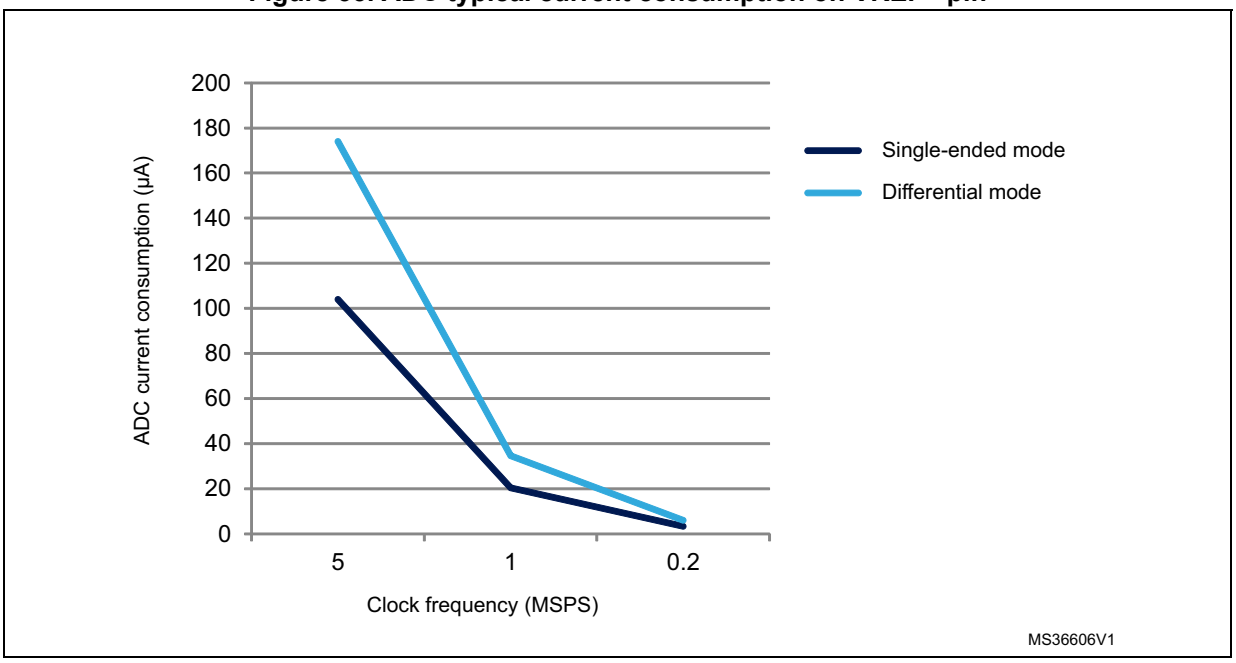


Table 71. ADC accuracy, 100-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2 V ≤ V_{DDA} , V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single Ended	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
ENOB (5)	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.2	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	

Table 71. ADC accuracy, 100-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
SINAD (5)	Signal-to-noise and distortion ratio	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 2 V ≤ V_{DDA}, V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	-74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 73. ADC accuracy, 64-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2.0 V ≤ V_{DDA} ≤ 3.6 V 64-pin package	Single ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB (5)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	

Figure 34. ADC accuracy characteristics

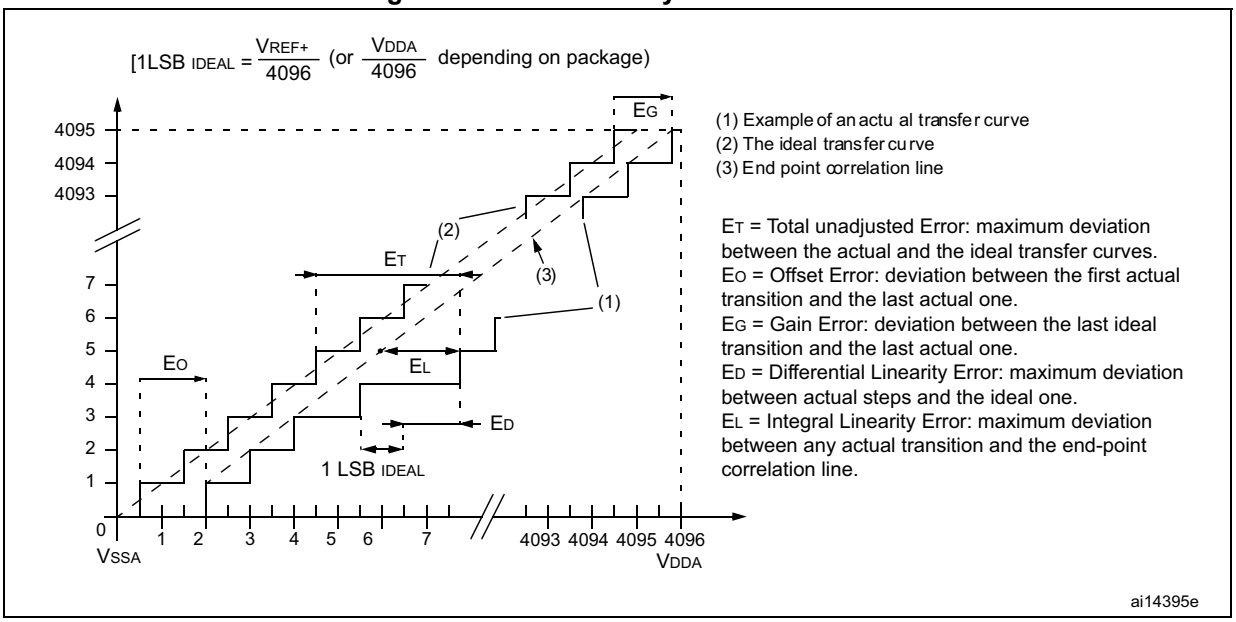
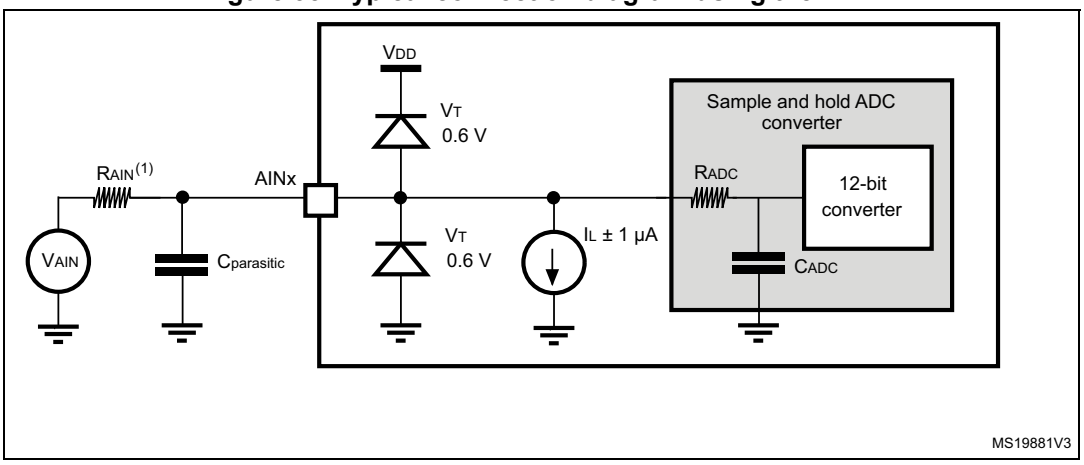


Figure 35. Typical connection diagram using the ADC



1. Refer to *Table 68* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 11*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.23 V_{BAT} monitoring characteristics

Table 80. V_{BAT} monitoring characteristics

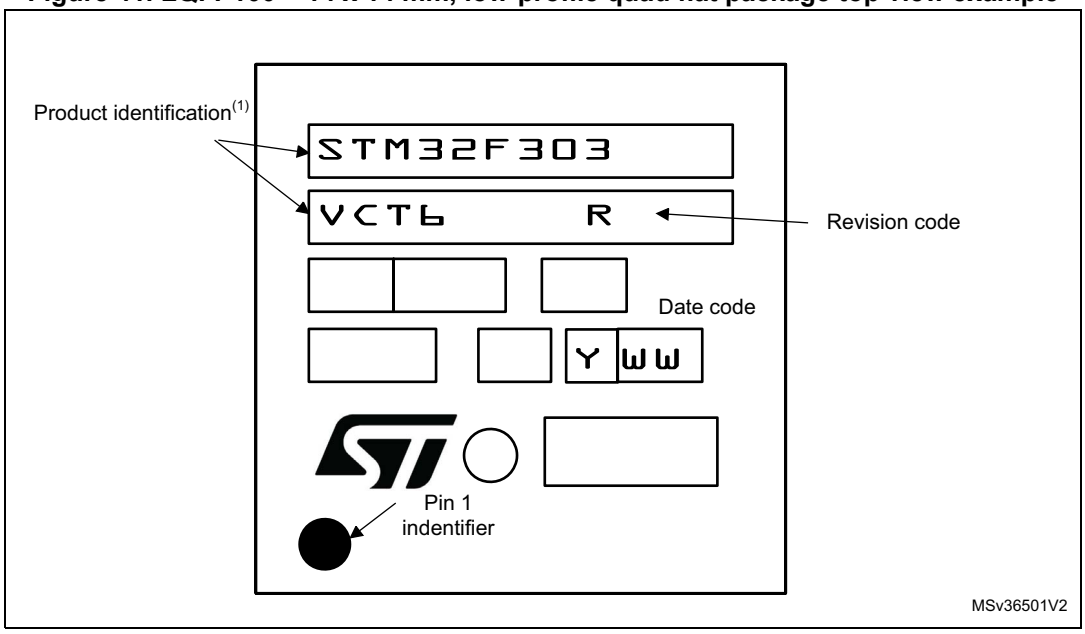
Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 41. LQFP100 – 14 x 14 mm, low-profile quad flat package top view example

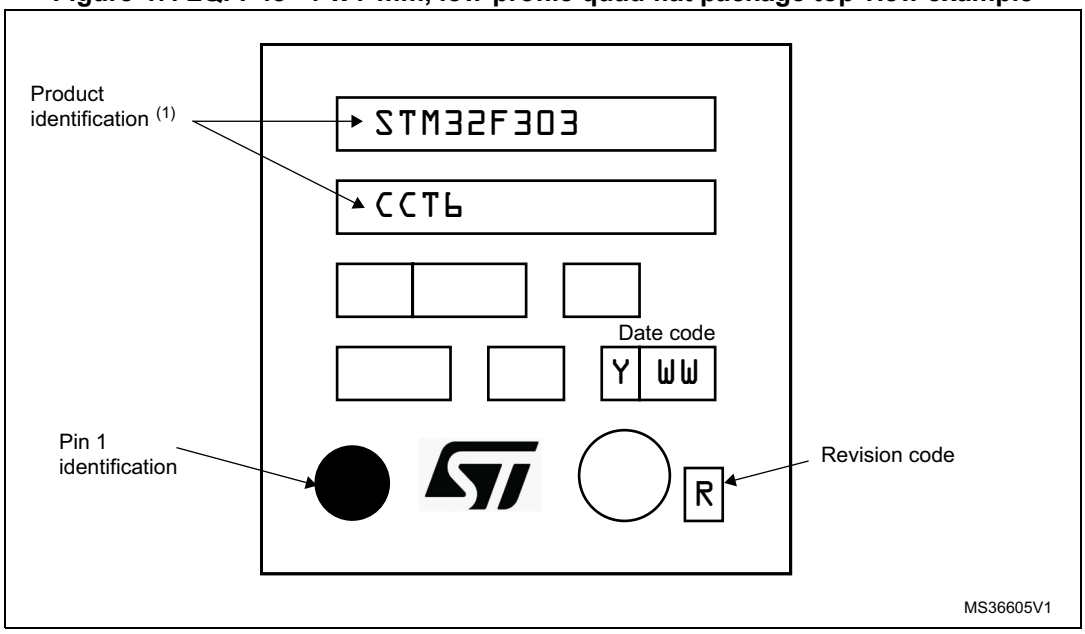


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 47. LQFP48 - 7 x 7 mm, low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 70 + 28.8 = 98.8 mW

Thus: P_{Dmax} = 98.8 mW

Using the values obtained in *Table 86* T_{Jmax} is calculated as follows:

– For LQFP100, 41°C/W

T_{Jmax} = 115 °C + (41°C/W × 98.8 mW) = 115 °C + 4.05 °C = 119.05 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*).

8 Ordering information

Table 87. Ordering information scheme

Example: STM32 F 303 R B T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

303 = STM32F303xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.