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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303rct7

Table 2. STM32F303xB/STM32F303xC family device features and peripheral counts

Peripheral		STM32F303Cx		STM32F303Rx		STM32F303Vx	
Flash (Kbytes)		128	256	128	256	128	256
SRAM (Kbytes) on data bus		32	40	32	40	32	40
CCM (Core Coupled Memory) RAM (Kbytes)		8					
Timers	Advanced control	2 (16-bit)					
	General purpose	5 (16-bit) 1 (32-bit)					
	Basic	2 (16-bit)					
PWM channels (all) (1)		31		33			
PWM channels (except complementary)		22		24			
Communication interfaces	SPI (I2S)(2)	3(2)					
	I^2C	2					
	USART	3					
	UART	0		2			
	CAN	1					
	USB	1					
GPIOs	Normal I/Os (TC, TTa)	20		27		45 in LQFP100 37 in WLCSP100	
	5-volt tolerant I/Os (FT, FTf)	17		25		42 in LQFP100 40 in WLCSP100	
DMA channels		12					
Capacitive sensing channels		17		18		24	
12-bit ADCs		4					
Number of channels		15		22		39 in LQFP100 32 in WLCSP100	
12-bit DAC channels		2					
Analog comparator		7					
Operational amplifiers		4					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP48		LQFP64		LQFP100 WLCSP100	

1. This total number considers also the PWMs generated on the complementary output channels
2. The SPI interfaces can work in an exclusive way in either the SPI mode or the I^2S audio mode.

3.4 Embedded SRAM

STM32F303xB/STM32F303xC devices feature up to 48 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz (when running code from the CCM (Core Coupled Memory) RAM).

- 8 Kbytes of CCM RAM mapped on both instruction and data bus, used to execute critical routines or to access data (parity check on all of CCM RAM).
- 40 Kbytes of SRAM mapped on the data bus (parity check on first 16 Kbytes of SRAM).

3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

Table 4. STM32F303xB/STM32F303xC peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx PVD GPIO	TIM1, TIM8, TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, please refer to the corresponding sections in the reference manual (RM0316).

3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.17.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter.It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stopand Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

3.22 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI1, SPI2 and SPI3.

Table 9. STM32F303xB/STM32F303xC SPI/I2S implementation

SPI features(1)	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	-	X	X
TI mode	X	X	X

1. X = supported.

3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Universal serial bus (USB)

The STM32F303xB/STM32F303xC devices embed an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator). The USB has a dedicated 512-bytes SRAM memory for data transmission and reception.

Figure 5. STM32F303xB/STM32F303xC LQFP64 pinout

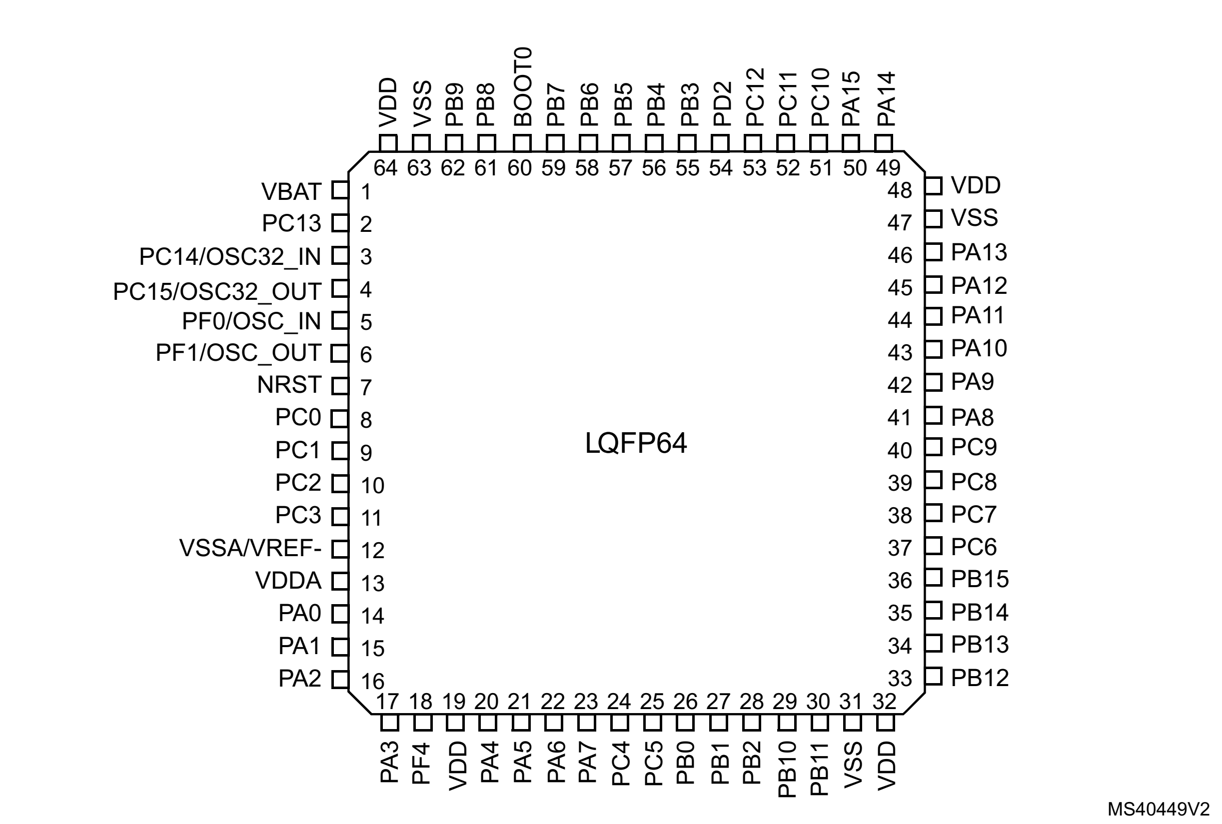


Figure 6. STM32F303xB/STM32F303xC LQFP100 pinout

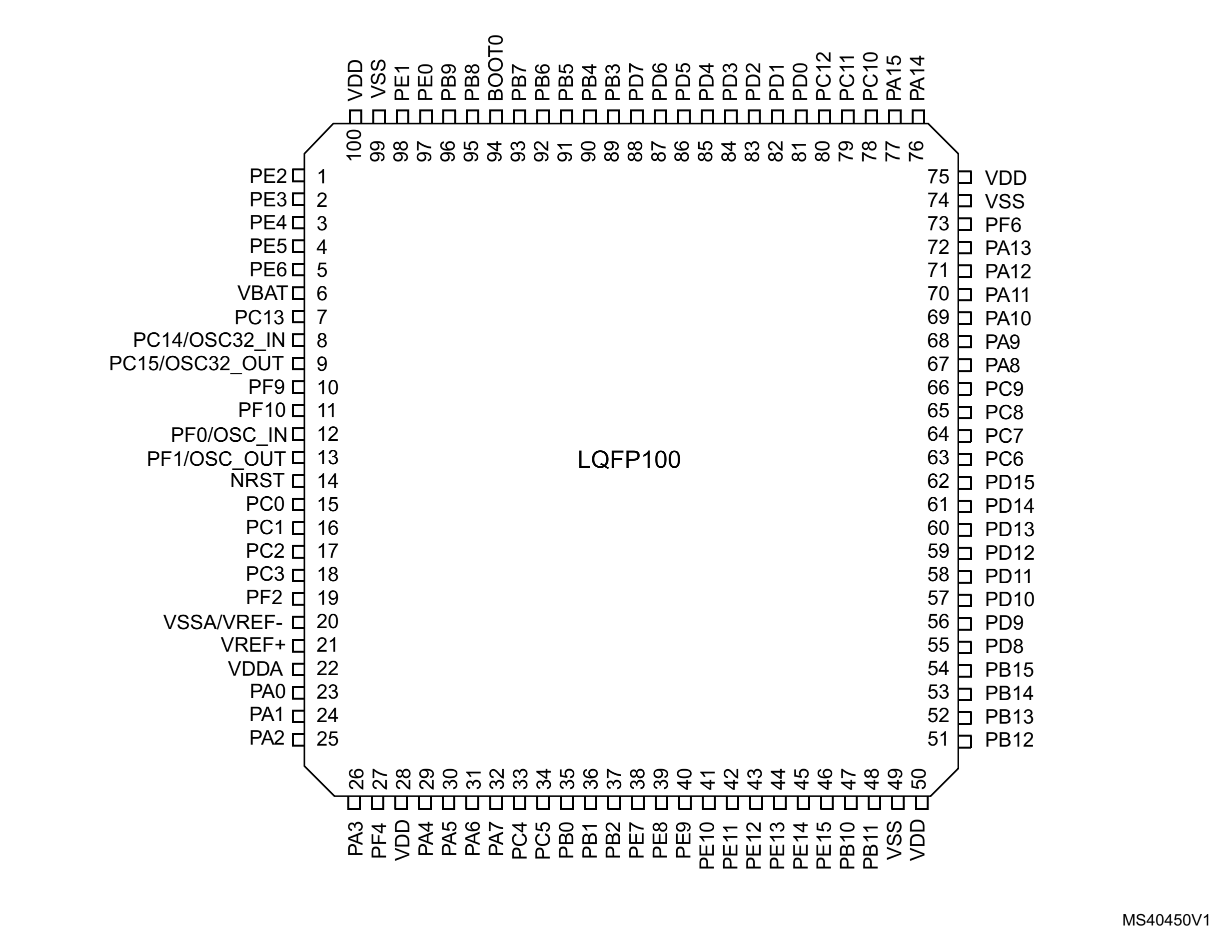


Figure 7. STM32F303xB/STM32F303xC WLCSP100 pinout

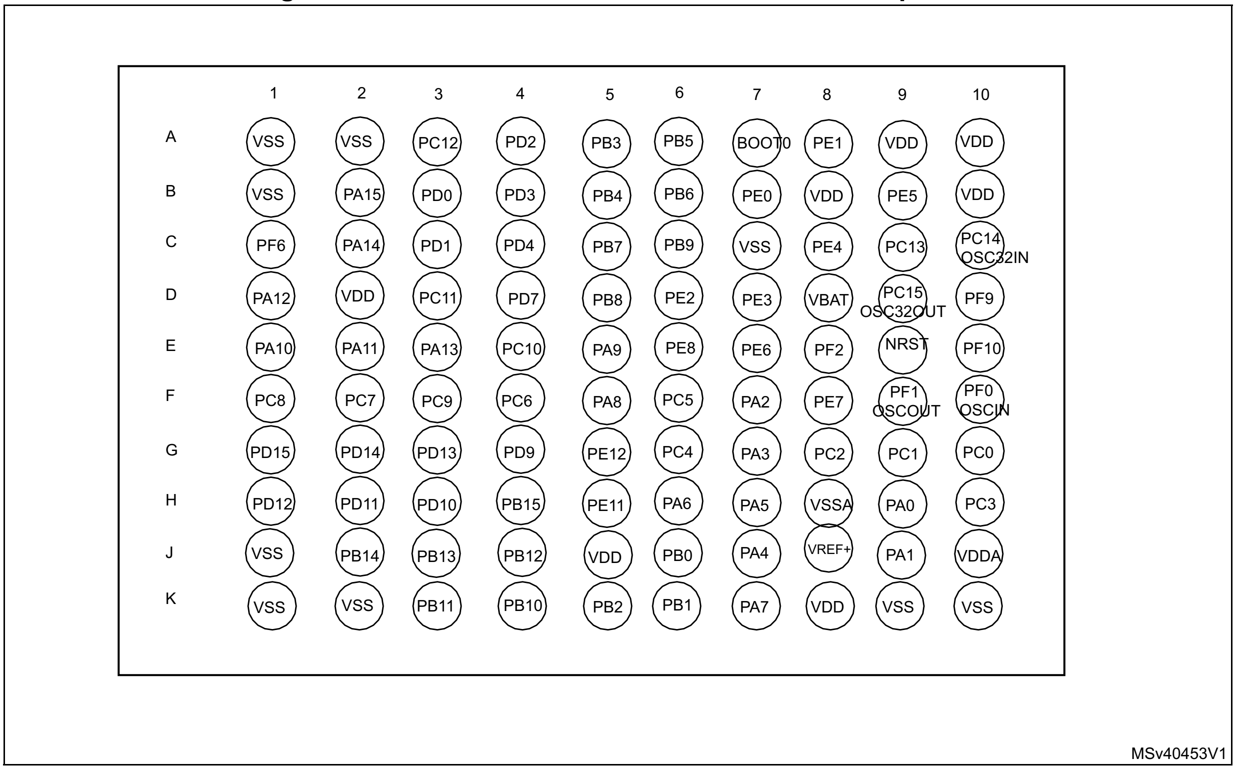


Table 15. Alternate functions for port B (continued)

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB13	-	-	-	TSC_ G6_IO3	-	SPI2_SCK, I2S2_CK	TIM1_ CH1N	USART3_ CTS	-	-	-	-	EVENT OUT
PB14	-	TIM15_ CH1	-	TSC_ G6_IO4	-	SPI2_MISO, I2S2ext_SD	TIM1_ CH2N	USART3_ RTS_DE	-	-	-	-	EVENT OUT
PB15	RTC_ REFIN	TIM15_ CH2	TIM15_ CH1N	-	TIM1_ CH3N	SPI2_MOSI, I2S2_SD	-	-	-	-	-	-	EVENT OUT

Table 17. Alternate functions for port D

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	-	-	-	-	-	CAN_RX
PD1	EVENTOUT	-	-	TIM8_CH4	-	TIM8_BKIN2	CAN_TX
PD2	EVENTOUT	TIM3_ETR	-	TIM8_BKIN	UART5_RX	-	-
PD3	EVENTOUT	TIM2_CH1_ETR	-	-	-	-	USART2_CTS
PD4	EVENTOUT	TIM2_CH2	-	-	-	-	USART2_RTS_DE
PD5	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	EVENTOUT	TIM2_CH4	-	-	-	-	USART2_RX
PD7	EVENTOUT	TIM2_CH3	-	-	-	-	USART2_CK
PD8	EVENTOUT	-	-	-	-	-	USART3_TX
PD9	EVENTOUT	-	-	-	-	-	USART3_RX
PD10	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS_DE
PD13	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	SPI2_NSS	-

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 25* are derived from tests performed under the ambient temperature condition summarized in *Table 24*.

Table 25. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 26. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 35. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	61.3	28.0	mA
			64 MHz	54.8	25.4	
			48 MHz	41.9	19.3	
			32 MHz	28.5	13.3	
			24 MHz	21.8	10.4	
			16 MHz	14.9	7.2	
			8 MHz	7.7	3.9	
			4 MHz	4.5	2.5	
			2 MHz	2.8	1.7	
			1 MHz	1.9	1.3	
			500 kHz	1.4	1.1	
			125 kHz	1.1	0.9	
I_{DDA}(1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	240.3	239.5	µA
			64 MHz	210.9	210.3	
			48 MHz	155.8	155.6	
			32 MHz	105.7	105.6	
			24 MHz	82.1	82.0	
			16 MHz	58.8	58.8	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 52. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

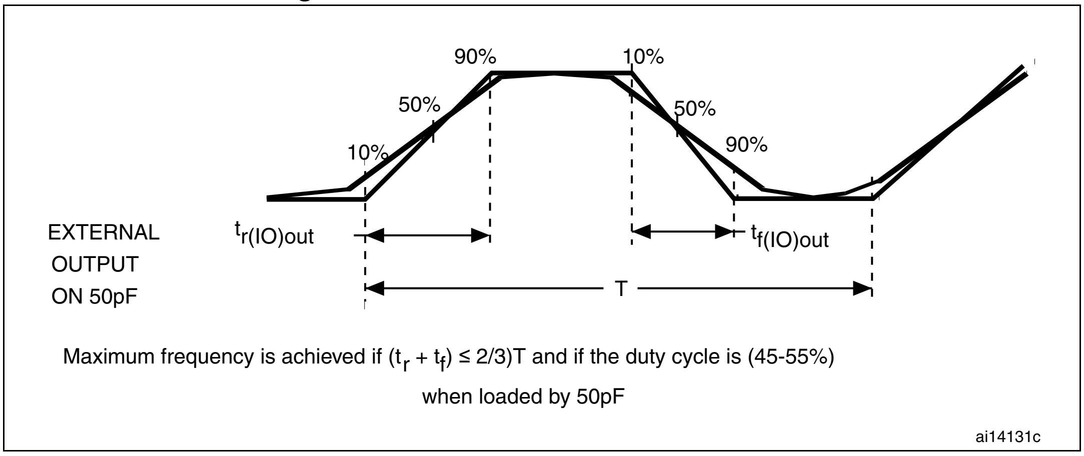
Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 53*.

Figure 23. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$+ 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}$+ 0.398(1)	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500(1)	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

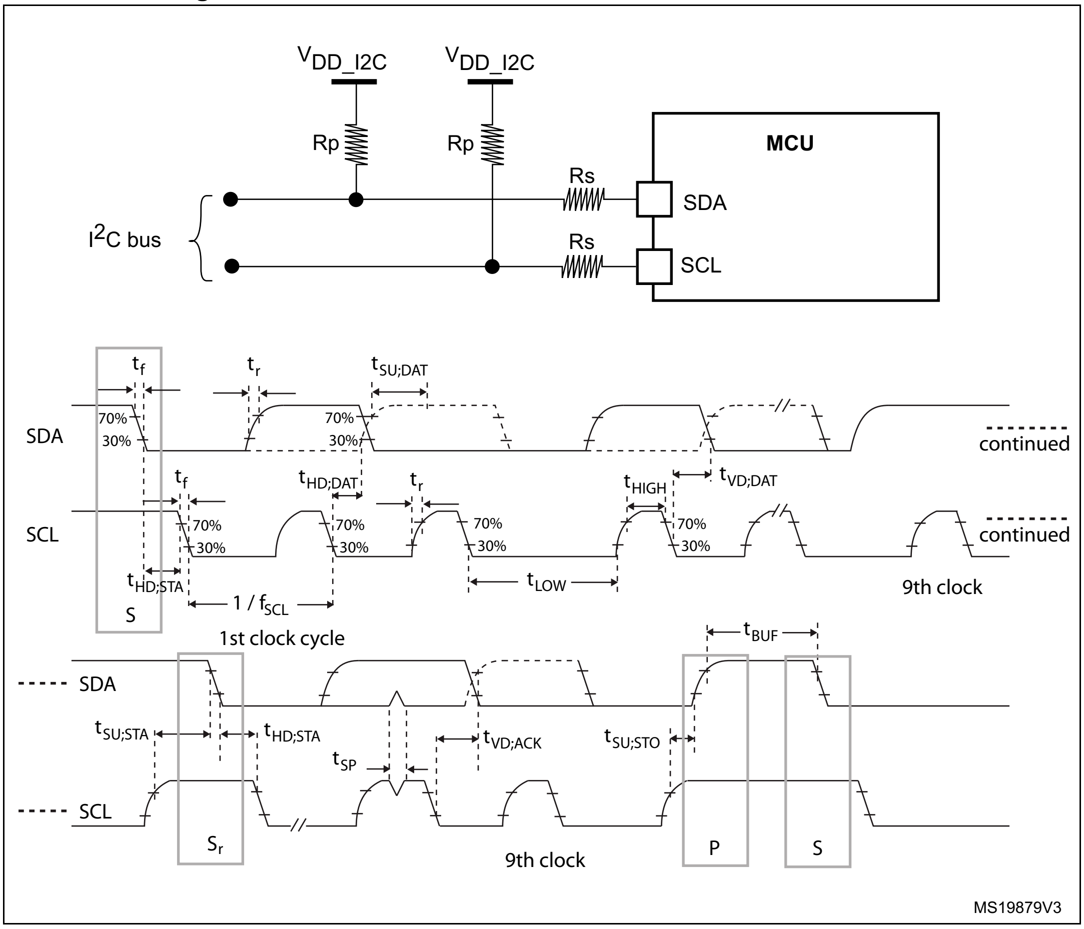
1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to the RM0316 reference manual).
2. The maximum tHD;DAT could be 3.45 μs, 0.9 μs and 0.45 μs for standard mode, fast mode and fast mode plus, but must be less than the maximum of tVD;DAT or tVD;ACK by a transition time.
3. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

Table 62. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design.

Figure 25. I^{2}C bus AC waveforms and measurement circuit



1. Rs: Series protection resistors, Rp: Pull-up resistors, VDD_I2C: I2C bus supply.

Table 68. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S (1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN} (1)	External input impedance	-	-	-	100	kΩ
C_{ADC} (1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB} (1)	Power-up time	-	1			conversion cycle
t_{CAL} (1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr} (1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$ (1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$

Table 70. ADC accuracy - limited test conditions, 100-pin packages (1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-76	-76	
				Slow channel 4.8 Ms	-	-76	-76	
			Differential	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-80	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 73. ADC accuracy, 64-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
SNR(5)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, $2\ V \leq V_{DDA} \leq 3.6\ V$ 64-pin package	Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 74. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS $2.4\ V \leq V_{DDA} = V_{REF+} \leq 3.6\ V$ Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.14: I/O port characteristics* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

Figure 34. ADC accuracy characteristics

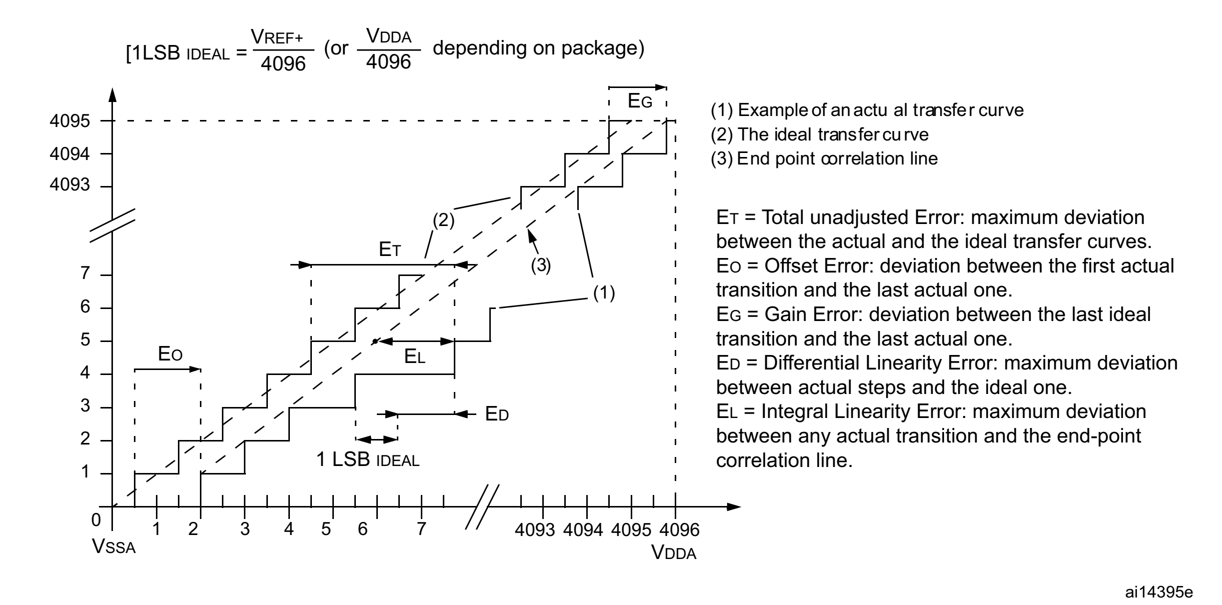
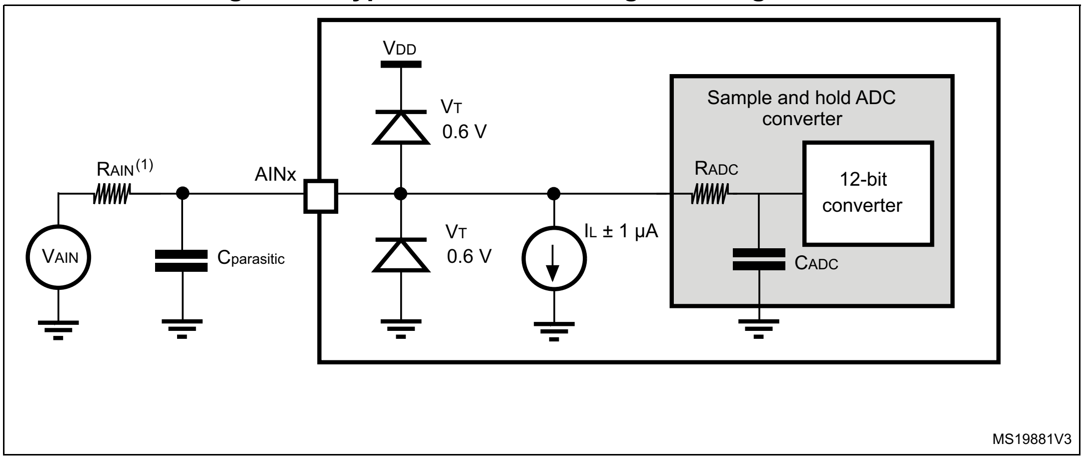


Figure 35. Typical connection diagram using the ADC



1. Refer to *Table 68* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

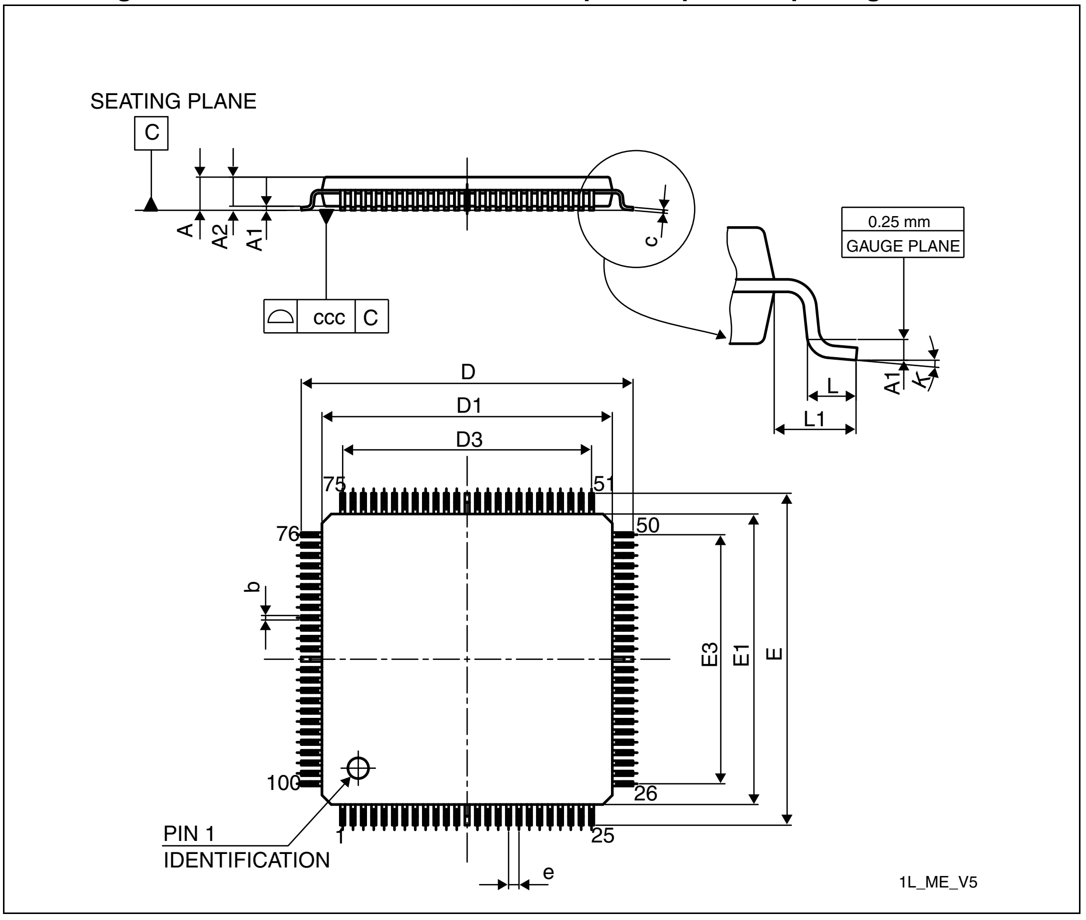
Power supply decoupling should be performed as shown in *Figure 11*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 – 14 x 14 mm, low-profile quad flat package information

Figure 39. LQFP100 – 14 x 14 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 81. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.0059