STMicroelectronics - STM32F303VBT6 Datasheet

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	87
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vbt6

Contents

3.7 Power management

3.7.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} differs from one analog peripheral to another. *Table 3* provides the summary of the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Table 3. External analog supply values for analog peripherals

Analog peripheral	Minimum V_{DDA} supply	Maximum V_{DDA} supply
ADC / COMP	2.0 V	3.6 V
DAC / OPAMP	2.4 V	3.6V

3.7.2 Power supply supervision

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, VPOR/PDR, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.13.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.13.4 OPAMP reference voltage (VREFOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17, VREFOPAMP3 connected to ADC3 channel 17, VREFOPAMP4 connected to ADC4 channel 17.

3.14 Digital-to-analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Two DAC output channels
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability (for each channel)
- External triggers for conversion

3.15 Operational amplifier (OPAMP)

The STM32F303xB/STM32F303xC embeds four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

Table 10. Capacitive sensing GPIOs available on STM32F303xB/STM32F303xC devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 11. No. of capacitive sensing channels available on STM32F303xB/STM32F303xC devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F303Vx	STM32F303Rx	STM32F303Cx
G1	3	3	3
G2	3	3	3
G3	3	3	2
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	24	18	17

Table 15. Alternate functions for port B

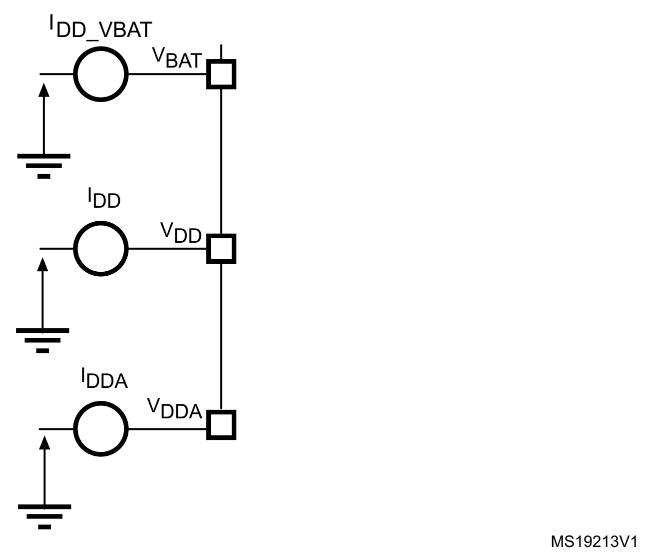
Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB0	-	-	TIM3_ CH3	TSC_ G3_IO2	TIM8_ CH2N	-	TIM1_CH2N	-	-	-	-	-	EVENT OUT
PB1	-	-	TIM3_ CH4	TSC_ G3_IO3	TIM8_ CH3N	-	TIM1_CH3N	-	COMP4_ OUT	-	-	-	EVENT OUT
PB2	-	-	-	TSC_ G3_IO4	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO-TRACES WO	TIM2_ CH2	TIM4_ ETR	TSC_ G5_IO1	TIM8_ CH1N	SPI1_ SCK	SPI3_SCK, I2S3_CK	USART2_ TX	-	-	TIM3_ ETR	-	EVENT OUT
PB4	NJTRST	TIM16_ CH1	TIM3_ CH1	TSC_ G5_IO2	TIM8_ CH2N	SPI1_ MISO	SPI3_MISO, I2S3ext_SD	USART2_ RX	-	-	TIM17_ BKIN	-	EVENT OUT
PB5	-	TIM16_ BKIN	TIM3_ CH2	TIM8_ CH3N	I2C1_ SMBA	SPI1_ MOSI	SPI3_MOSI, I2S3_SD	USART2_ CK	-	-	TIM17_ CH1	-	EVENT OUT
PB6	-	TIM16_ CH1N	TIM4_ CH1	TSC_ G5_IO3	I2C1_SCL	TIM8_CH1	TIM8_ ETR	USART1_ TX	-	-	TIM8_ BKIN2	-	EVENT OUT
PB7	-	TIM17_ CH1N	TIM4_ CH2	TSC_ G5_IO4	I2C1_ SDA	TIM8_ BKIN	-	USART1_ RX	-	-	TIM3_ CH4	-	EVENT OUT
PB8	-	TIM16_ CH1	TIM4_ CH3	TSC_ SYNC	I2C1_SCL	-	-	-	COMP1_ OUT	CAN_RX	TIM8_ CH2	TIM1_ BKIN	EVENT OUT
PB9	-	TIM17_ CH1	TIM4_ CH4		I2C1_ SDA	-	IR_OUT	-	COMP2_ OUT	CAN_TX	TIM8_ CH3	-	EVENT OUT
PB10	-	TIM2_ CH3	-	TSC_ SYNC	-	-	-	USART3_ TX	-	-	-	-	EVENT OUT
PB11	-	TIM2_ CH4	-	TSC_ G6_IO1	-	-	-	USART3_ RX	-	-	-	-	EVENT OUT
PB12	-	-	-	TSC_ G6_IO2	I2C2_ SMBA	SPI2_NSS, I2S2_WS	TIM1_ BKIN	USART3_ CK	-	-	-	-	EVENT OUT

Table 17. Alternate functions for port D

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	-	-	-	-	-	CAN_RX
PD1	EVENTOUT	-	-	TIM8_CH4	-	TIM8_BKIN2	CAN_TX
PD2	EVENTOUT	TIM3_ETR	-	TIM8_BKIN	UART5_RX	-	-
PD3	EVENTOUT	TIM2_CH1_ETR	-	-	-	-	USART2_CTS
PD4	EVENTOUT	TIM2_CH2	-	-	-	-	USART2_RTS_DE
PD5	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	EVENTOUT	TIM2_CH4	-	-	-	-	USART2_RX
PD7	EVENTOUT	TIM2_CH3	-	-	-	-	USART2_CK
PD8	EVENTOUT	-	-	-	-	-	USART3_TX
PD9	EVENTOUT	-	-	-	-	-	USART3_RX
PD10	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS_DE
PD13	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	SPI2_NSS	-

6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics*, and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
V_{REF+}–V_{DDA}(2)	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
V_{IN}(3)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins(4)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.

Table 32. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	20.05	20.33	20.42	20.50	20.67	20.80	44.2(2)	350	735(2)	µA
		Regulator in low-power mode, all oscillators OFF	7.63	7.77	7.90	8.07	8.17	8.33	30.6(2)	335	720(2)	
	Supply current in Standby mode	LSI ON and IWDG ON	0.80	0.96	1.09	1.23	1.37	1.51	-	-	-	
		LSI OFF and IWDG OFF	0.60	0.74	0.83	0.93	1.02	1.11	5.0(2)	7.8	13.3(2)	

1. Guaranteed by characterization results unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 33. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	µA
			Regulator in low-power mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	
	Supply current in Standby mode		LSI ON and IWDG ON	2.22	2.42	2.59	2.78	3.0	3.24	-	-	-	
			LSI OFF and IWDG OFF	1.69	1.82	1.94	2.08	2.23	2.40	3.5	5.4	9.2	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.44	1.52	1.60	1.71	1.84	1.98	-	-	-	
			LSI OFF and IWDG OFF	0.93	0.95	0.98	1.02	1.08	1.15	-	-	-	

1. Guaranteed by characterization results.

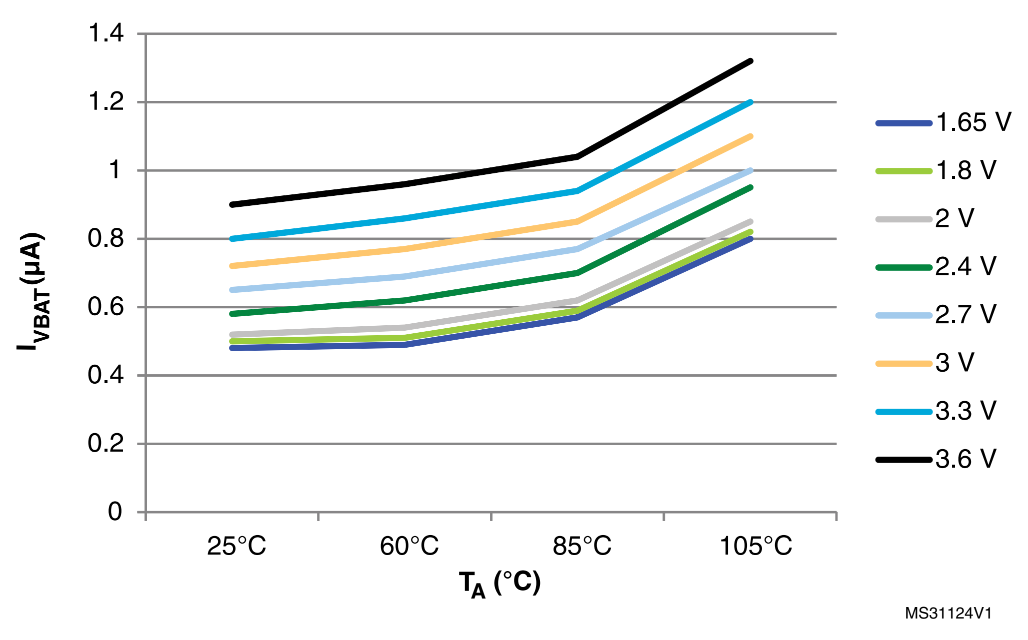
The total consumption is the sum of IDD and IDDA.

Table 34. Typical and maximum current consumption from V_{BAT} supply

Symbol	Parameter	Conditions (1)	Typ @V_{BAT}								Max @V_{BAT} = 3.6 V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 13. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = ’00’)



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 35. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	61.3	28.0	mA
			64 MHz	54.8	25.4	
			48 MHz	41.9	19.3	
			32 MHz	28.5	13.3	
			24 MHz	21.8	10.4	
			16 MHz	14.9	7.2	
			8 MHz	7.7	3.9	
			4 MHz	4.5	2.5	
			2 MHz	2.8	1.7	
			1 MHz	1.9	1.3	
			500 kHz	1.4	1.1	
			125 kHz	1.1	0.9	
I_{DDA}(1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	240.3	239.5	µA
			64 MHz	210.9	210.3	
			48 MHz	155.8	155.6	
			32 MHz	105.7	105.6	
			24 MHz	82.1	82.0	
			16 MHz	58.8	58.8	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 38. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
TIM6	9.7	µA/MHz
TIM7	12.1	
WWDG	6.4	
SPI2	40.4	
SPI3	40.0	
USART2	41.9	
USART3	40.2	
UART4	36.5	
UART5	30.8	
I2C1	10.5	
I2C2	10.4	
USB	26.2	
CAN	33.4	
PWR	5.7	
DAC	15.4	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 49*. They are based on the EMS levels and classes defined in the application note AN1709.

Table 49. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 50. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	**7**	dBµV
			30 to 130 MHz	**20**	
			130 MHz to 1GHz	**27**	
			SAE EMI Level	**4**	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114, ANSI/ESD STM5.3.1 standard.

Table 51. ESD absolute maximum ratings

Symbol	Ratings	Conditions		Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	WLCSP100 package	3	250	
			Packages except WLCSP100	4	500	

1. Guaranteed by characterization results.

Figure 26. SPI timing diagram - slave mode and CPHA = 0

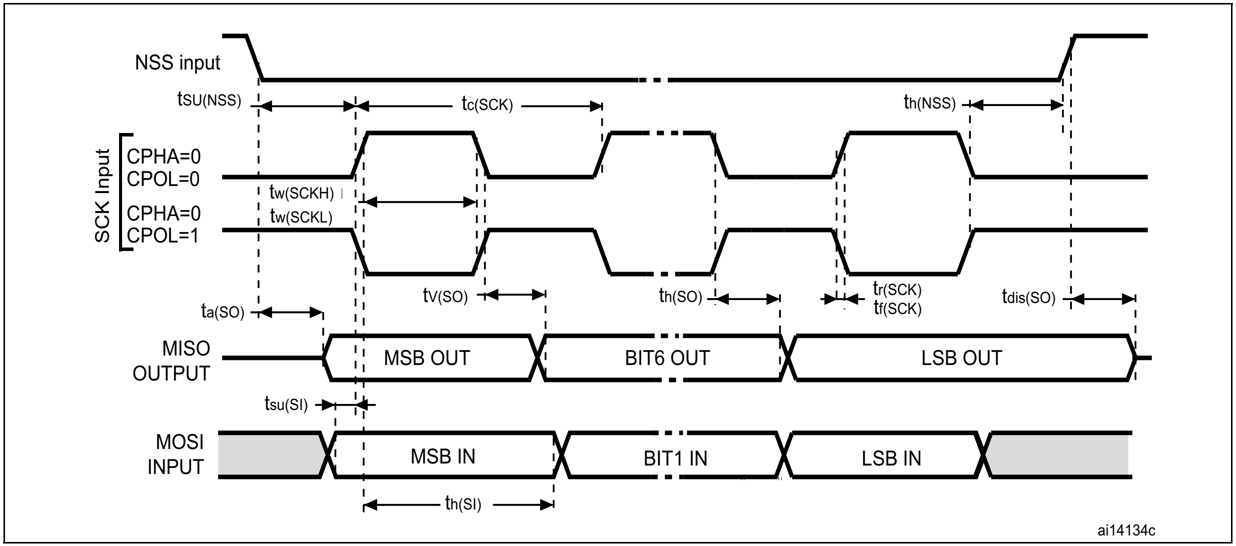
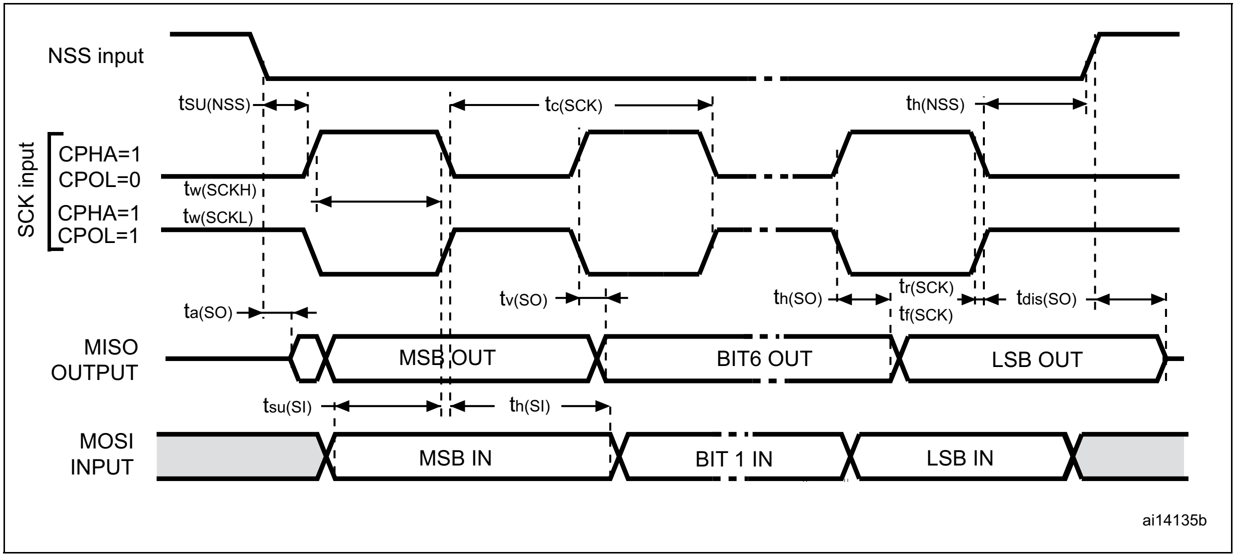


Figure 27. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in *Table 68* to *Table 70* are guaranteed by design, with conditions summarized in *Table 24*.

Table 68. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	2	-	3.6	V
I_{DDA}	ADC current consumption on VDDA pin (see *Figure 32*)	Single-ended mode, 5 MSPS	-	907	1033.0	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	0	-	
I_{REF}	ADC current consumption on VREF+ pin (see *Figure 33*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	

Table 73. ADC accuracy, 64-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
SNR(5)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, $2\ V \leq V_{DDA} \leq 3.6\ V$ 64-pin package	Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 74. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS $2.4\ V \leq V_{DDA} = V_{REF+} \leq 3.6\ V$ Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

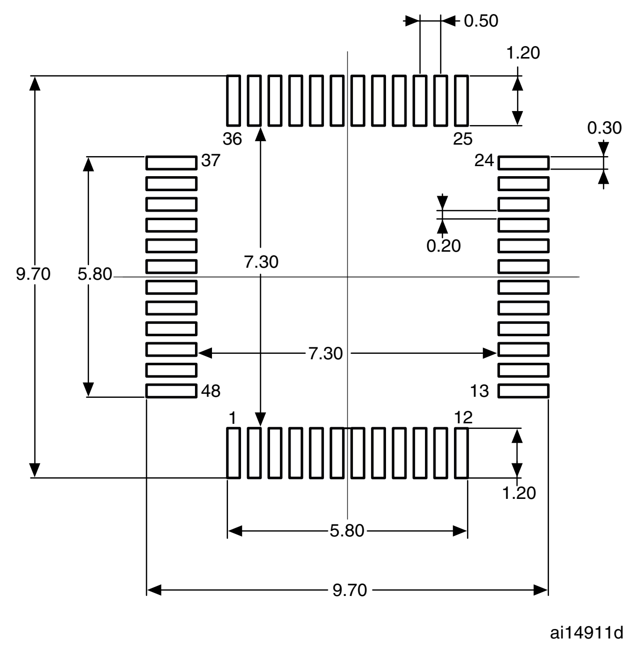
1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.14: I/O port characteristics* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3	-	5.50	-	-	0.2165	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP48 - 7 x 7 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

Figure 49. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint

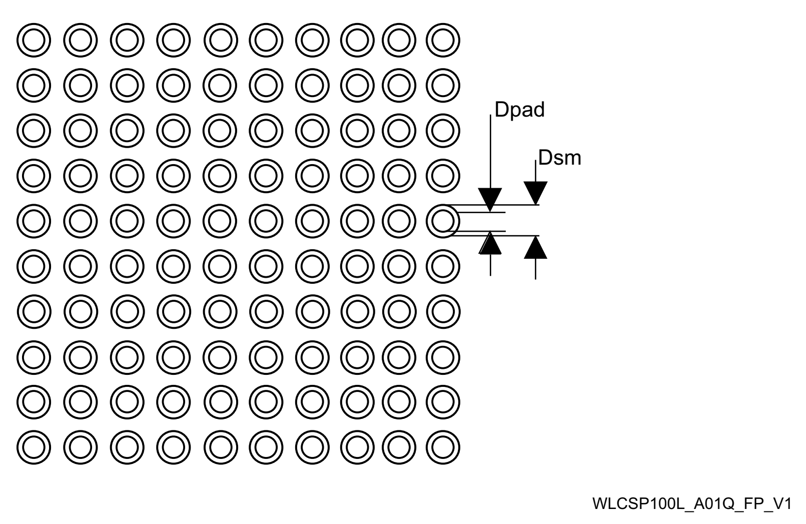


Table 85. WLCSP100 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

Table 88. Document revision history (continued)

Date	Revision	Changes
06-May-2016	13	Updated *Table 43: LSE oscillator characteristics (fLSE = 32.768 kHz)* LSEDRV[1:0] bits. Updated *Table 28: Embedded internal reference voltage* V_{REFINT} internal reference voltage (min and typ values). Updated *Figure 5: STM32F303xB/STM32F303xC LQFP64 pinout* replacing VSS by PF4. Updated *Table 51: ESD absolute maximum ratings* ESD CDM at class 3 and 4 including WLCSP100 package information. Updated *Table 13: STM32F303xB/STM32F303xC pin definitions*: – Adding ‘digital power supply’ in the Pin function column at the line corresponding to K8/28/19 pins. – Adding VSS digital ground line with WLCSP100 K9 and K10 pins connected. – Replacing in VDD line for WLCSP100: ‘A10, B10’ by ‘A9, A10, B10, B8’. Updated *Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port*. Updated *Table 77: Operational amplifier characteristics* high saturation and low saturation voltages. Updated *Table 13: STM32F303xB/STM32F303xC pin definitions* adding note ‘Fast ADC channel’ for ADCx_IN1..5. Updated *Table 75: DAC characteristics* resistive load. Updated *Table 68: ADC characteristics* adding CMIR parameter and modifying tSTAB parameter characteristics.