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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	87
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vbt6tr

3.7 Power management

3.7.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} differs from one analog peripheral to another. *Table 3* provides the summary of the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Table 3. External analog supply values for analog peripherals

Analog peripheral	Minimum V_{DDA} supply	Maximum V_{DDA} supply
ADC / COMP	2.0 V	3.6 V
DAC / OPAMP	2.4 V	3.6V

3.7.2 Power supply supervision

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

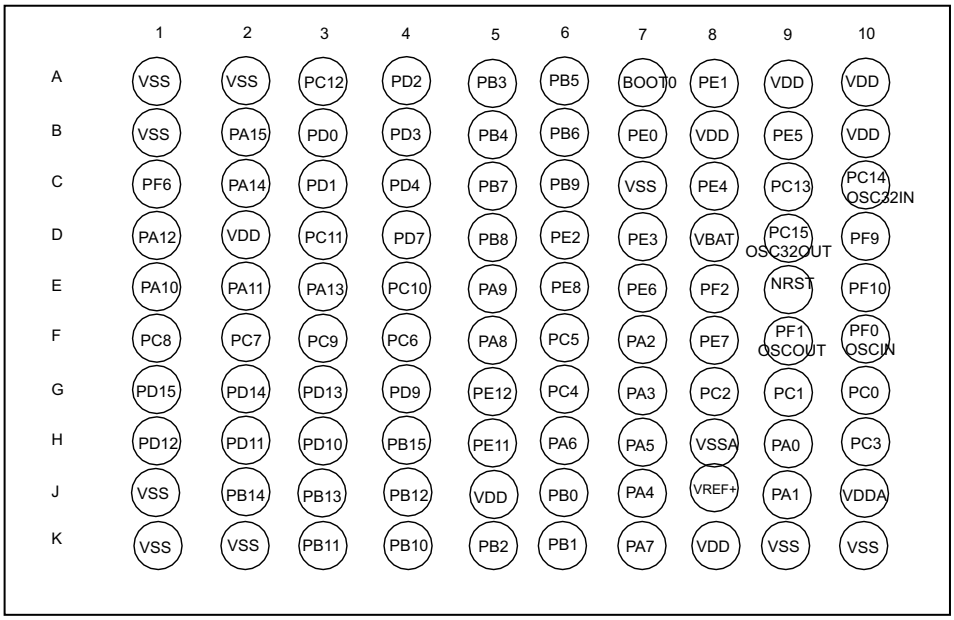
3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

Figure 7. STM32F303xB/STM32F303xC WLCSP100 pinout



MSv40453V1

Table 13. STM32F303xB/STM32F303xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
C9	7	2	2	PC13(2)	I/O	TC	-	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
C10	8	3	3	PC14(2) OSC32_IN (PC14)	I/O	TC	-	-	OSC32_IN
D9	9	4	4	PC15(2) OSC32_ OUT (PC15)	I/O	TC	-	-	OSC32_OUT
D10	10	-	-	PF9	I/O	FT	(1)	TIM15_CH1, SPI2_SCK, EVENTOUT	-
E10	11	-	-	PF10	I/O	FT	(1)	TIM15_CH2, SPI2_SCK, EVENTOUT	-
F10	12	5	5	PF0- OSC_IN (PF0)	I/O	FTf	-	TIM1_CH3N, I2C2_SDA,	OSC_IN
F9	13	6	6	PF1- OSC_OUT (PF1)	I/O	FTf	-	I2C2_SCL	OSC_OUT
E9	14	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
G10	15	8	-	PC0	I/O	TTa	(1)	EVENTOUT	ADC12_IN6, COMP7_INM
G9	16	9	-	PC1	I/O	TTa	(1)	EVENTOUT	ADC12_IN7, COMP7_INP
G8	17	10	-	PC2	I/O	TTa	(1)	COMP7_OUT, EVENTOUT	ADC12_IN8
H10	18	11	-	PC3	I/O	TTa	(1)	TIM1_BKIN2, EVENTOUT	ADC12_IN9
E8	19	-	-	PF2	I/O	TTa	(1)	EVENTOUT	ADC12_IN10
H8	20	12	8	VSSA/ VREF-	S	-	-	Analog ground/Negative reference voltage	
J8	21	-	-	VREF+(3)	S	-	-	Positive reference voltage	
J10	22	-	-	VDDA	S	-	-	Analog power supply	
-	-	13	9	VDDA/ VREF+	S	-	-	Analog power supply/Positive reference voltage	
H9	23	14	10	PA0	I/O	TTa	(4)	USART2_CTS, TIM2_CH1_ETR,TIM8_BKIN, TIM8_ETR,TSC_G1_IO1, COMP1_OUT, EVENTOUT	ADC1_IN1, COMP1_INM, RTC_ TAMP2, WKUP1, COMP7_INP

Table 13. STM32F303xB/STM32F303xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
B5	90	56	40	PB4	I/O	FT	-	SPI3_MISO, I2S3ext_SD, SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TIM8_CH2N, TSC_G5_IO2, NJTRST, EVENTOUT	-
A6	91	57	41	PB5	I/O	FT	-	SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM8_CH3N, TIM17_CH1, EVENTOUT	-
B6	92	58	42	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TIM4_CH1, TIM8_CH1,TSC_G5_IO3, TIM8_ETR, TIM8_BKIN2, EVENTOUT	-
C5	93	59	43	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM3_CH4, TIM4_CH2, TIM17_CH1N, TIM8_BKIN, TSC_G5_IO4, EVENTOUT	-
A7	94	60	44	BOOT0	I	B	-	Boot memory selection	
D5	95	61	45	PB8	I/O	FTf	-	I2C1_SCL, CAN_RX, TIM16_CH1, TIM4_CH3, TIM8_CH2, TIM1_BKIN, TSC_SYNC, COMP1_OUT, EVENTOUT	-
C6	96	62	46	PB9	I/O	FTf	-	I2C1_SDA, CAN_TX, TIM17_CH1, TIM4_CH4, TIM8_CH3, IR_OUT, COMP2_OUT, EVENTOUT	-
B7	97	-	-	PE0	I/O	FT	(1)	USART1_TX, TIM4_ETR, TIM16_CH1, EVENTOUT	-
A8	98	-	-	PE1	I/O	FT	(1)	USART1_RX, TIM17_CH1, EVENTOUT	-
C7	99	63	47	VSS	S	-	-	Ground	
A9, A10, B10, B8	100	64	48	VDD	S	-	-	Digital power supply	

1. Function availability depends on the chosen device.
   When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).

   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0316 reference manual.
3. The VREF+ functionality is available only on the 100 pin package. On the 64-pin and 48-pin packages, the VREF+ is internally connected to VDDA.
4. Fast ADC channel.
5. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 15. Alternate functions for port B

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB0	-	-	TIM3_ CH3	TSC_ G3_IO2	TIM8_ CH2N	-	TIM1_CH2N	-	-	-	-	-	EVENT OUT
PB1	-	-	TIM3_ CH4	TSC_ G3_IO3	TIM8_ CH3N	-	TIM1_CH3N	-	COMP4_ OUT	-	-	-	EVENT OUT
PB2	-	-	-	TSC_ G3_IO4	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO-TRACESWO	TIM2_ CH2	TIM4_ ETR	TSC_ G5_IO1	TIM8_ CH1N	SPI1_ SCK	SPI3_SCK, I2S3_CK	USART2_ TX	-	-	TIM3_ ETR	-	EVENT OUT
PB4	NJTRST	TIM16_ CH1	TIM3_ CH1	TSC_ G5_IO2	TIM8_ CH2N	SPI1_ MISO	SPI3_MISO, I2S3ext_SD	USART2_ RX	-	-	TIM17_ BKIN	-	EVENT OUT
PB5	-	TIM16_ BKIN	TIM3_ CH2	TIM8_ CH3N	I2C1_ SMBA	SPI1_ MOSI	SPI3_MOSI, I2S3_SD	USART2_ CK	-	-	TIM17_ CH1	-	EVENT OUT
PB6	-	TIM16_ CH1N	TIM4_ CH1	TSC_ G5_IO3	I2C1_SCL	TIM8_CH1	TIM8_ ETR	USART1_ TX	-	-	TIM8_ BKIN2	-	EVENT OUT
PB7	-	TIM17_ CH1N	TIM4_ CH2	TSC_ G5_IO4	I2C1_ SDA	TIM8_ BKIN	-	USART1_ RX	-	-	TIM3_ CH4	-	EVENT OUT
PB8	-	TIM16_ CH1	TIM4_ CH3	TSC_ SYNC	I2C1_SCL	-	-	-	COMP1_ OUT	CAN_RX	TIM8_ CH2	TIM1_ BKIN	EVENT OUT
PB9	-	TIM17_ CH1	TIM4_ CH4		I2C1_ SDA	-	IR_OUT	-	COMP2_ OUT	CAN_TX	TIM8_ CH3	-	EVENT OUT
PB10	-	TIM2_ CH3	-	TSC_ SYNC	-	-	-	USART3_ TX	-	-	-	-	EVENT OUT
PB11	-	TIM2_ CH4	-	TSC_ G6_IO1	-	-	-	USART3_ RX	-	-	-	-	EVENT OUT
PB12	-	-	-	TSC_ G6_IO2	I2C2_ SMBA	SPI2_NSS, I2S2_WS	TIM1_ BKIN	USART3_ CK	-	-	-	-	EVENT OUT

Table 20. STM32F303xB/STM32F303xC memory map, peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0x5000 0400 - 0x5000 07FF	1 K	ADC3 - ADC4
	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	TIM8
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP

Table 36. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	44.1	7.0	mA
			64 MHz	39.7	6.3	
			48 MHz	30.3	4.9	
			32 MHz	20.5	3.5	
			24 MHz	15.4	2.8	
			16 MHz	10.6	2.0	
			8 MHz	5.4	1.1	
			4 MHz	3.2	1.0	
			2 MHz	2.1	0.9	
			1 MHz	1.5	0.8	
			500 kHz	1.2	0.8	
			125 kHz	1.0	0.8	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.7	238.5	µA
			64 MHz	210.5	209.6	
			48 MHz	155.0	155.6	
			32 MHz	105.3	105.2	
			24 MHz	81.9	81.8	
			16 MHz	58.7	58.6	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

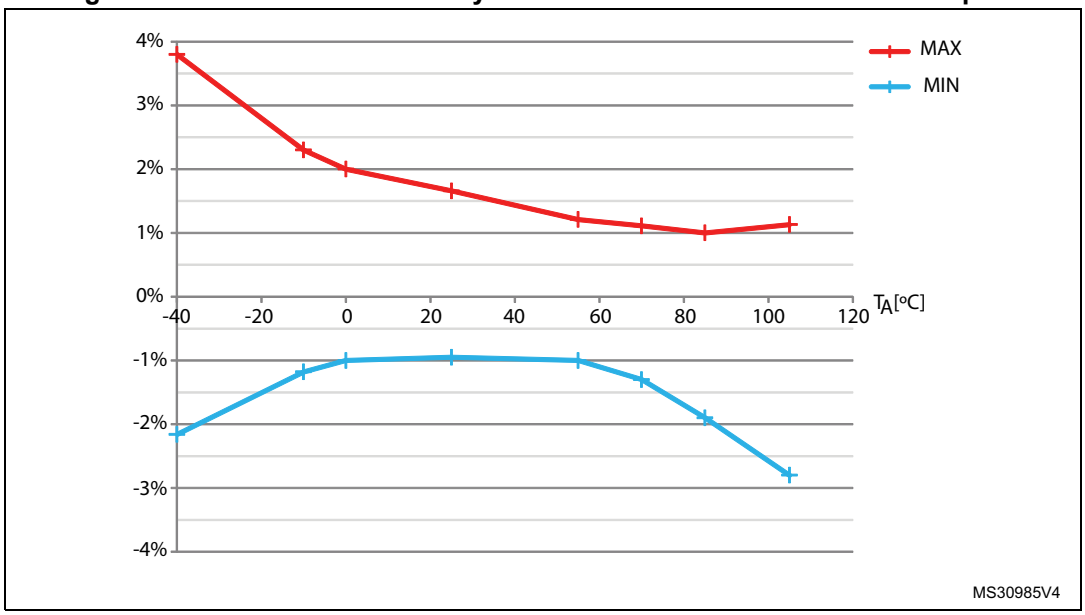
1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 38. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
TIM6	9.7	µA/MHz
TIM7	12.1	
WWDG	6.4	
SPI2	40.4	
SPI3	40.0	
USART2	41.9	
USART3	40.2	
UART4	36.5	
UART5	30.8	
I2C1	10.5	
I2C2	10.4	
USB	26.2	
CAN	33.4	
PWR	5.7	
DAC	15.4	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

Figure 18. HSI oscillator accuracy characterization results for soldered parts



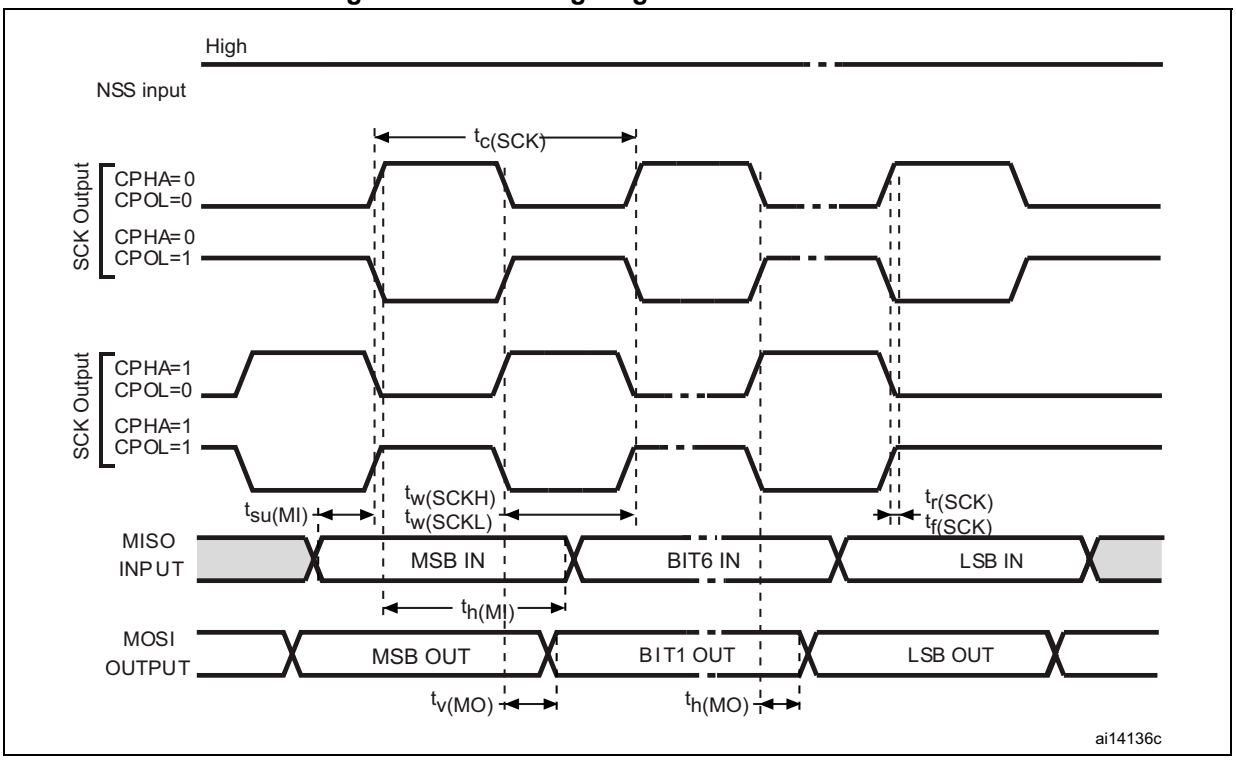
Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

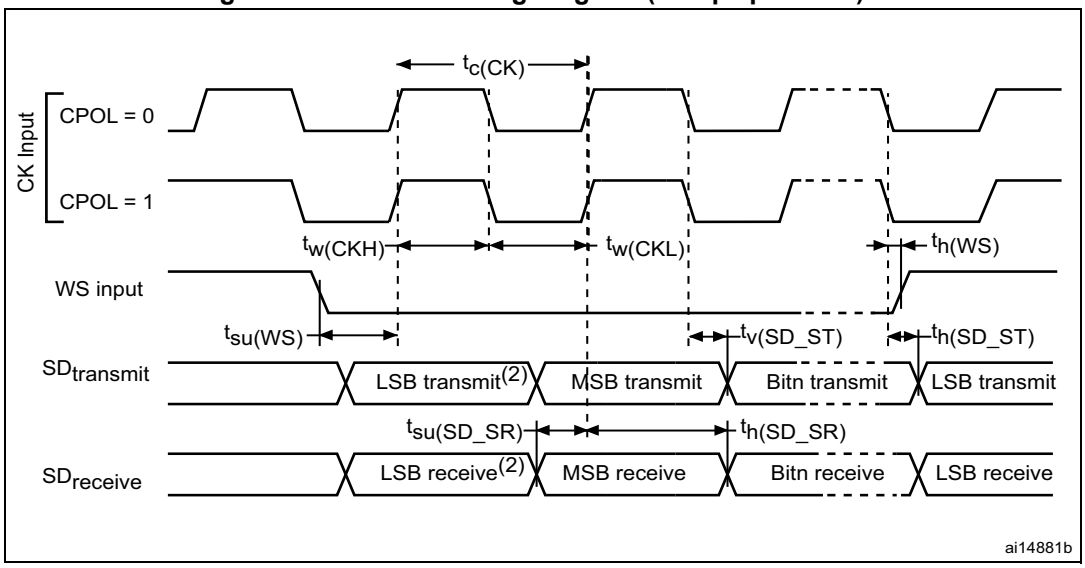
1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.

Figure 28. SPI timing diagram - master mode(1)



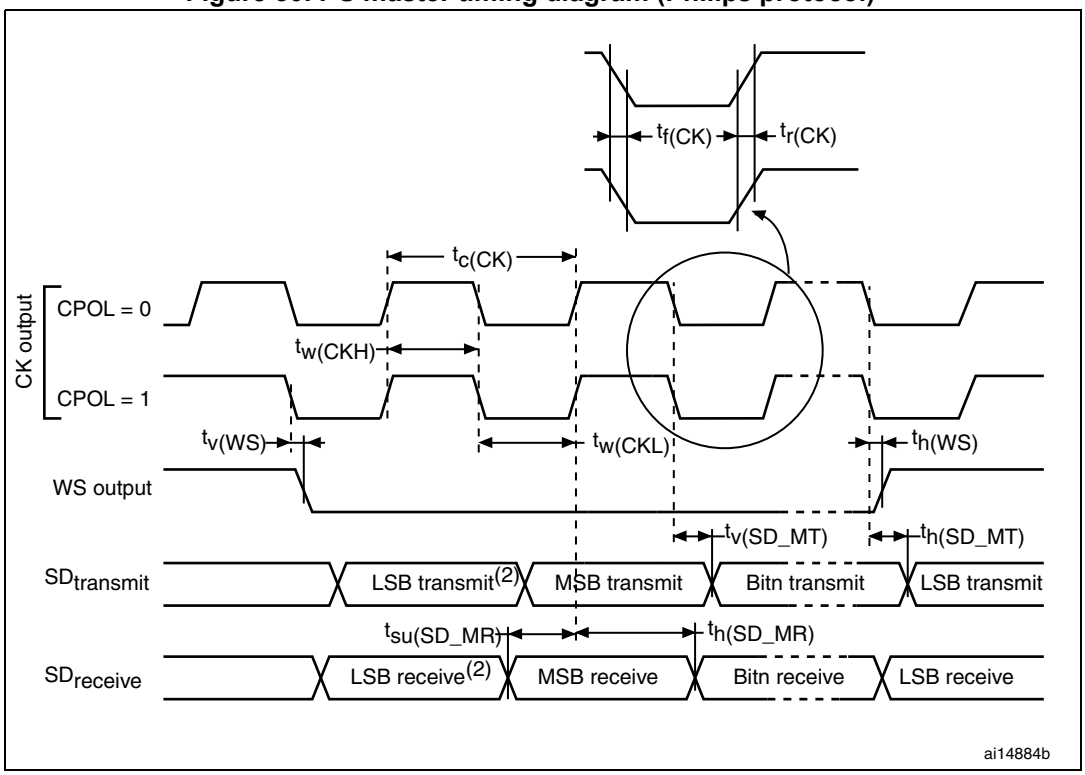
1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 29. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 30. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB characteristics

Table 65. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 66. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F303xB/STM32F303xC USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers.

Figure 31. USB timings: definition of data signal rise and fall time

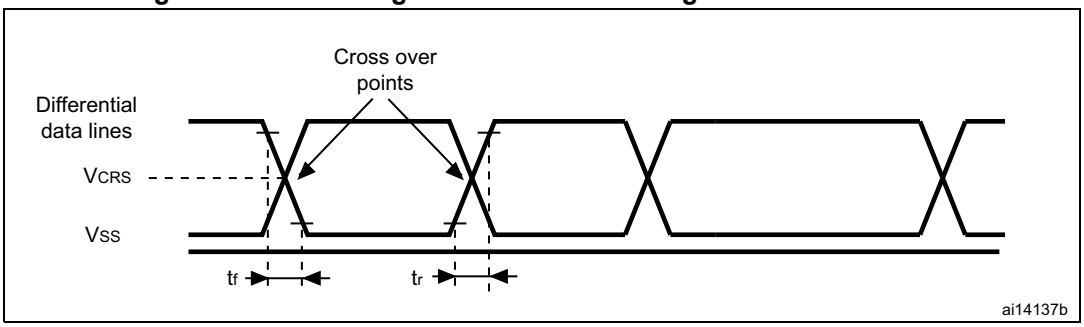


Table 67. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in *Table 68* to *Table 70* are guaranteed by design, with conditions summarized in *Table 24*.

Table 68. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	2	-	3.6	V
I_{DDA}	ADC current consumption on VDDA pin (see *Figure 32*)	Single-ended mode, 5 MSPS	-	907	1033.0	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	0	-	
I_{REF}	ADC current consumption on VREF+ pin (see *Figure 33*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	

6.3.21 Operational amplifier characteristics

Table 77. Operational amplifier characteristics(1)

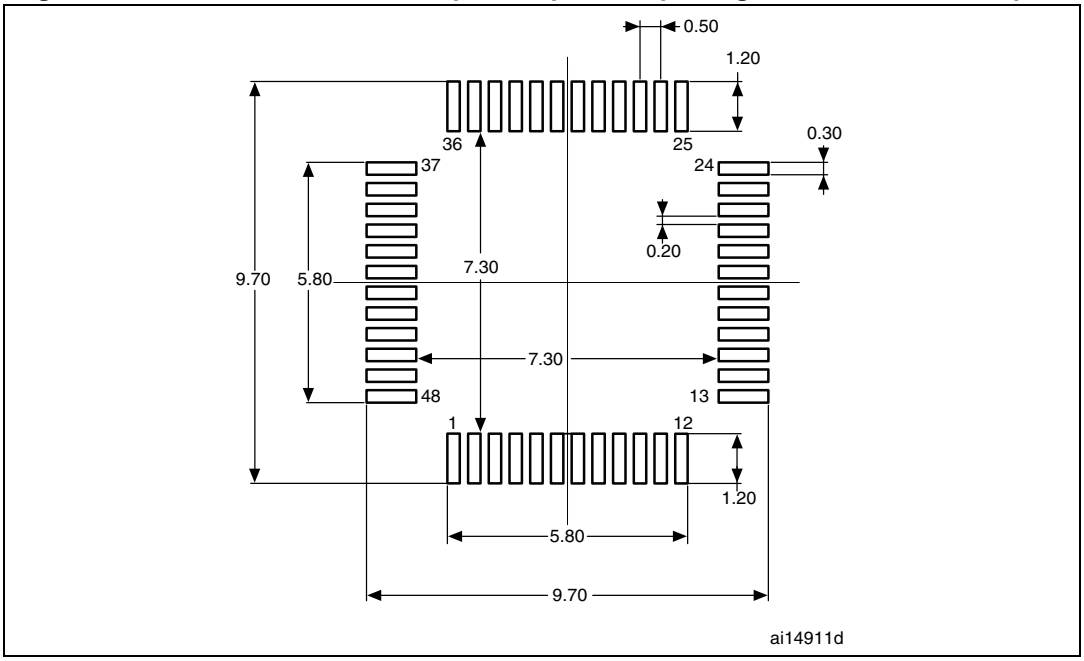
Symbol	Parameter		Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	µA
TS_OPAMP_VOUT	ADC sampling time when reading the OPAMP output.		-	400	-	-	ns
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage(2)		R_{load} = min, Input at V_{DDA}.	V_{DDA} -100	-	-	mV
			R_{load} = 20K, Input at V_{DDA}.	V_{DDA} -20	-	-	
VOL_{SAT}	High saturation voltage(2)		Rload = min, input at 0V	-	-	100	
			Rload = 20K, input at 0V.	-	-	20	
φm	Phase margin		-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.		C_{LOAD} ≤50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	2.8	5	µs

Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3	-	5.50	-	-	0.2165	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP48 - 7 x 7 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

Figure 49. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint

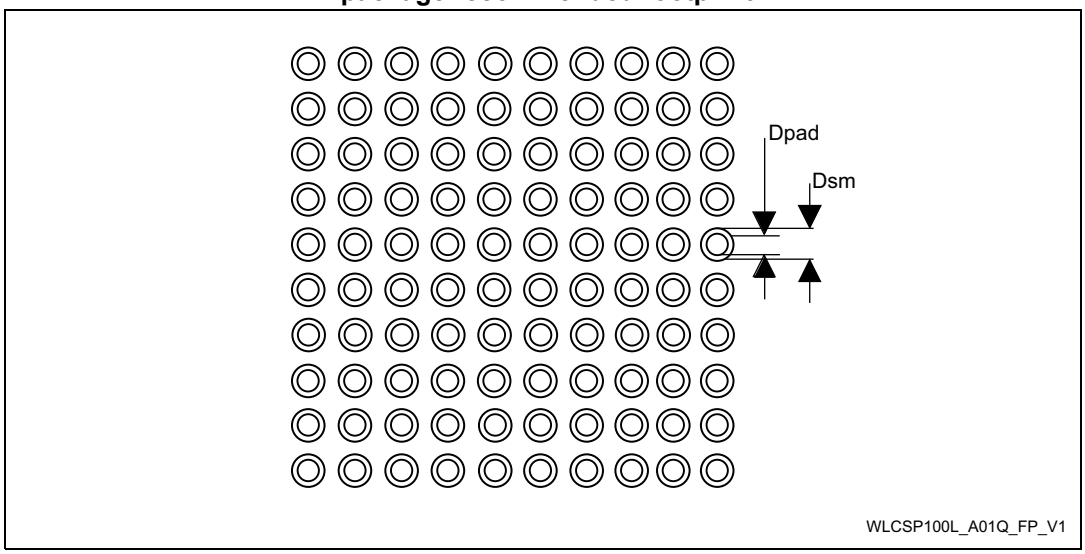


Table 85. WLCSP100 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

8 Ordering information

Table 87. Ordering information scheme

Example: STM32 F 303 R B T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

303 = STM32F303xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.