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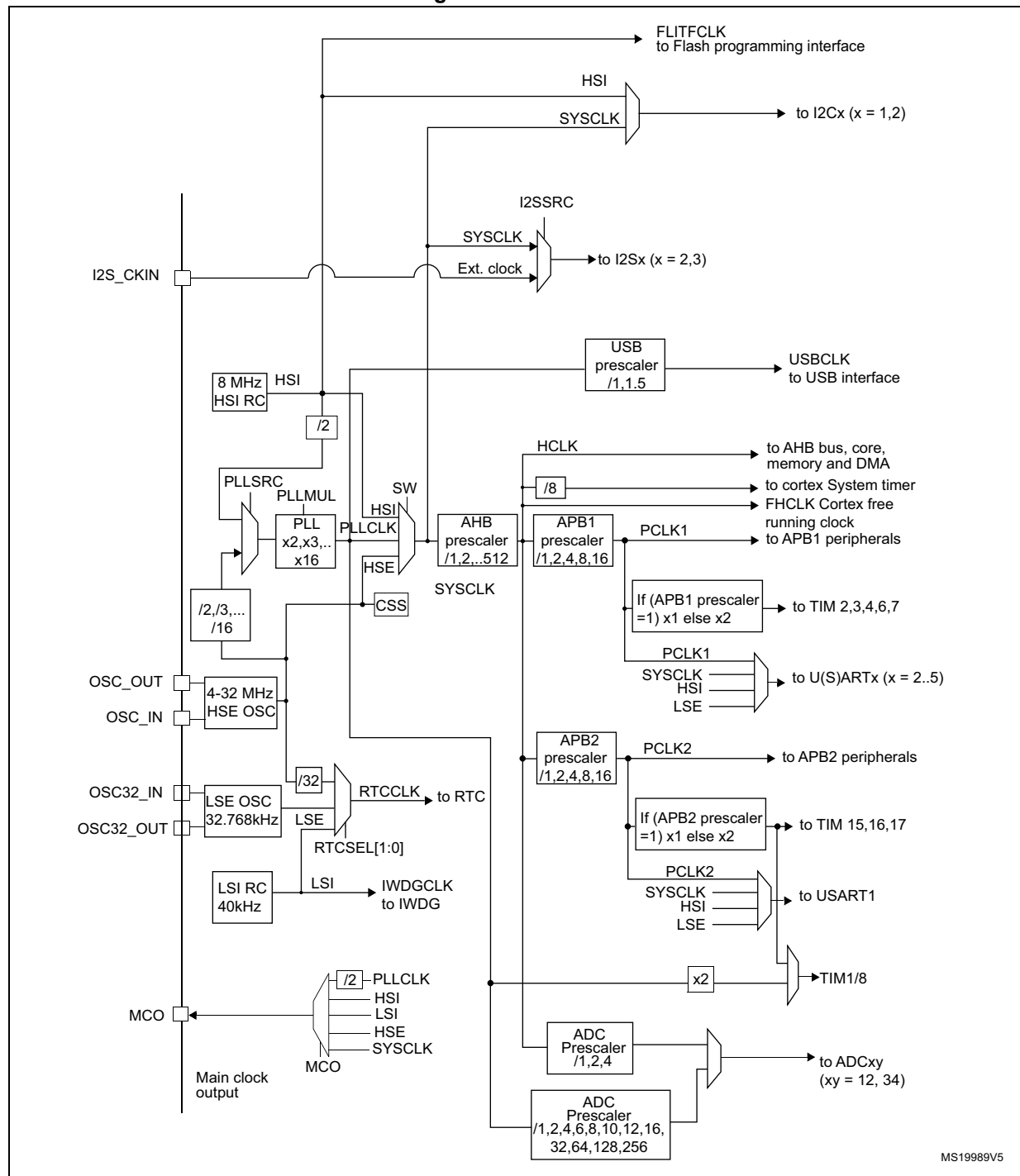
Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vct6

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Figure 2. Clock tree



3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose timers, DAC and ADC.

3.12 Interrupts and events

3.12.1 Nested vectored interrupt controller (NVIC)

The STM32F303xB/STM32F303xC devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F303xB/STM32F303xC pin definitions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
D6	1	-	-	PE2	I/O	FT	(1)	TRACECK, TIM3_CH1, TSC_G7_IO1, EVENTOUT	-
D7	2	-	-	PE3	I/O	FT	(1)	TRACED0, TIM3_CH2, TSC_G7_IO2, EVENTOUT	-
C8	3	-	-	PE4	I/O	FT	(1)	TRACED1, TIM3_CH3, TSC_G7_IO3, EVENTOUT	-
B9	4	-	-	PE5	I/O	FT	(1)	TRACED2, TIM3_CH4, TSC_G7_IO4, EVENTOUT	-
E7	5	-	-	PE6	I/O	FT	(1)	TRACED3, EVENTOUT	WKUP3, RTC_TAMP3
D8	6	1	1	V _{BAT}	S	-	-	Backup power supply	



Table 14. Alternate functions for port A

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA0	-	TIM2_CH1_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR	-	-	-	EVENT OUT
PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS_DE		TIM15_CH1N	-	-	-	-	EVENT OUT
PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	EVENT OUT
PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	EVENT OUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_CK	-	-	-	-	-	-	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	EVENT OUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	TIM8_BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	-	-	-	-	EVENT OUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N	-	COMP2_OUT	-	-	-	-	-	EVENT OUT
PA8	MCO	-	-	-	I2C2_SMBA	I2S2_MCK	TIM1_CH1	USART1_CK	COMP3_OUT	-	TIM4_ETR	-	-	-	EVENT OUT
PA9	-	-	-	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	COMP5_OUT	TIM15_BKIN	TIM2_CH3	-	-	-	EVENT OUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	-	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	TIM8_BKIN	-	-	EVENT OUT
PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	USB_DM	EVENT OUT

Table 18. Alternate functions for port E

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF6	AF7
PE0	-	EVENTOUT	TIM4_ETR	-	TIM16_CH1	-	USART1_TX
PE1	-	EVENTOUT	-	-	TIM17_CH1	-	USART1_RX
PE2	TRACECK	EVENTOUT	TIM3_CH1	TSC_G7_IO1	-	-	-
PE3	TRACED0	EVENTOUT	TIM3_CH2	TSC_G7_IO2	-	-	-
PE4	TRACED1	EVENTOUT	TIM3_CH3	TSC_G7_IO3	-	-	-
PE5	TRACED2	EVENTOUT	TIM3_CH4	TSC_G7_IO4	-	-	-
PE6	TRACED3	EVENTOUT		-	-	-	-
PE7	-	EVENTOUT	TIM1_ETR	-	-	-	-
PE8	-	EVENTOUT	TIM1_CH1N	-	-	-	-
PE9	-	EVENTOUT	TIM1_CH1	-	-	-	-
PE10	-	EVENTOUT	TIM1_CH2N	-	-	-	-
PE11	-	EVENTOUT	TIM1_CH2	-	-	-	-
PE12	-	EVENTOUT	TIM1_CH3N	-	-	-	-
PE13	-	EVENTOUT	TIM1_CH3	-	-	-	-
PE14	-	EVENTOUT	TIM1_CH4	-	-	TIM1_BKIN2	-
PE15	-	EVENTOUT	TIM1_BKIN	-	-	-	USART3_RX

2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA} .
3. V_{IN} maximum must always be respected. Refer to [Table 22: Current characteristics](#) for the maximum allowed injected current values.
4. Include VREF- pin.

Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)	-160	
I_{VDD}	Maximum current into each V_{DD} power line (source) ⁽¹⁾	100	
I_{VSS}	Maximum current out of each V_{SS} ground line (sink) ⁽¹⁾	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins ⁽²⁾	80	
	Total output current sourced by sum of all IOs and control pins ⁽²⁾	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins ⁽³⁾	-5/+0	
	Injected current on TC and RST pin ⁽⁴⁾	± 5	
	Injected current on TTa pins ⁽⁵⁾	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 21: Voltage characteristics](#) for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to [Table 21: Voltage characteristics](#) for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below [Table 70](#).
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3\text{ V}$
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB}/2$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 35. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	61.3	28.0	mA
			64 MHz	54.8	25.4	
			48 MHz	41.9	19.3	
			32 MHz	28.5	13.3	
			24 MHz	21.8	10.4	
			16 MHz	14.9	7.2	
			8 MHz	7.7	3.9	
			4 MHz	4.5	2.5	
			2 MHz	2.8	1.7	
			1 MHz	1.9	1.3	
			500 kHz	1.4	1.1	
			125 kHz	1.1	0.9	
$I_{DDA}^{(1)(2)}$	Supply current in Run mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	240.3	239.5	μA
			64 MHz	210.9	210.3	
			48 MHz	155.8	155.6	
			32 MHz	105.7	105.6	
			24 MHz	82.1	82.0	
			16 MHz	58.8	58.8	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.

2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 36. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	44.1	7.0	mA
			64 MHz	39.7	6.3	
			48 MHz	30.3	4.9	
			32 MHz	20.5	3.5	
			24 MHz	15.4	2.8	
			16 MHz	10.6	2.0	
			8 MHz	5.4	1.1	
			4 MHz	3.2	1.0	
			2 MHz	2.1	0.9	
			1 MHz	1.5	0.8	
			500 kHz	1.2	0.8	
			125 kHz	1.0	0.8	
$I_{DDA}^{(1)(2)}$	Supply current in Sleep mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	239.7	238.5	μA
			64 MHz	210.5	209.6	
			48 MHz	155.0	155.6	
			32 MHz	105.3	105.2	
			24 MHz	81.9	81.8	
			16 MHz	58.7	58.6	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.

2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 54](#) are derived from tests performed under the conditions summarized in [Table 24](#). All I/Os are CMOS and TTL compliant.

Table 54. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3 V_{DD} + 0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475 V_{DD} - 0.2^{(1)}$	
		BOOT0	-	-	$0.3 V_{DD} - 0.3^{(1)}$	
		All I/Os except BOOT0	-	-	$0.3 V_{DD}^{(2)}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445 V_{DD} + 0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5 V_{DD} + 0.2^{(1)}$	-	-	
		BOOT0	$0.2 V_{DD} + 0.95^{(1)}$	-	-	
		All I/Os except BOOT0	$0.7 V_{DD}^{(2)}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200 ⁽¹⁾	-	mV
		FT and FTf I/O	-	100 ⁽¹⁾	-	
		BOOT0	-	300 ⁽¹⁾	-	
I_{lkg}	Input leakage current ⁽³⁾	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 0.1	μA
		TTa I/O in digital mode $V_{DD} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O ⁽⁴⁾ $V_{DD} \leq V_{IN} \leq 5 V$	-	-	10	
R_{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$	25	40	55	$k\Omega$
R_{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	25	40	55	$k\Omega$
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.

2. Tested in production.

3. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 53: I/O current injection susceptibility](#).

4. To sustain a voltage higher than $V_{DD} + 0.3 V$, the internal pull-up/pull-down resistors must be disabled.

5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 19](#) and [Figure 20](#) for standard I/Os.

Figure 19. TC and TTa I/O input characteristics - CMOS port

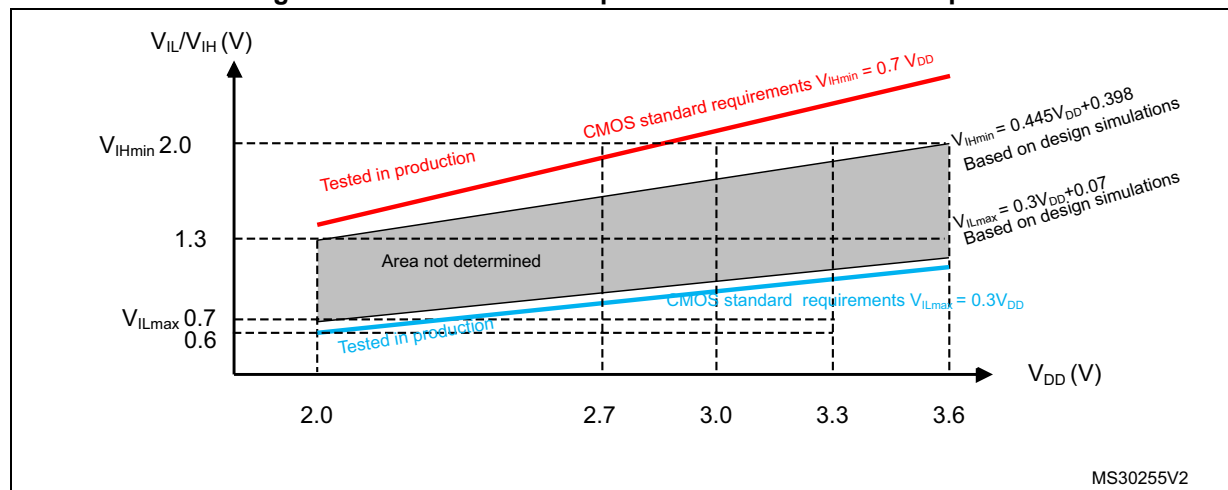
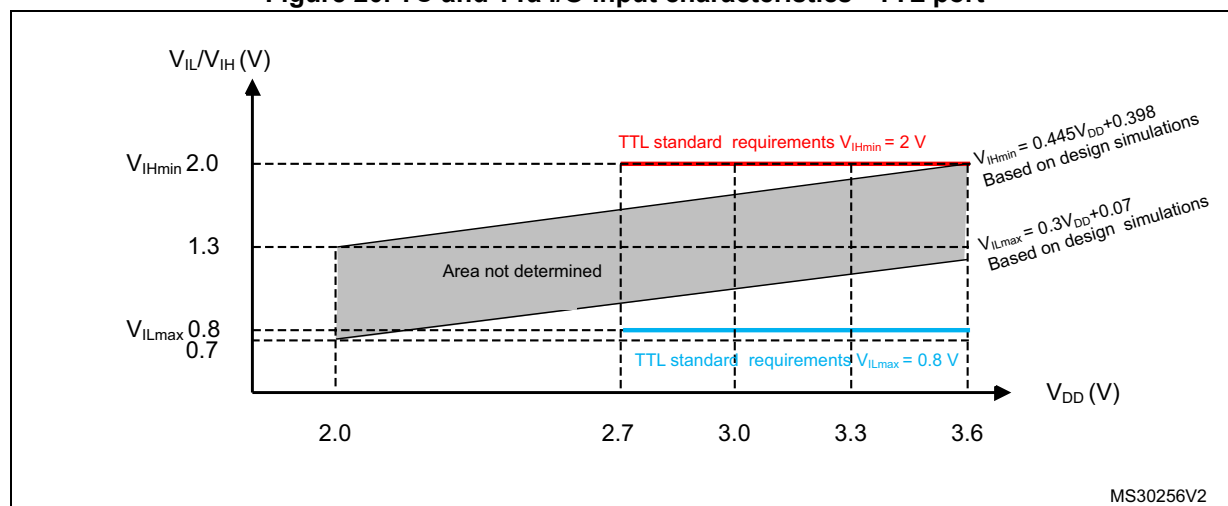


Figure 20. TC and TTa I/O input characteristics - TTL port



USB characteristics

Table 65. USB startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB transceiver startup time	1	μs

1. Guaranteed by design.

Table 66. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input levels					
V _{DD}	USB operating voltage ⁽²⁾	-	3.0 ⁽³⁾	3.6	V
V _{DI} ⁽⁴⁾	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V _{CM} ⁽⁴⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	
V _{SE} ⁽⁴⁾	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V _{OL}	Static output level low	R _L of 1.5 kΩ to 3.6 V ⁽⁵⁾	-	0.3	V
V _{OH}	Static output level high	R _L of 15 kΩ to V _{SS} ⁽⁵⁾	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 k Ω resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F303xB/STM32F303xC USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_{L} is the load connected on the USB drivers.

Figure 31. USB timings: definition of data signal rise and fall time

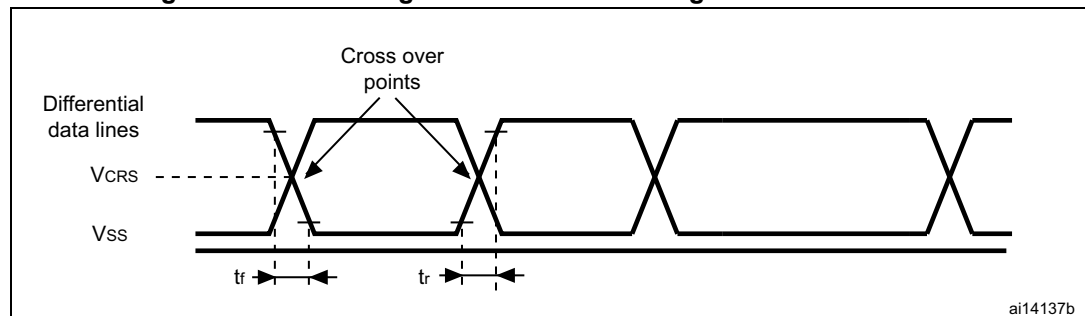
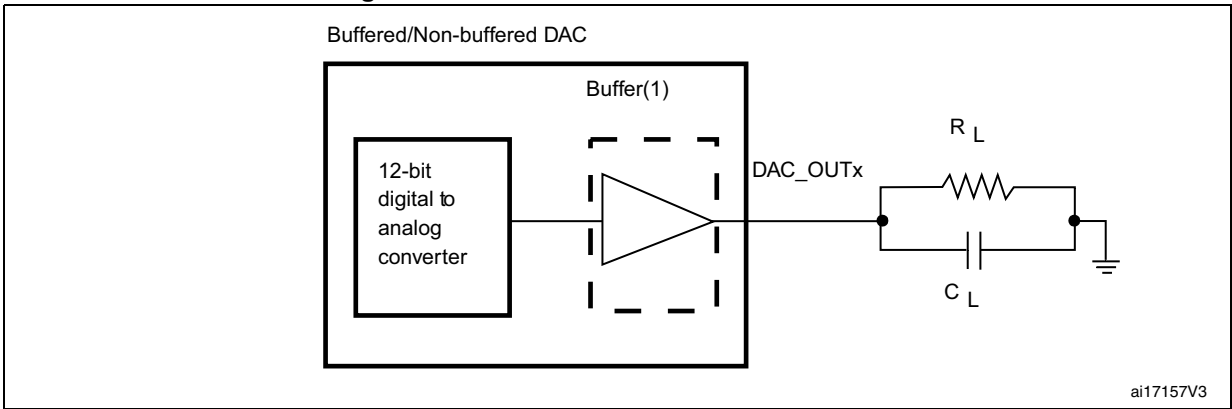


Table 75. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{WAKEUP}}^{(3)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{\text{LOAD}} \leq 50 \text{ pF}$, $R_{\text{LOAD}} \geq 5 \text{ k}\Omega$	-	6.5	10	μs
PSRR+ ⁽¹⁾	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	$C_{\text{LOAD}} = 50 \text{ pF}$, No $R_{\text{LOAD}} \geq 5 \text{ k}\Omega$	-	-67	-40	dB

1. Guaranteed by design.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization results.

Figure 36. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

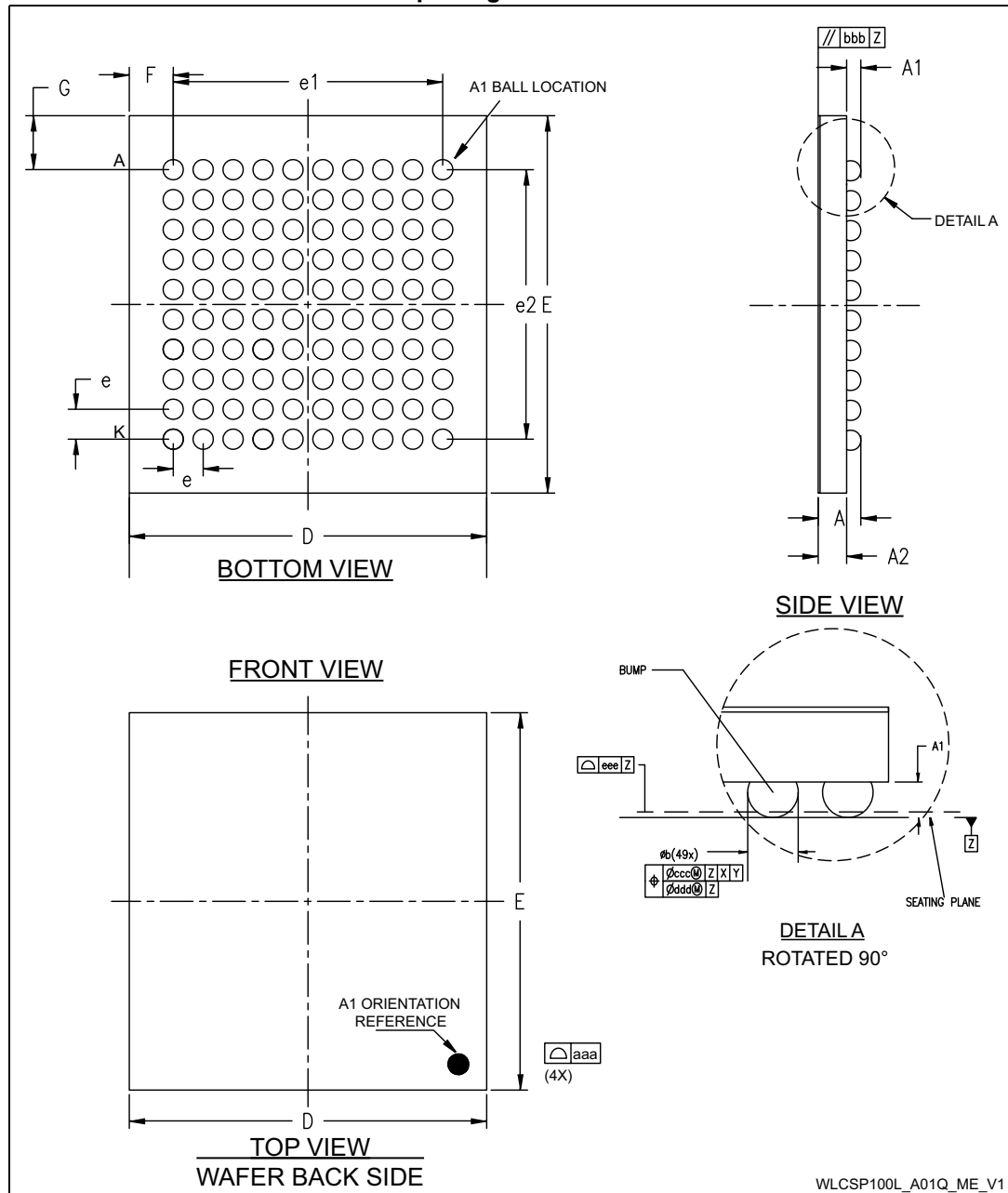
6.3.20 Comparator characteristics

Table 76. Comparator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-	-	1.2	-	
V_{SC}	Scaler offset voltage	-	-	± 5	± 10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on	-	-	1 ⁽²⁾	s
		Next activations	-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification	-	-	60	μ s
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low-power mode	-	2	4.5	μ s
		Low-power mode	-	0.7	1.5	
		Medium power mode	-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V		-	ns
			$V_{DDA} < 2.7$ V		-	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low-power mode	-	2	7	μ s
		Low-power mode	-	0.7	2.1	
		Medium power mode	-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V		-	ns
			$V_{DDA} < 2.7$ V		-	
V_{offset}	Comparator offset error	-	-	± 4	± 10	mV
dV_{offset}/dT	Offset error temperature coefficient	-	-	18	-	μ V/ $^{\circ}$ C
$I_{DD(Comp)}$	COMP current consumption	Ultra-low-power mode	-	1.2	1.5	μ A
		Low-power mode	-	3	5	
		Medium power mode	-	10	15	
		High speed mode	-	75	100	

7.4 WLCSP100 - 0.4 mm pitch wafer level chip scale package information

Figure 48.WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 84. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Typ	Min	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
Ø b ⁽³⁾	0.22	0.25	0.28	-	0.0098	0.0110
D	4.166	4.201	4.236	-	0.1654	0.1668
E	4.628	4.663	4.698	-	0.1836	0.1850
e	-	0.4	-	-	0.0157	-
e1	-	3.6	-	-	0.1417	-
e2	-	3.6	-	-	0.1417	-
F	-	0.3005	-	-	0.0118	-
G	-	0.5315	-	-	0.0209	-
N	-	100	-	-	3.9370	-
aaa	-	0.1	-	-	0.0039	-
bbb	-	0.1	-	-	0.0039	-
ccc	-	0.1	-	-	0.0039	-
ddd	-	0.05	-	-	0.0020	-
eee	-	0.05	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating.

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Table 88. Document revision history (continued)

Date	Revision	Changes
18-Apr-2014	8	Updated Table 50: EMI characteristics conditions :3.3v replaced by 3.6V. Updated Section 6.3.17: Communications interfaces I²C interface. Updated Table 77: Operational amplifier characteristics adding TS_OPAMP_VOUT row. Updated Section 3.13: Fast analog-to-digital converter (ADC). updated ARM and Cortex trademark. Updated Table 32: Typical and maximum VDD consumption in Stop and Standby modes with Max value at 85°C and 105°C. Updated Table 70: ADC accuracy - limited test conditions, 100-pin packages and Table 71: ADC accuracy, 100-pin packages for 100-pin package. Added Table 72: ADC accuracy - limited test conditions, 64-pin packages and Table 73: ADC accuracy, 64-pin packages for 64-pin package. Added Table 74: ADC accuracy at 1MSPS for 1MSPS sampling frequency. Updated Table 63: SPI characteristics. Updated Table 75: DAC characteristics.
09-Dec-2014	9	Updated core description in cover page. Updated HSI characteristics Table 44: HSI oscillator characteristics and Figure 18: HSI oscillator accuracy characterization results for soldered parts. Updated Table 58: TIMx characteristics. Updated Table 16: STM32F302xB/STM32F302xC pin definitions adding note for I/Os featuring an analog output function (DAC_OUT, OPAMP_OUT). Updated Table 68: ADC characteristics adding IDDA & IREF consumptions. Added Figure 32: ADC typical current consumption on VDDA pin and Figure 33: ADC typical current consumption on VREF+ pin. Added Section 3.8: Interconnect matrix. Updated Figure 5: Clock tree. Added note after Table 32: Typical and maximum VDD consumption in Stop and Standby modes. Updated Section : <i>In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.</i> with new LQFP100, LQFP64, LQFP48 package marking. Updated Table 16: STM32F302xB/STM32F302xC pin definitions and alternate functions tables replacing usart_rts by usart_rts_de.
29-Jan-2015	10	Updated Section 6.3.20: Comparator characteristics modifying ts_sc characteristics in Table 76 and adding Figure 37: Maximum VREFINT scaler startup time from power down. Updated I_{DD} data in Table 42: HSE oscillator characteristics.

Table 88. Document revision history (continued)

Date	Revision	Changes
06-May-2016	13	Updated Table 43: LSE oscillator characteristics (fLSE = 32.768 kHz) LSEDRV[1:0] bits. Updated Table 28: Embedded internal reference voltage V_{REFINT} internal reference voltage (min and typ values). Updated Figure 5: STM32F303xB/STM32F303xC LQFP64 pinout replacing VSS by PF4. Updated Table 51: ESD absolute maximum ratings ESD CDM at class 3 and 4 including WLCSP100 package information. Updated Table 13: STM32F303xB/STM32F303xC pin definitions: – Adding 'digital power supply' in the Pin function column at the line corresponding to K8/28/19 pins. – Adding VSS digital ground line with WLCSP100 K9 and K10 pins connected. – Replacing in VDD line for WLCSP100: 'A10, B10' by 'A9, A10, B10, B8'. Updated Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port. Updated Table 77: Operational amplifier characteristics high saturation and low saturation voltages. Updated Table 13: STM32F303xB/STM32F303xC pin definitions adding note 'Fast ADC channel' for ADCx_IN1..5. Updated Table 75: DAC characteristics resistive load. Updated Table 68: ADC characteristics adding CMIR parameter and modifying tSTAB parameter characteristics.