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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flit19f1m6tr

16.5	CLEARING ACTIVE INTERRUPTS OUTSIDE INTERRUPT ROUTINE	129
16.6	USING PB4 AS EXTERNAL INTERRUPT	129
17	REVISION HISTORY	130

To obtain the most recent version of this datasheet,
please check at www.st.com>products>technical literature>datasheet

Please also pay special attention to the Section “IMPORTANT NOTES” on page 128.

FLASH PROGRAM MEMORY (Cont'd)

4.5 Memory Protection

There are two different types of memory protection: Read Out Protection and Write/Erase Protection which can be applied individually.

4.5.1 Read out Protection

Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller. Both program and data E² memory are protected.

In flash devices, this protection is removed by reprogramming the option. In this case, both program and data E² memory are automatically erased and the device can be reprogrammed.

Read-out protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the Option List.

4.5.2 Flash Write/Erase Protection

Write/erase protection, when set, makes it impossible to both overwrite and erase program memory. It does not apply to E² data. Its purpose is to provide advanced security to applications and prevent any change being made to the memory content.

Warning: Once set, Write/erase protection can never be removed. A write-protected flash device is no longer reprogrammable.

Write/erase protection is enabled through the FMP_W bit in the option byte.

4.6 Related Documentation

For details on Flash programming and ICC protocol, refer to the ST7 Flash Programming Reference Manual and to the ST7 ICC Protocol Reference Manual.

4.7 Register Description

FLASH CONTROL/STATUS REGISTER (FCSR)

Read/Write

Reset Value: 000 0000 (00h)

1st RASS Key: 0101 0110 (56h)

2nd RASS Key: 1010 1110 (AEh)

7					0		
0	0	0	0	0	OPT	LAT	PGM

Note: This register is reserved for programming using ICP, IAP or other programming methods. It controls the XFlash programming and erasing operations.

When an EPB or another programming tool is used (in socket or ICP mode), the RASS keys are sent automatically.

5 DATA EEPROM

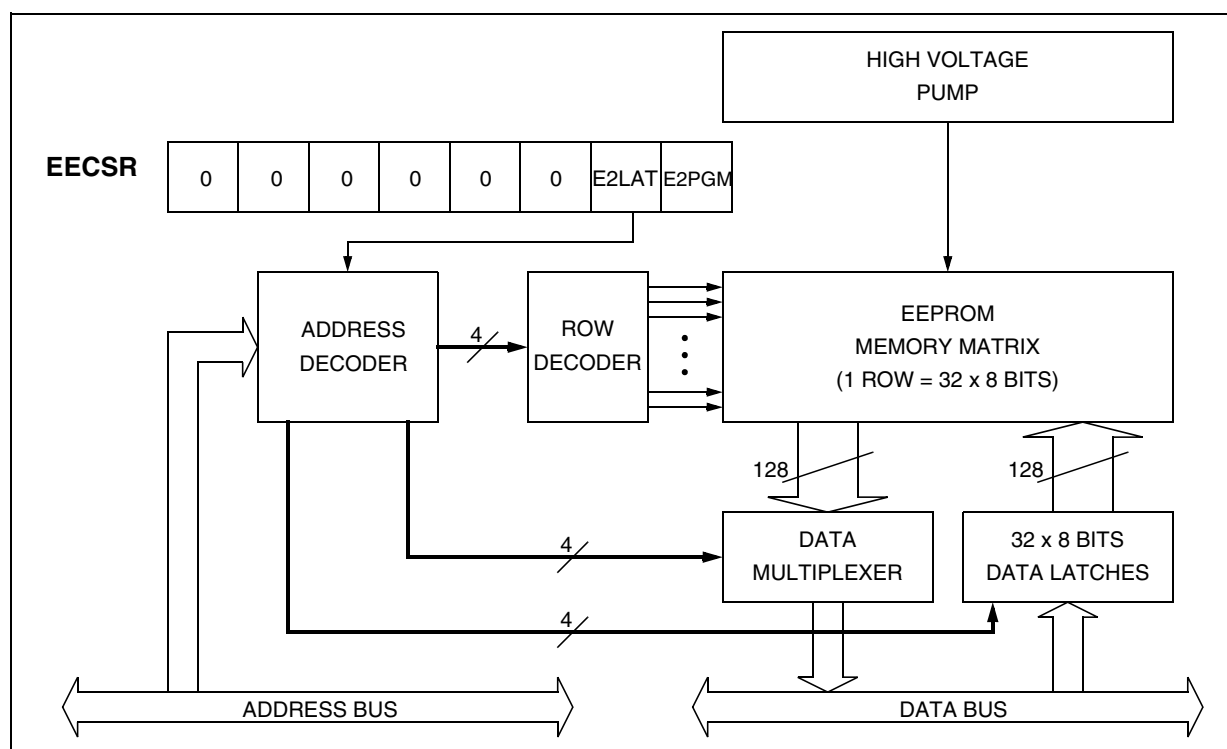
5.1 INTRODUCTION

The Electrically Erasable Programmable Read Only Memory can be used as a non volatile back-up for storing data. Using the EEPROM requires a basic access protocol described in this chapter.

5.2 MAIN FEATURES

- Up to 32 Bytes programmed in the same cycle
- EEPROM mono-voltage (charge pump)
- Chained erase and programming cycles
- Internal control of the global programming cycle duration
- WAIT mode management
- Readout protection

Figure 5. EEPROM Block Diagram



SYSTEM INTEGRITY MANAGEMENT (Cont'd)

7.6.2 Auxiliary Voltage Detector (AVD)

The Voltage Detector function (AVD) is based on an analog comparison between a $V_{IT-(AVD)}$ and $V_{IT+(AVD)}$ reference value and the V_{DD} main supply voltage (V_{AVD}). The $V_{IT-(AVD)}$ reference value for falling voltage is lower than the $V_{IT+(AVD)}$ reference value for rising voltage in order to avoid parasitic detection (hysteresis).

The output of the AVD comparator is directly readable by the application software through a real time status bit (AVDF) in the SICSR register. This bit is read only.

Caution: The AVD functions only if the LVD is enabled through the option byte.

abled through the option byte.

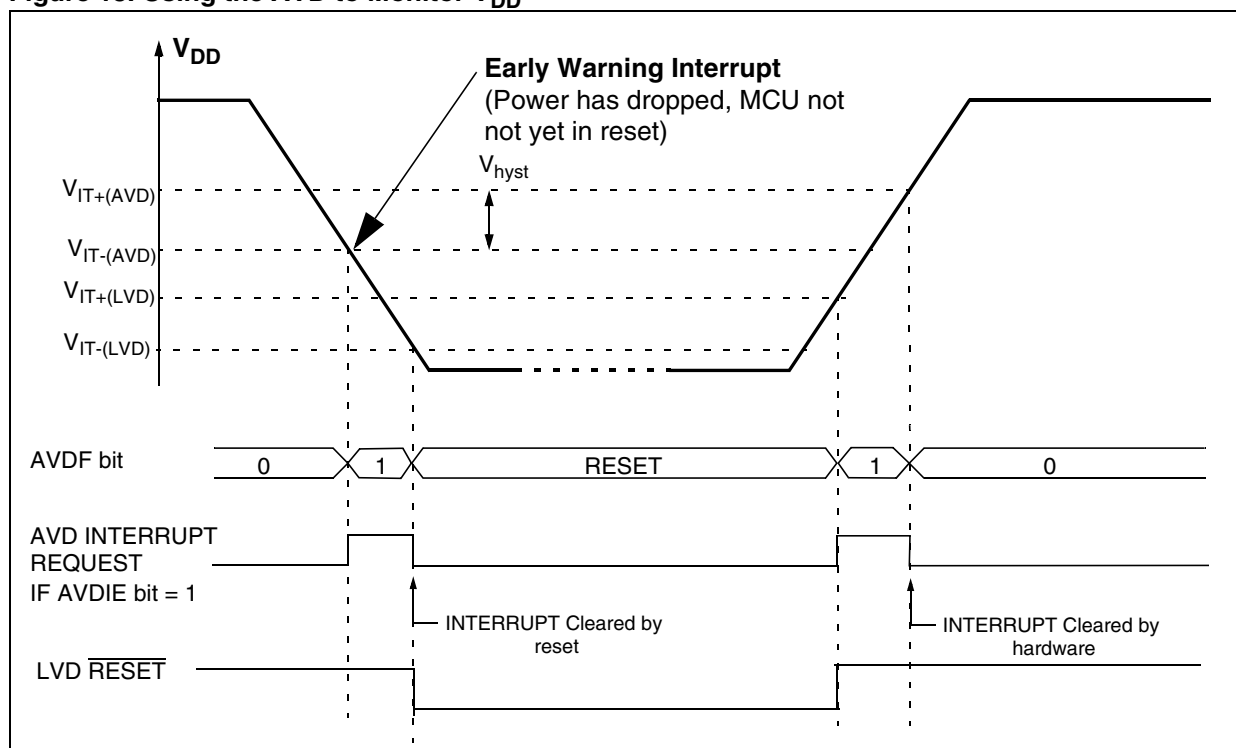
7.6.2.1 Monitoring the V_{DD} Main Supply

The AVD voltage threshold value is relative to the selected LVD threshold configured by option byte (see [section 15.1 on page 121](#)).

If the AVD interrupt is enabled, an interrupt is generated when the voltage crosses the $V_{IT+(LVD)}$ or $V_{IT-(AVD)}$ threshold (AVDF bit is set).

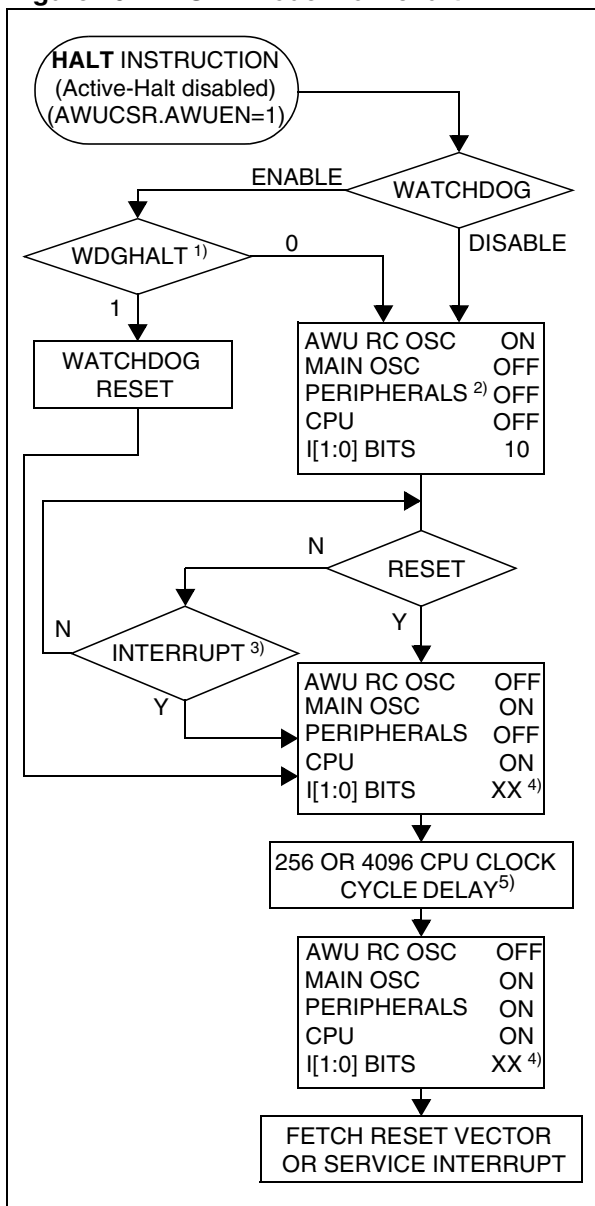
In the case of a drop in voltage, the AVD interrupt acts as an early warning, allowing software to shut down safely before the LVD resets the microcontroller. See [Figure 18](#).

Figure 18. Using the AVD to Monitor V_{DD}



POWER SAVING MODES (Cont'd)

Figure 29. AWUFH Mode Flow-chart



Notes:

1. WDGHALT is an option bit. See option byte section for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only an AWUFH interrupt and some specific interrupts can exit the MCU from HALT mode (such as external interrupt). Refer to Table 5, "Interrupt Mapping," on page 35 for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.
5. If the PLL is enabled by option byte, it outputs the clock after an additional delay of $t_{STARTUP}$ (see Figure 11).

I/O PORTS (Cont'd)

10.7 DEVICE-SPECIFIC I/O PORT CONFIGURATION

The I/O port register configurations are summarised as follows.

Standard Ports

PA7:0, PB6:0

MODE	DDR	OR
floating input	0	0
pull-up input	0	1
open drain output	1	0
push-pull output	1	1

Interrupt Ports

Ports where the external interrupt capability is selected using the EISR register

MODE	DDR	OR
floating input	0	0
pull-up interrupt input	0	1
open drain output	1	0
push-pull output	1	1

Table 10. Port Configuration (Standard ports)

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	floating	pull-up	open drain	push-pull
Port B	PB6:0	floating	pull-up	open drain	push-pull

Note: On ports where the external interrupt capability is selected using the EISR register, the configuration will be as follows:

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	floating	pull-up interrupt	open drain	push-pull
Port B	PB6:0	floating	pull-up interrupt	open drain	push-pull

Table 11. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0000h	PADR Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
0001h	PADDR Reset Value	MSB 0	0	0	0	0	0	0	LSB 0
0002h	PAOR Reset Value	MSB 0	1	0	0	0	0	0	LSB 0
0003h	PBDR Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
0004h	PBDDR Reset Value	MSB 0	0	0	0	0	0	0	LSB 0
0005h	PBOR Reset Value	MSB 0	0	0	0	0	0	0	LSB 0

WATCHDOG TIMER (Cont'd)

The application program must write in the CR register at regular intervals during normal operation to prevent an MCU reset. This downcounter is free-running: it counts down even if the watchdog is disabled. The value to be stored in the CR register must be between FFh and C0h (see [Table 12 .Watchdog Timing](#)):

- The WDGA bit is set (watchdog enabled)
- The T6 bit is set to prevent generating an immediate reset
- The T[5:0] bits contain the number of increments which represents the time delay before the watchdog produces a reset.

Following a reset, the watchdog is disabled. Once activated it cannot be disabled, except by a reset.

The T6 bit can be used to generate a software reset (the WDGA bit is set and the T6 bit is cleared).

If the watchdog is activated, the HALT instruction will generate a Reset.

Table 12. Watchdog Timing

$f_{\text{CPU}} = 8\text{MHz}$		
WDG Counter Code	min [ms]	max [ms]
C0h	1	2
FFh	127	128

Notes:

1. The timing variation shown in [Table 12](#) is due to the unknown status of the prescaler when writing to the CR register.

2. The number of CPU clock cycles applied during the RESET phase (256 or 4096) must be taken into account in addition to these timings.

11.1.4 Hardware Watchdog Option

If Hardware Watchdog is selected by option byte, the watchdog is always active and the WDGA bit in the CR is not used.

Refer to the Option Byte description in [section 15 on page 121](#).

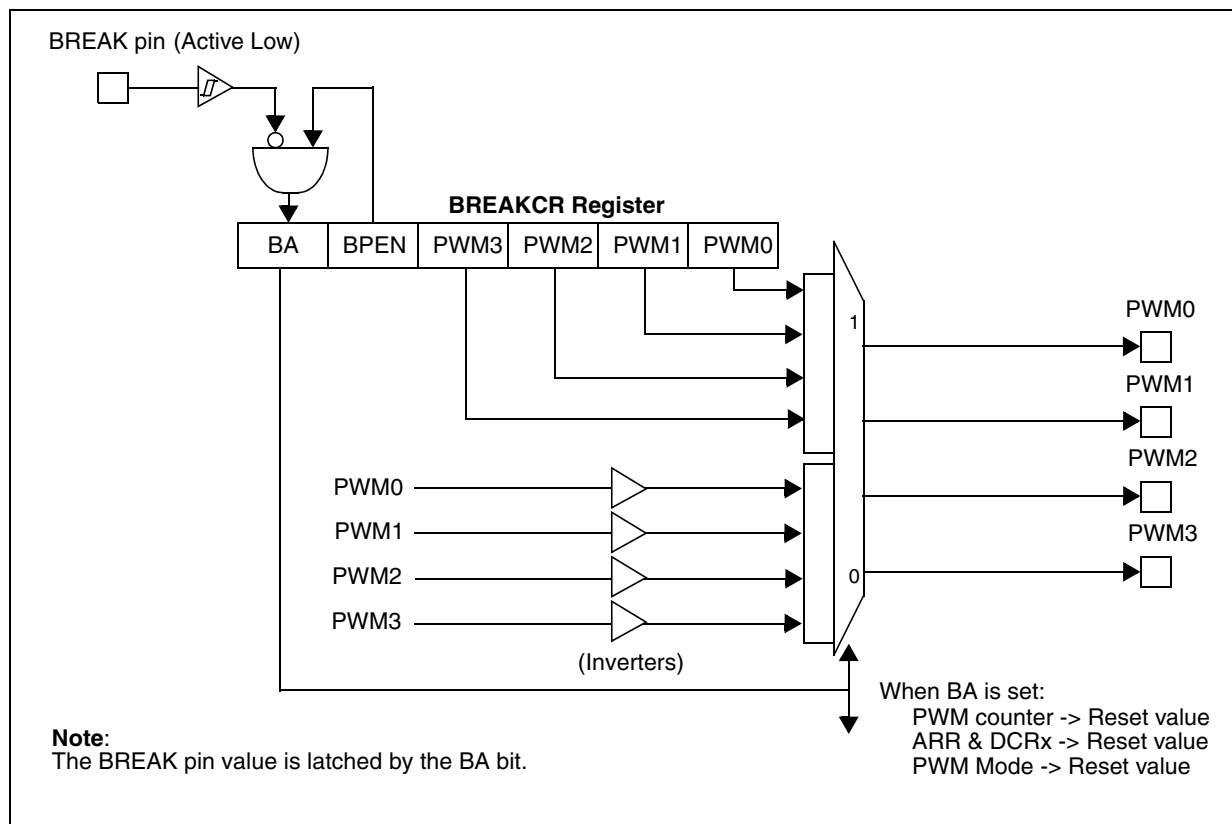
11.1.4.1 Using Halt Mode with the WDG (WDGHALT option)

If Halt mode with Watchdog is enabled by option byte (No watchdog reset on HALT instruction), it is recommended before executing the HALT instruction to refresh the WDG counter, to avoid an unexpected WDG reset immediately after waking up the microcontroller. Same behavior in active-halt mode.

WATCHDOG TIMER (Cont'd)**Table 13. Watchdog Timer Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Eh	WDGCR Reset Value	WDGA 0	T6 1	T5 1	T4 1	T3 1	T2 1	T1 1	T0 1

Figure 37. Block Diagram of Break Function

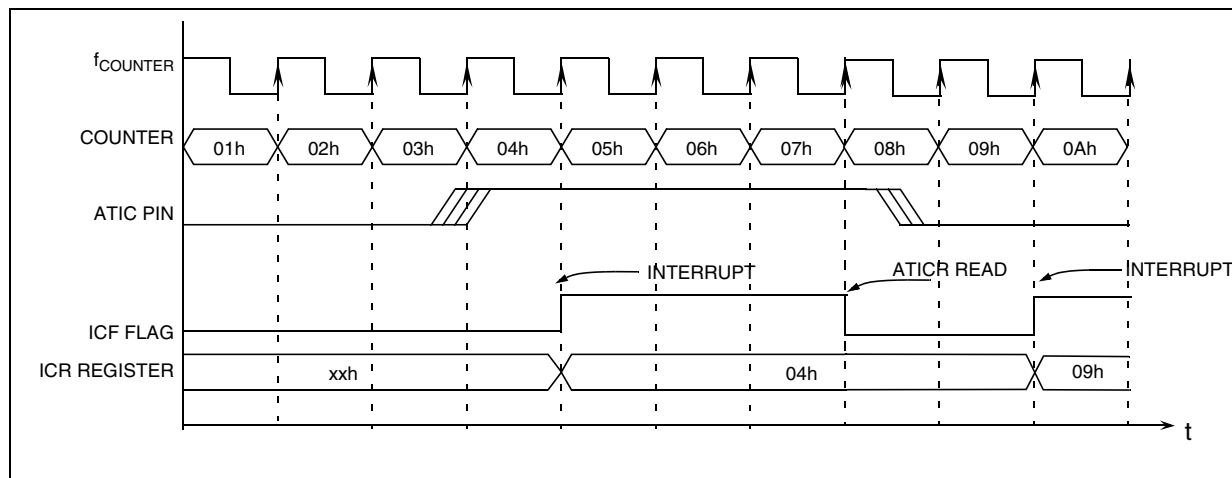


11.2.3.1 Input Capture

The 12-bit ATICR register is used to latch the value of the 12-bit free running upcounter after a rising or falling edge is detected on the ATIC pin. When an input capture occurs, the ICF bit is set and the ATICR register contains the value of the

free running upcounter. An IC interrupt is generated if the ICIE bit is set. The ICF bit is reset by reading the ATICR register when the ICF bit is set. The ATICR is a read only register and always contains the free running upcounter value which corresponds to the most recent input capture. Any further input capture is inhibited while the ICF bit is set.

Figure 38. Input Capture Timing Diagram



LITE TIMER (Cont'd)

- The opcode for the HALT instruction is 0x8E. To avoid an unexpected HALT instruction due to a program counter failure, it is advised to clear all occurrences of the data value 0x8E from memory. For example, avoid defining a constant in ROM with the value 0x8E.
- As the HALT instruction clears the I bit in the CC register to allow interrupts, the user may choose to clear all pending interrupt bits before executing the HALT instruction. This avoids entering other peripheral interrupt routines after executing the external interrupt routine corresponding to the wake-up event (reset or external interrupt).

11.3.4 Low Power Modes

Mode	Description
SLOW	No effect on Lite timer (this peripheral is driven directly by $f_{OSC}/32$)
WAIT	No effect on Lite timer
ACTIVE-HALT	No effect on Lite timer
HALT	Lite timer stops counting

11.3.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Active Halt	Exit from Halt
Timebase 1 Event	TB1F	TB1IE	Yes	Yes	No
Timebase 2 Event	TB2F	TB2IE	Yes	No	No
IC Event	ICF	ICIE	Yes	No	No

Note: The TBxF and ICF interrupt events are connected to separate interrupt vectors (see Interrupts chapter).

They generate an interrupt if the enable bit is set in the LTCSR1 or LTCSR2 register and the interrupt mask in the CC register is reset (RIM instruction).

11.3.6 Register Description

LITE TIMER CONTROL/STATUS REGISTER 2 (LTCSR2)

Read / Write

Reset Value: 0x00 0000 (x0h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TB2IE	TB2F

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **TB2IE** *Timebase 2 Interrupt enable.*

This bit is set and cleared by software.

0: Timebase (TB2) interrupt disabled

1: Timebase (TB2) interrupt enabled

Bit 0 = **TB2F** *Timebase 2 Interrupt Flag.*

This bit is set by hardware and cleared by software reading the LTCSR register. Writing to this bit has no effect.

0: No Counter 2 overflow

1: A Counter 2 overflow has occurred

LITE TIMER AUTORELOAD REGISTER (LTARR)

Read / Write

Reset Value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
AR7	AR7	AR7	AR7	AR3	AR2	AR1	AR0

Bits 7:0 = **AR[7:0]** *Counter 2 Reload Value.*

These bits register is read/write by software. The LTARR value is automatically loaded into Counter 2 (LTCNTR) when an overflow occurs.

LITE TIMER (Cont'd)

Table 15. Lite Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
08	LTCSR2 Reset Value	0	0	0	0	0	0	TB2IE 0	TB2F 0
09	LTARR Reset Value	AR7 0	AR6 0	AR5 0	AR4 0	AR3 0	AR2 0	AR1 0	AR0 0
0A	LTCNTR Reset Value	CNT7 0	CNT6 0	CNT5 0	CNT4 0	CNT3 0	CNT2 0	CNT1 0	CNT0 0
0B	LTCSR1 Reset Value	ICIE 0	ICF x	TB 0	TB1IE 0	TB1F 0	0	0	0
0C	LTICR Reset Value	ICR7 0	ICR6 0	ICR5 0	ICR4 0	ICR3 0	ICR2 0	ICR1 0	ICR0 0

SERIAL PERIPHERAL INTERFACE (Cont'd)

11.4.3.2 Slave Select Management

As an alternative to using the \overline{SS} pin to control the Slave Select signal, the application can choose to manage the Slave Select signal by software. This is configured by the SSM bit in the SPICSR register (see Figure 44)

In software management, the external \overline{SS} pin is free for other application uses and the internal \overline{SS} signal level is driven by writing to the SSI bit in the SPICSR register.

In Master mode:

- \overline{SS} internal must be held high continuously

In Slave Mode:

There are two cases depending on the data/clock timing relationship (see Figure 43):

If CPHA=1 (data latched on 2nd clock edge):

- \overline{SS} internal must be held low during the entire transmission. This implies that in single slave applications the \overline{SS} pin either can be tied to V_{SS} , or made free for standard I/O by managing the \overline{SS} function by software (SSM= 1 and SSI=0 in the in the SPICSR register)

If CPHA=0 (data latched on 1st clock edge):

- \overline{SS} internal must be held low during byte transmission and pulled high between each byte to allow the slave to write to the shift register. If \overline{SS} is not pulled high, a Write Collision error will occur when the slave writes to the shift register (see Section 11.4.5.3).

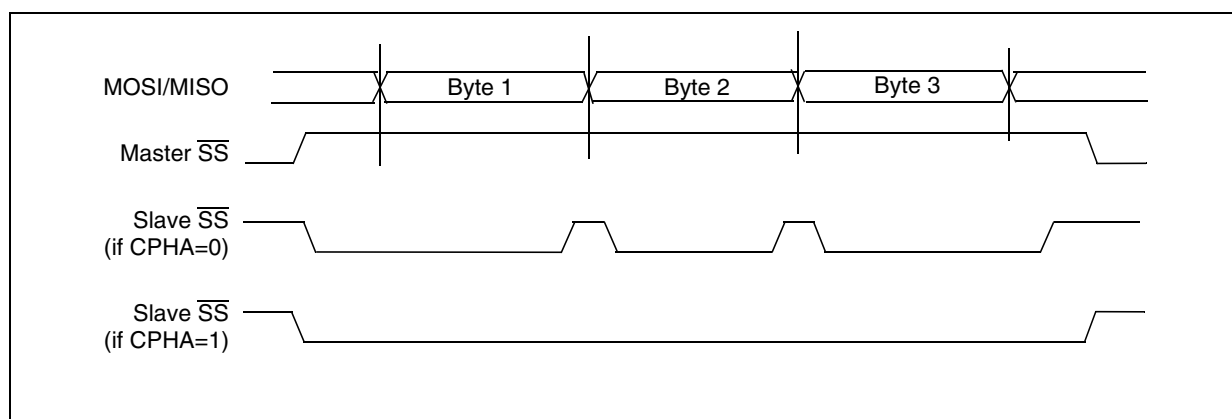
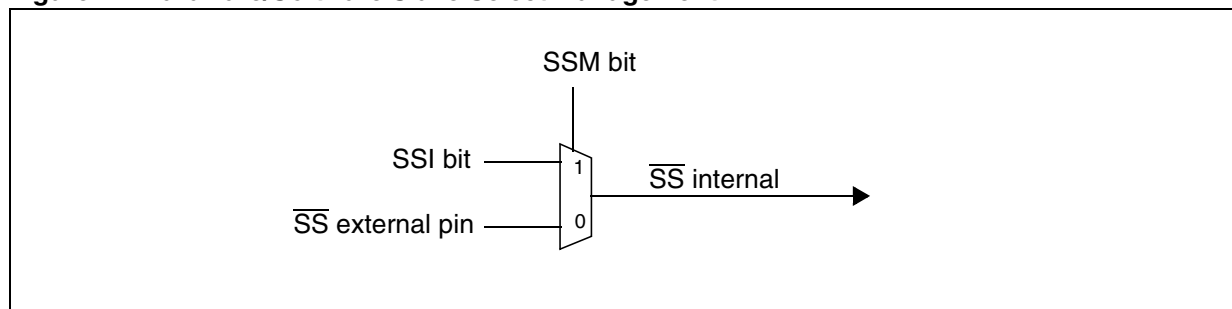
Figure 43. Generic \overline{SS} Timing Diagram

Figure 44. Hardware/Software Slave Select Management



SERIAL PERIPHERAL INTERFACE (Cont'd)

11.4.5 Error Flags

11.4.5.1 Master Mode Fault (MODF)

Master mode fault occurs when the master device has its \overline{SS} pin pulled low.

When a Master mode fault occurs:

- The MODF bit is set and an SPI interrupt request is generated if the SPIE bit is set.
- The SPE bit is reset. This blocks all output from the Device and disables the SPI peripheral.
- The MSTR bit is reset, thus forcing the Device into slave mode.

Clearing the MODF bit is done through a software sequence:

1. A read access to the SPICSR register while the MODF bit is set.
2. A write to the SPICR register.

Notes: To avoid any conflicts in an application with multiple slaves, the \overline{SS} pin must be pulled high during the MODF bit clearing sequence. The SPE and MSTR bits may be restored to their original state during or after this clearing sequence.

Hardware does not allow the user to set the SPE and MSTR bits while the MODF bit is set except in the MODF bit clearing sequence.

In a slave device, the MODF bit can not be set, but in a multi master configuration the Device can be in slave mode with the MODF bit set.

The MODF bit indicates that there might have been a multi-master conflict and allows software to handle this using an interrupt routine and either perform to a reset or return to an application default state.

11.4.5.2 Overrun Condition (OVR)

An overrun condition occurs, when the master device has sent a data byte and the slave device has not cleared the SPIF bit issued from the previously transmitted byte.

When an Overrun occurs:

- The OVR bit is set and an interrupt request is generated if the SPIE bit is set.

In this case, the receiver buffer contains the byte sent after the SPIF bit was last cleared. A read to the SPIDR register returns this byte. All other bytes are lost.

The OVR bit is cleared by reading the SPICSR register.

11.4.5.3 Write Collision Error (WCOL)

A write collision occurs when the software tries to write to the SPIDR register while a data transfer is taking place with an external device. When this happens, the transfer continues uninterrupted; and the software write will be unsuccessful.

Write collisions can occur both in master and slave mode. See also [Section 11.4.3.2 Slave Select Management](#).

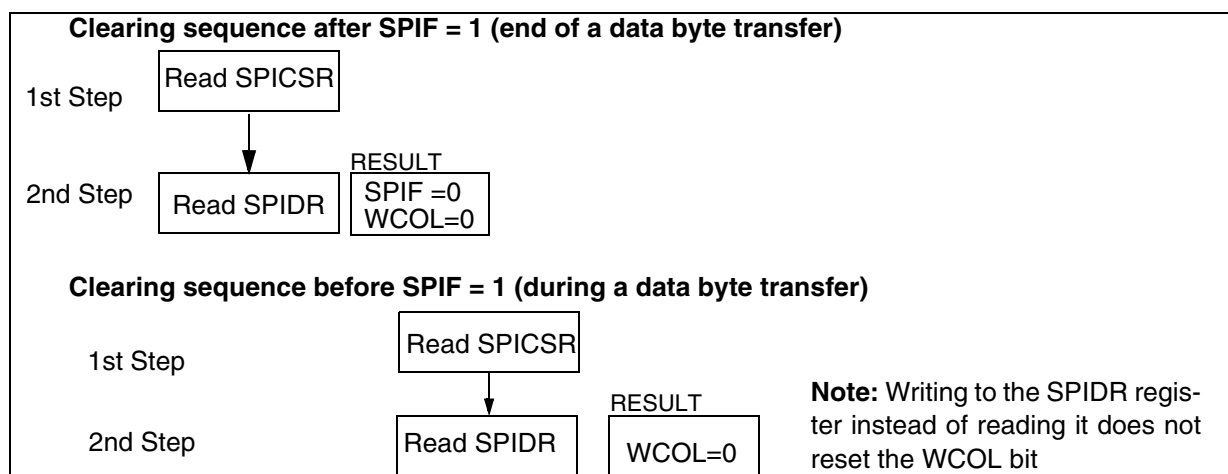
Note: a "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the CPU operation.

The WCOL bit in the SPICSR register is set if a write collision occurs.

No SPI interrupt is generated when the WCOL bit is set (the WCOL bit is a status flag only).

Clearing the WCOL bit is done through a software sequence (see [Figure 46](#)).

Figure 46. Clearing the WCOL bit (Write Collision Flag) Software Sequence



13 ELECTRICAL CHARACTERISTICS

13.1 PARAMETER CONDITIONS

Unless otherwise specified, all voltages are referred to V_{SS} .

13.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A=25^{\circ}\text{C}$ and $T_A=T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\Sigma$).

13.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A=25^{\circ}\text{C}$, $V_{DD}=5\text{V}$ (for the $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ voltage range) and $V_{DD}=3.3\text{V}$ (for the $3\text{V} \leq V_{DD} \leq 4\text{V}$ voltage range). They are given only as design guidelines and are not tested.

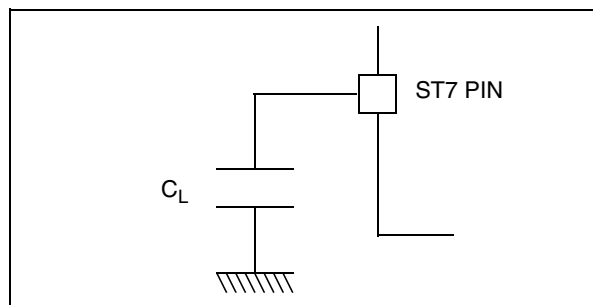
13.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

13.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 49](#).

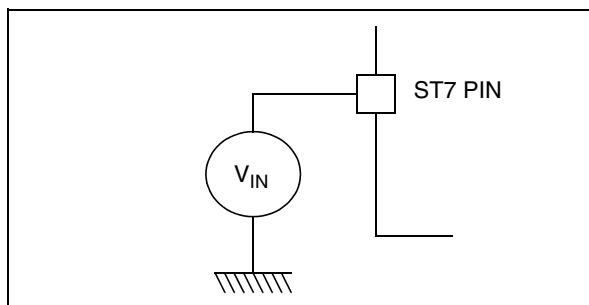
Figure 49. Pin loading conditions



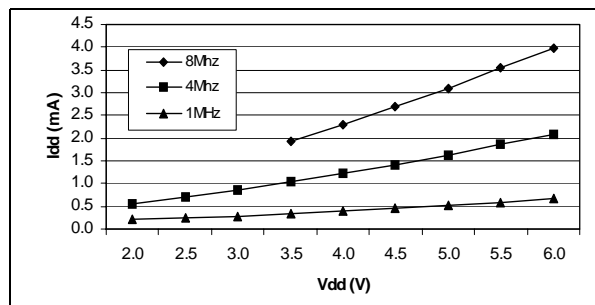
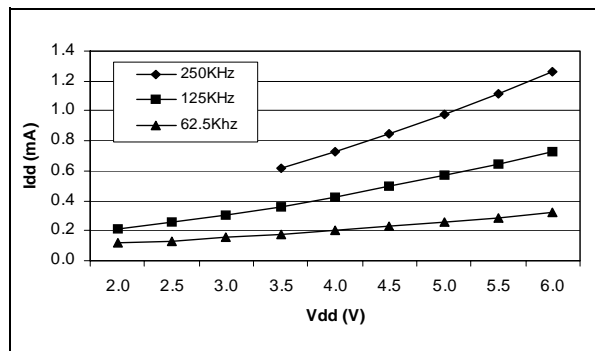
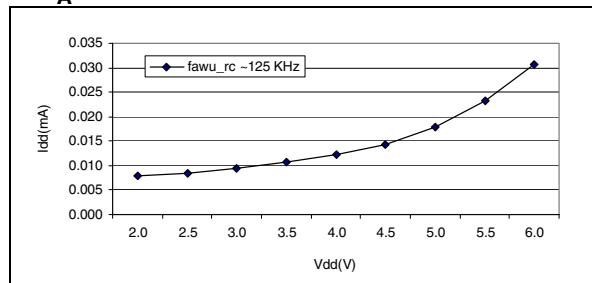
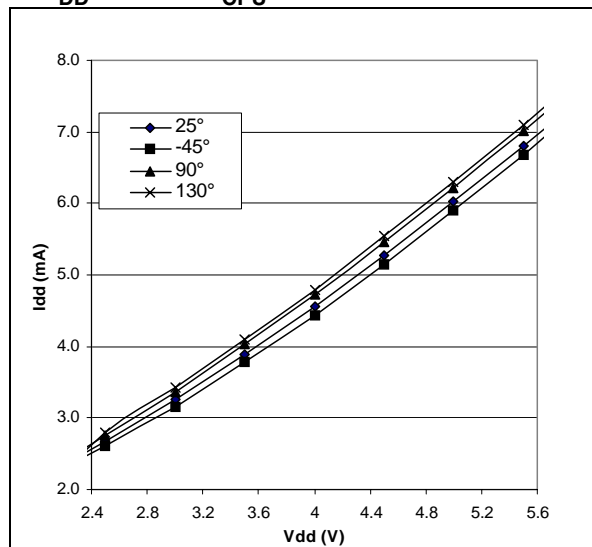
13.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 50](#).

Figure 50. Pin input voltage



SUPPLY CURRENT CHARACTERISTICS (Cont'd)

Figure 61. Typical I_{DD} in WAIT vs. f_{CPU} Figure 62. Typical I_{DD} in SLOW-WAIT vs. f_{CPU} Figure 63. Typical I_{DD} in AWUFH mode at $T_A=25^\circ\text{C}$ Figure 64. Typical I_{DD} vs. Temperature at $V_{DD} = 5\text{V}$ and $f_{CPU} = 8\text{MHz}$ 

13.4.2 On-chip peripherals

Symbol	Parameter	Conditions		Typ	Unit
$I_{DD(AT)}$	12-bit Auto-Reload Timer supply current ¹⁾	$f_{CPU}=4\text{MHz}$	$V_{DD}=3.0\text{V}$	300	μA
		$f_{CPU}=8\text{MHz}$	$V_{DD}=5.0\text{V}$	1000	
$I_{DD(SPI)}$	SPI supply current ²⁾	$f_{CPU}=4\text{MHz}$	$V_{DD}=3.0\text{V}$	50	
		$f_{CPU}=8\text{MHz}$	$V_{DD}=5.0\text{V}$	300	
$I_{DD(ADC)}$	ADC supply current when converting ³⁾	$f_{ADC}=4\text{MHz}$	$V_{DD}=3.0\text{V}$	250	
			$V_{DD}=5.0\text{V}$	1100	

1. Data based on a differential I_{DD} measurement between reset configuration (timer stopped) and a timer running in PWM mode at $f_{CPU}=8\text{MHz}$.

2. Data based on a differential I_{DD} measurement between reset configuration and a permanent SPI master communication (data sent equal to 55h).

3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions with amplifier off.

13.7 EMC CHARACTERISTICS

Susceptibility tests are performed on a sample basis during product characterization.

13.7.1 Functional EMS (Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

13.7.1.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical applica-

tion environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD}=5V$, $T_A=+25^{\circ}C$, $f_{OSC}=8MHz$ conforms to IEC 1000-4-2	3B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	$V_{DD}=5V$, $T_A=+25^{\circ}C$, $f_{OSC}=8MHz$ conforms to IEC 1000-4-4	3B

13.7.2 Electro Magnetic Interference (EMI)

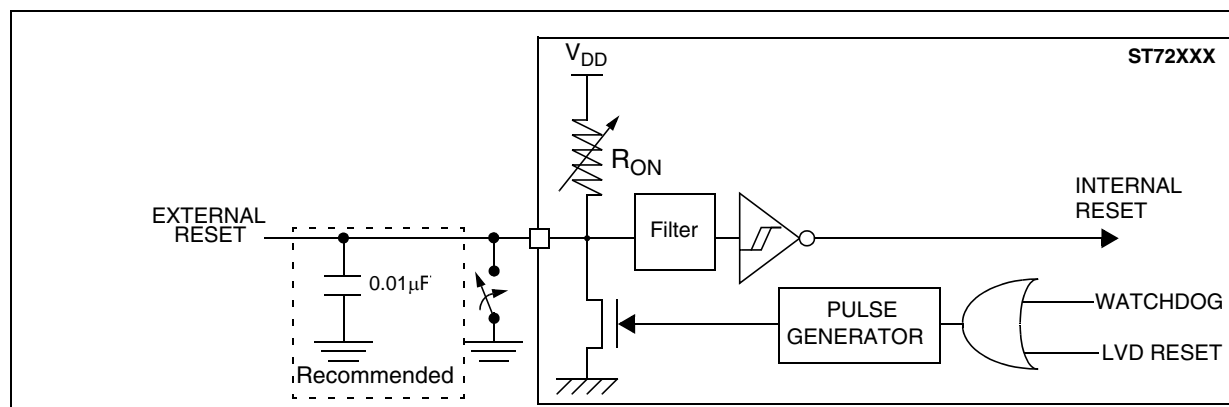
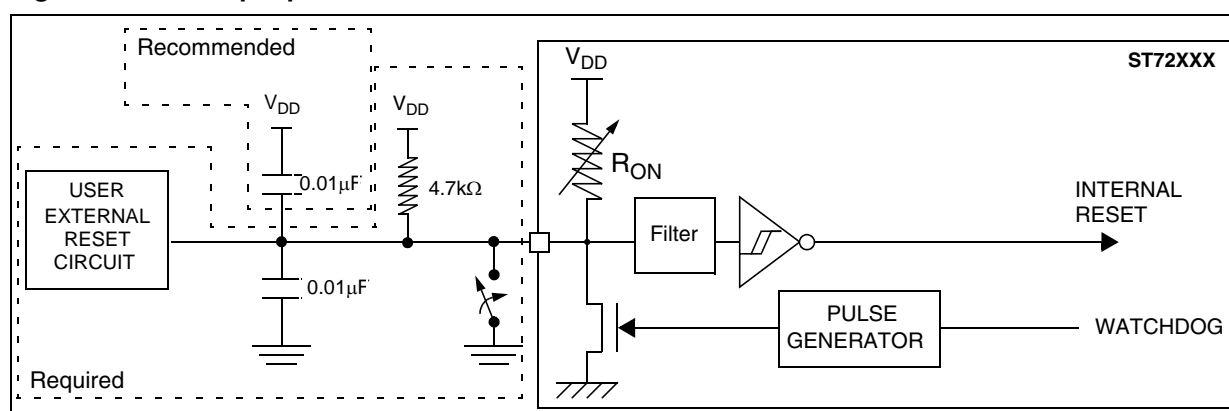
Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f _{OSC} /f _{CPU}]		Unit
				8/4MHz	16/8MHz	
S _{EMI}	Peak level	V _{DD} =5V, T _A =+25°C, SO20 package, conforming to SAE J 1752/3	0.1MHz to 30MHz	9	17	dBμV
			30MHz to 130MHz	31	36	
			130MHz to 1GHz	25	27	
			SAE EMI Level	3.5	4	-

Notes:

1. Data based on characterization results, not tested in production.

CONTROL PIN CHARACTERISTICS (Cont'd)

Figure 82. $\overline{\text{RESET}}$ pin protection when LVD is enabled.¹⁾²⁾³⁾⁴⁾⁵⁾Figure 83. $\overline{\text{RESET}}$ pin protection when LVD is disabled.¹⁾²⁾³⁾

1. The reset network protects the device against parasitic resets.
2. The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
3. Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in [section 13.9.1 on page 110](#). Otherwise the reset will not be taken into account internally.
4. Because the reset circuit is designed to allow the internal RESET to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin (by an external pull-up for example) is less than the absolute maximum value specified for $I_{INJ}(\overline{\text{RESET}})$ in [section 13.2.2 on page 92](#).
5. When the LVD is enabled, it is mandatory not to connect a pull-up resistor and a capacitor to V_{DD} on the $\overline{\text{RESET}}$ pin.

PACKAGE CHARACTERISTICS (Cont'd)**Table 21. THERMAL CHARACTERISTICS**

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient) SO20 DIP20	125 TBD	°C/W
P_D	Power dissipation ¹⁾	500	mW
T_{Jmax}	Maximum junction temperature ²⁾	150	°C

Notes:

1. The power dissipation is obtained from the formula $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD} \times V_{DD}$) and P_{PORT} is the port power dissipation determined by the user.

2. The average chip-junction temperature can be obtained from the formula $T_J = T_A + P_D \times R_{thJA}$.

OPTION BYTES (Cont'd)

OPTION BYTE 1

OPT7 = **PLLx4x8** *PLL Factor selection.*

0: PLLx4

1: PLLx8

OPT6 = **PLLOFF** *PLL disable.*

0: PLL enabled

1: PLL disabled (by-passed)

OPT5 = **PLL32OFF** *32MHz PLL disable.*

0: PLL32 enabled

1: PLL32 disabled (by-passed)

OPT4 = **OSC RC** *Oscillator selection*

0: RC oscillator on

1: RC oscillator off

Note: 1% RC oscillator available on ST7LITE15 and ST7LITE19 devices only

OPT3:2 = **LVD[1:0]** *Low voltage detection selection*

These option bits enable the LVD block with a selected threshold as shown in [Table 22](#).

Table 22. LVD Threshold Configuration

Configuration	LVD1	LVD0
LVD Off	1	1
Highest Voltage Threshold (~4.1V)	1	0
Medium Voltage Threshold (~3.5V)	0	1
Lowest Voltage Threshold (~2.8V)	0	0

OPT1 = **WDG SW** *Hardware or Software Watchdog*

This option bit selects the watchdog type.

0: Hardware (watchdog always enabled)

1: Software (watchdog to be enabled by software)

OPT0 = **WDG HALT** *Watchdog Reset on Halt*

This option bit determines if a RESET is generated when entering HALT mode while the Watchdog is active.

0: No Reset generation when entering Halt mode

1: Reset generation when entering Halt mode

Table 23. List of valid option combinations

Operating conditions		Option Bits				
V _{DD} range	Clock Source	PLL	Typ f _{CPU}	OSC	PLLOFF	PLLx4x8
2.4V - 3.3V	Internal RC 1% ¹⁾	off	0.7MHz @3V	0	1	1
		x4	2.8MHz @3V	0	0	0
		x8	-	-	-	-
	External clock or oscillator (depending on OPT6:4 selection)	off	0-4MHz	1	1	1
		x4	4MHz	1	0	0
		x8	-	-	-	-
3.3V - 5.5V	Internal RC 1% ¹⁾	off	1MHz @5V	0	1	1
		x4	-	-	-	-
		x8	8MHz @5V	0	0	1
	External clock or oscillator (depending on OPT6:4 selection)	off	0-8MHz	1	1	1
		x4	-	-	-	-
		x8	8 MHz	1	0	1

Note 1: Configuration available on ST7LITE15 and ST7LITE19 devices only

Note: see Clock Management Block diagram in [Figure 12](#)

16 IMPORTANT NOTES

16.1 EXECUTION OF BTJX INSTRUCTION

When testing the address \$FF with the "BTJT" or "BTJF" instructions, the CPU may perform an incorrect operation when the relative jump is negative and performs an address page change.

To avoid this issue, including when using a C compiler, it is recommended to never use address \$00FF as a variable (using the linker parameter for example).

16.2 ADC CONVERSION SPURIOUS RESULTS

Spurious conversions occur with a rate lower than 50 per million. Such conversions happen when the measured voltage is just between 2 consecutive digital values.

Workaround

A software filter should be implemented to remove erratic conversion results whenever they may cause unwanted consequences.

16.3 A/D CONVERTER ACCURACY FOR FIRST CONVERSION

When the ADC is enabled after being powered down (for example when waking up from HALT, ACTIVE-HALT or setting the ADON bit in the AD-CCSR register), the first conversion (8-bit or 10-bit) accuracy does not meet the accuracy specified in the datasheet.

Workaround

In order to have the accuracy specified in the datasheet, the first conversion after a ADC switch-on has to be ignored.

16.4 NEGATIVE INJECTION IMPACT ON ADC ACCURACY

Injecting a negative current on an analog input pins significantly reduces the accuracy of the AD Converter. Whenever necessary, the negative in-

jection should be prevented by the addition of a Schottky diode between the concerned I/Os and ground.

Injecting a negative current on digital input pins degrades ADC accuracy especially if performed on a pin close to ADC channel in use.

16.5 CLEARING ACTIVE INTERRUPTS OUTSIDE INTERRUPT ROUTINE

When an active interrupt request occurs at the same time as the related flag or interrupt mask is being cleared, the CC register may be corrupted.

Concurrent interrupt context

The symptom does not occur when the interrupts are handled normally, i.e. when:

- The interrupt request is cleared (flag reset or interrupt mask) within its own interrupt routine
- The interrupt request is cleared (flag reset or interrupt mask) within any interrupt routine
- The interrupt request is cleared (flag reset or interrupt mask) in any part of the code while this interrupt is disabled

If these conditions are not met, the symptom can be avoided by implementing the following sequence:

Perform SIM and RIM operation before and after resetting an active interrupt request

Ex:

SIM

reset flag or interrupt mask

RIM

16.6 USING PB4 AS EXTERNAL INTERRUPT

PB4 cannot be used as an external interrupt in HALT mode because the port pin PB4 is not active in this mode.