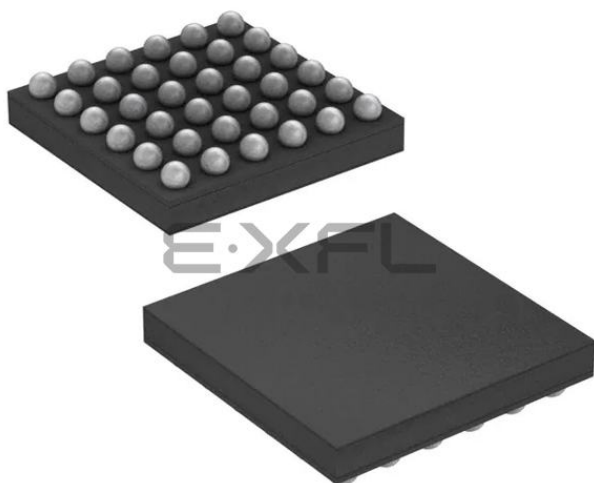




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	260
Total RAM Bits	-
Number of I/O	23
Number of Gates	10000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-20°C ~ 85°C (TJ)
Package / Case	36-WFBGA, CSPBGA
Supplier Device Package	36-UCSP (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln010v5-ucg36

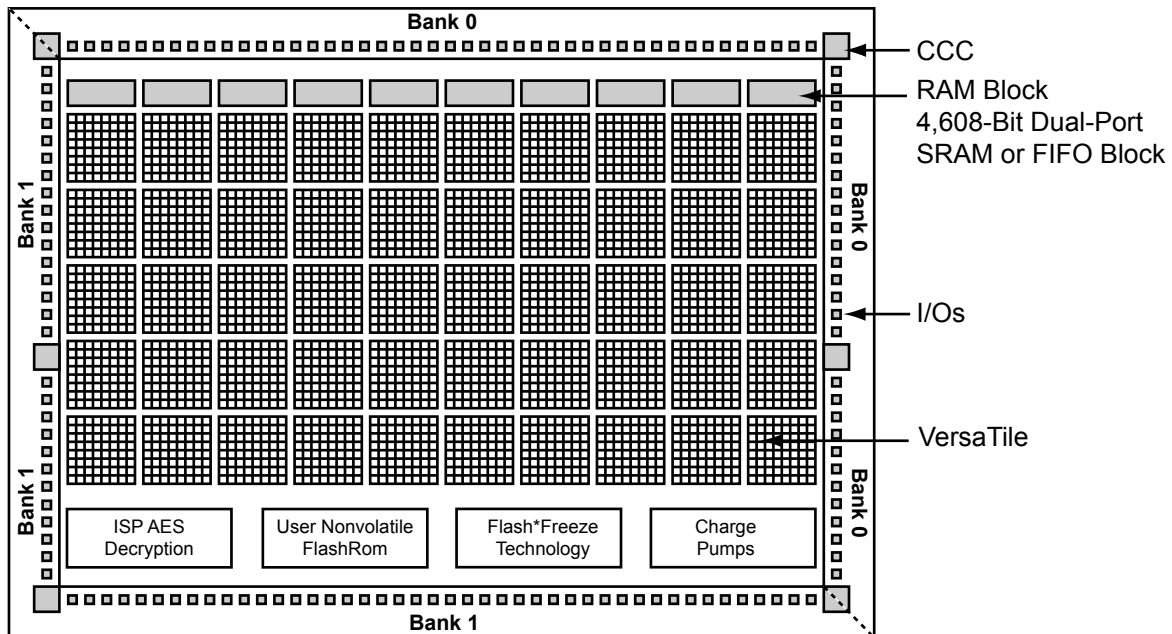


Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125)

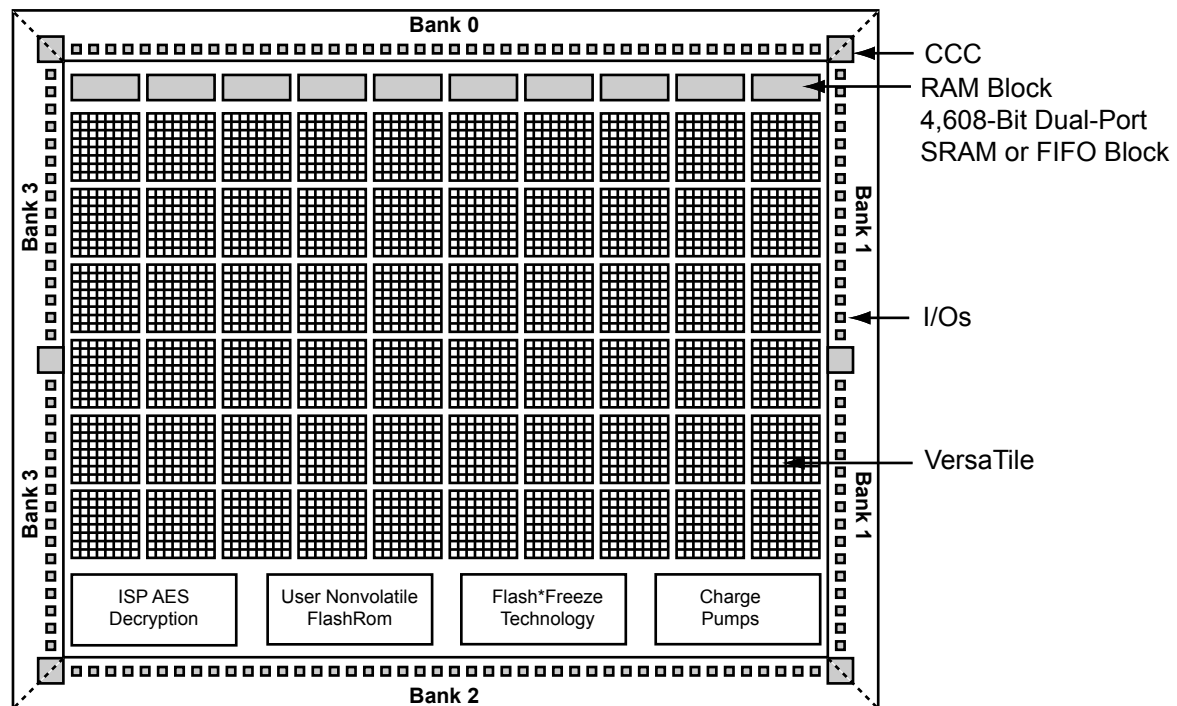


Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)

2 – IGLOO nano DC and Switching Characteristics

General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash*Freeze bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, and hot-swap I/O capability. Refer to "IGLOO nano Ordering Information" on page IV for more information.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI ¹	I/O input voltage	–0.3 V to 3.6 V	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.
2. For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (^\circ\text{C/W)}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{20.5^\circ\text{C/W}} = 1.46 \text{ W}$$

EQ 2

Table 2-5 • Package Thermal Resistivities

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Chip Scale Package (CSP)	36	TBD	TBD	TBD	TBD	C/W
	81	TBD	TBD	TBD	TBD	C/W
Quad Flat No Lead (QFN)	48	TBD	TBD	TBD	TBD	C/W
	68	TBD	TBD	TBD	TBD	C/W
	100	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425 \text{ V}$)
For IGLOO nano V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Array Voltage V_{CC} (V)	Junction Temperature ($^\circ\text{C}$)						
	-40°C	-20°C	0°C	25°C	70°C	85°C	100°C
1.425	0.947	0.956	0.965	0.978	1.000	1.009	1.013
1.5	0.875	0.883	0.892	0.904	0.925	0.932	0.937
1.575	0.821	0.829	0.837	0.848	0.868	0.875	0.879

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode*

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	μA

Note: $*I_{DD} = N_{BANKS} * I_{CCI}$

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Shutdown Mode

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	0	0	0	μA

Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode¹

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
ICCA Current²								
Typical (25°C)	1.2 V	3.7	5	5	10	13	18	μA
	1.5 V	8	14	14	20	28	44	μA
ICCI or JTAG Current								
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	μA

Notes:

1. $IDD = N_{BANKS} * ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC, VCCPLL, and VPUMP currents.

**Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices
For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

Parameter	Definition	Device-Specific Dynamic Power ($\mu\text{W}/\text{MHz}$)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	2.829	2.875	1.728	0	0	0
PAC2	Clock contribution of a Global Spine	1.731	1.265	1.268	2.562	2.562	1.685
PAC3	Clock contribution of a VersaTile row	0.957	0.963	0.967	0.862	0.862	0.858
PAC4	Clock contribution of a VersaTile used as a sequential module	0.098	0.098	0.098	0.094	0.094	0.091
PAC5	First contribution of a VersaTile used as a sequential module	0.045					
PAC6	Second contribution of a VersaTile used as a sequential module	0.186					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11					
PAC8	Average contribution of a routing net	0.45					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9					
PAC11	Average contribution of a RAM block during a read operation	25.00			N/A		
PAC12	Average contribution of a RAM block during a write operation	30.00			N/A		
PAC13	Dynamic contribution for PLL	2.10			N/A		

**Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO nano Devices
For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

Parameter	Definition	Device-Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8					
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7					
PDC4 ¹	Static PLL contribution	0.90			N/A		
PDC5	Bank quiescent power (VCCI-dependent) ²	See Table 2-12 on page 2-8					

Notes:

1. Minimum contribution of the PLL when running at lowest frequency.
2. For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.

Detailed I/O DC Characteristics

Table 2-27 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF

Table 2-28 • I/O Output Buffer Maximum Resistances ¹

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range	100 μ A	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS ⁴	1 mA	315	315
1.2 V LVCMOS Wide Range ⁴	100 μ A	315	315

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models posted at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCI}max - V_{OHspec}) / I_{OHspec}$
4. Applicable to IGLOO nano V2 devices operating at $V_{CCI} \geq V_{CC}$.

3.3 V LVCMOS Wide Range

Table 2-40 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range

3.3 V LVCMOS Wide Range ¹	Equivalent Software Default Drive Strength Option ⁴	VIL		VIH		VOL	VOH	IOL	I _{OH}	IIL ²	IIH ³
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10

Notes:

1. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V Wide Range, as specified in the JEDEC JESD8-B specification.
2. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu A$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
5. Currents are measured at 85°C junction temperature.
6. Software default selection is highlighted in gray.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-47 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	4.13	0.19	1.10	1.24	0.66	4.01	4.13	1.73	1.74	ns
4 mA	STD	0.97	4.13	0.19	1.10	1.24	0.66	4.01	4.13	1.73	1.74	ns
8 mA	STD	0.97	3.39	0.19	1.10	1.24	0.66	3.31	3.39	1.98	2.19	ns
8 mA	STD	0.97	3.39	0.19	1.10	1.24	0.66	3.31	3.39	1.98	2.19	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-48 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.19	0.19	1.10	1.24	0.66	2.23	2.11	1.72	1.80	ns
4 mA	STD	0.97	2.19	0.19	1.10	1.24	0.66	2.23	2.11	1.72	1.80	ns
6 mA	STD	0.97	1.81	0.19	1.10	1.24	0.66	1.85	1.63	1.97	2.26	ns
8 mA	STD	0.97	1.81	0.19	1.10	1.24	0.66	1.85	1.63	1.97	2.26	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Asynchronous Preset

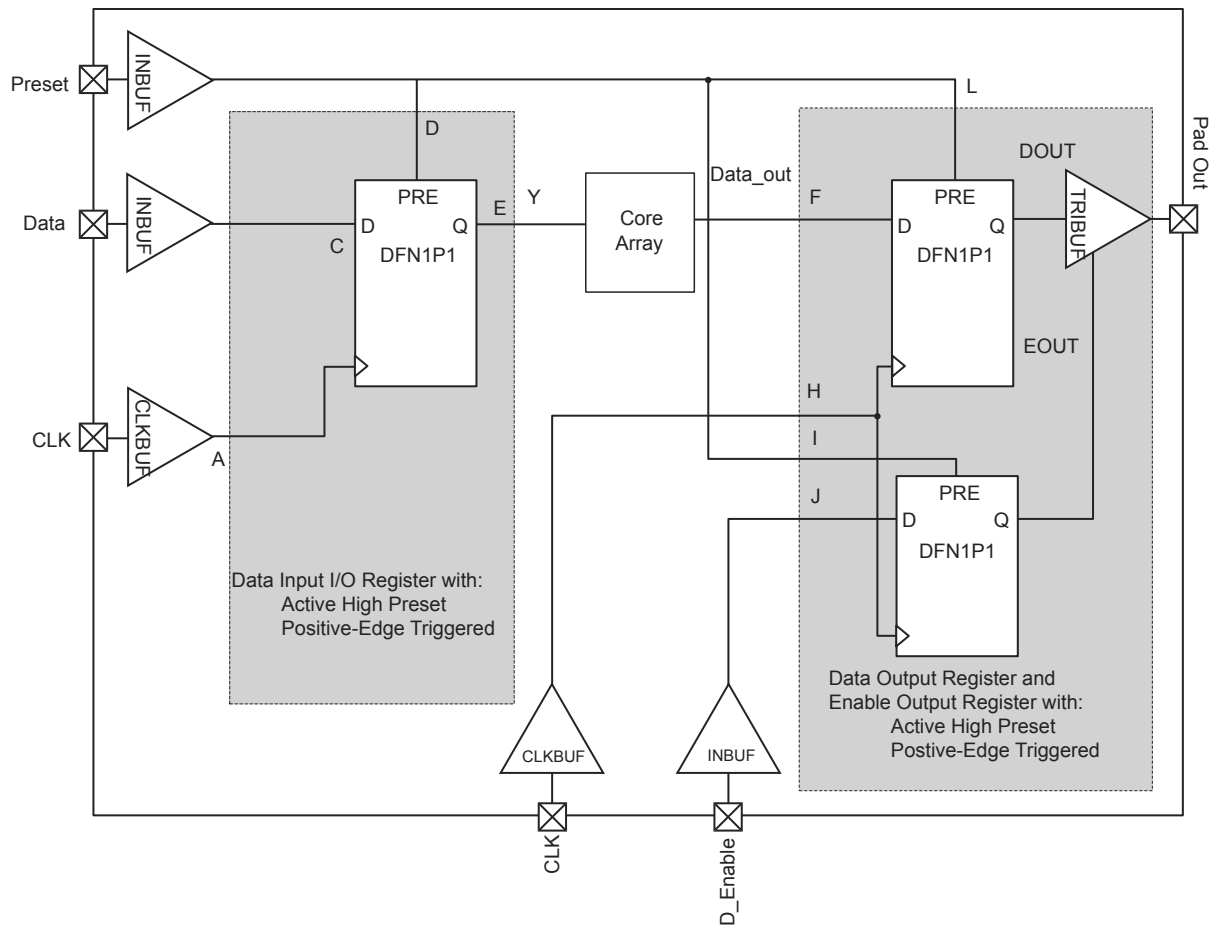


Figure 2-12 • Timing Model of Registered I/O Buffers with Asynchronous Preset

Input Register

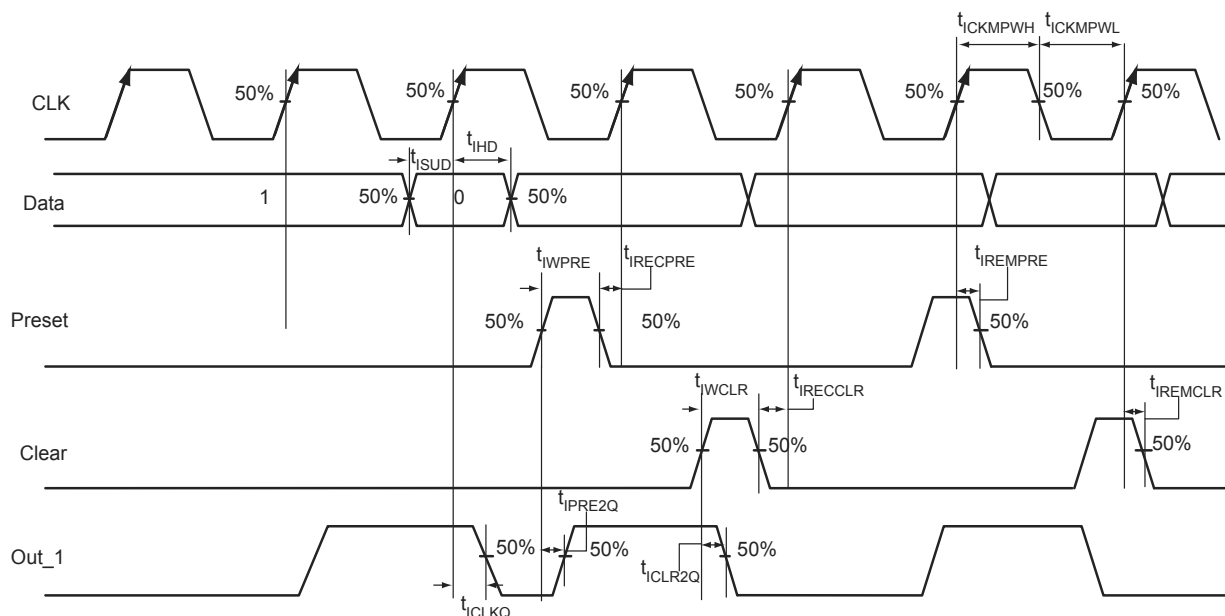


Figure 2-14 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-72 • Input Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

DDR Module Specifications

Note: DDR is not supported for AGLN010, AGLN015, and AGLN020 devices.

Input DDR Module

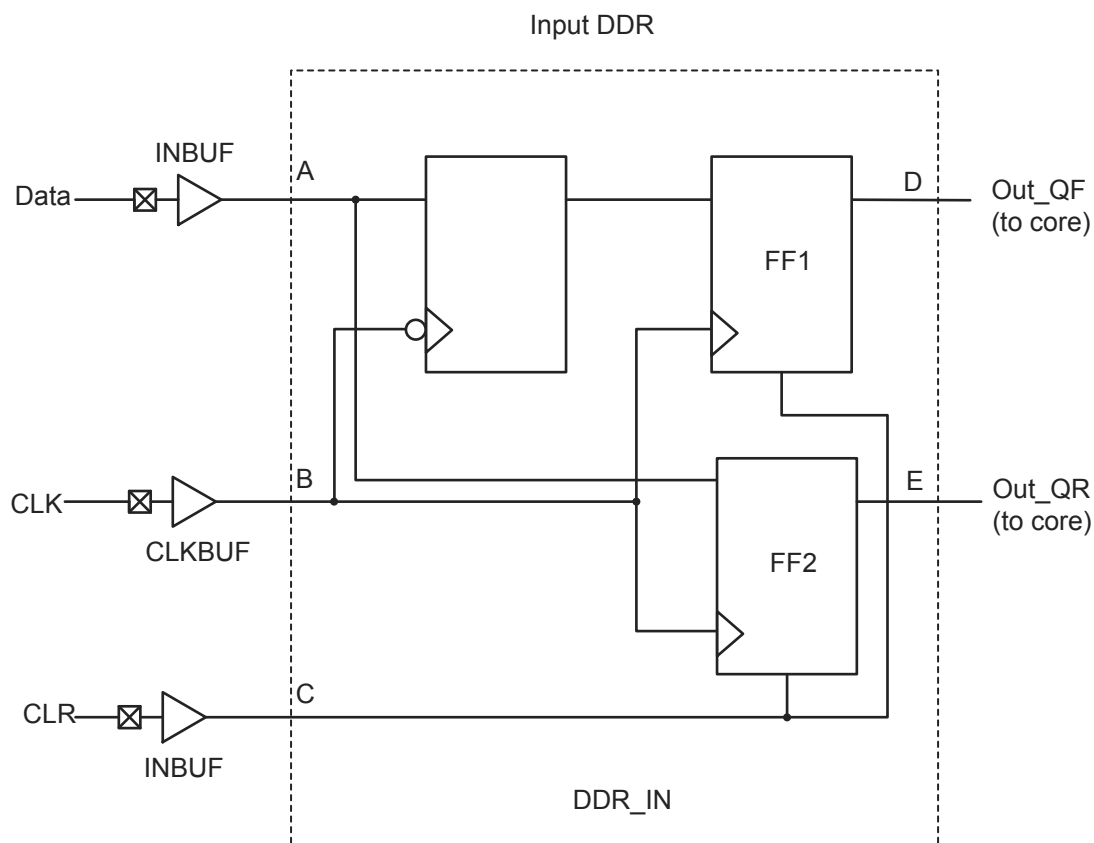


Figure 2-17 • Input DDR Timing Model

Table 2-78 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDRICKQ1}	Clock-to-Out Out_QR	B, D
t_{DDRICKQ2}	Clock-to-Out Out_QF	B, E
t_{DDRISUD}	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B

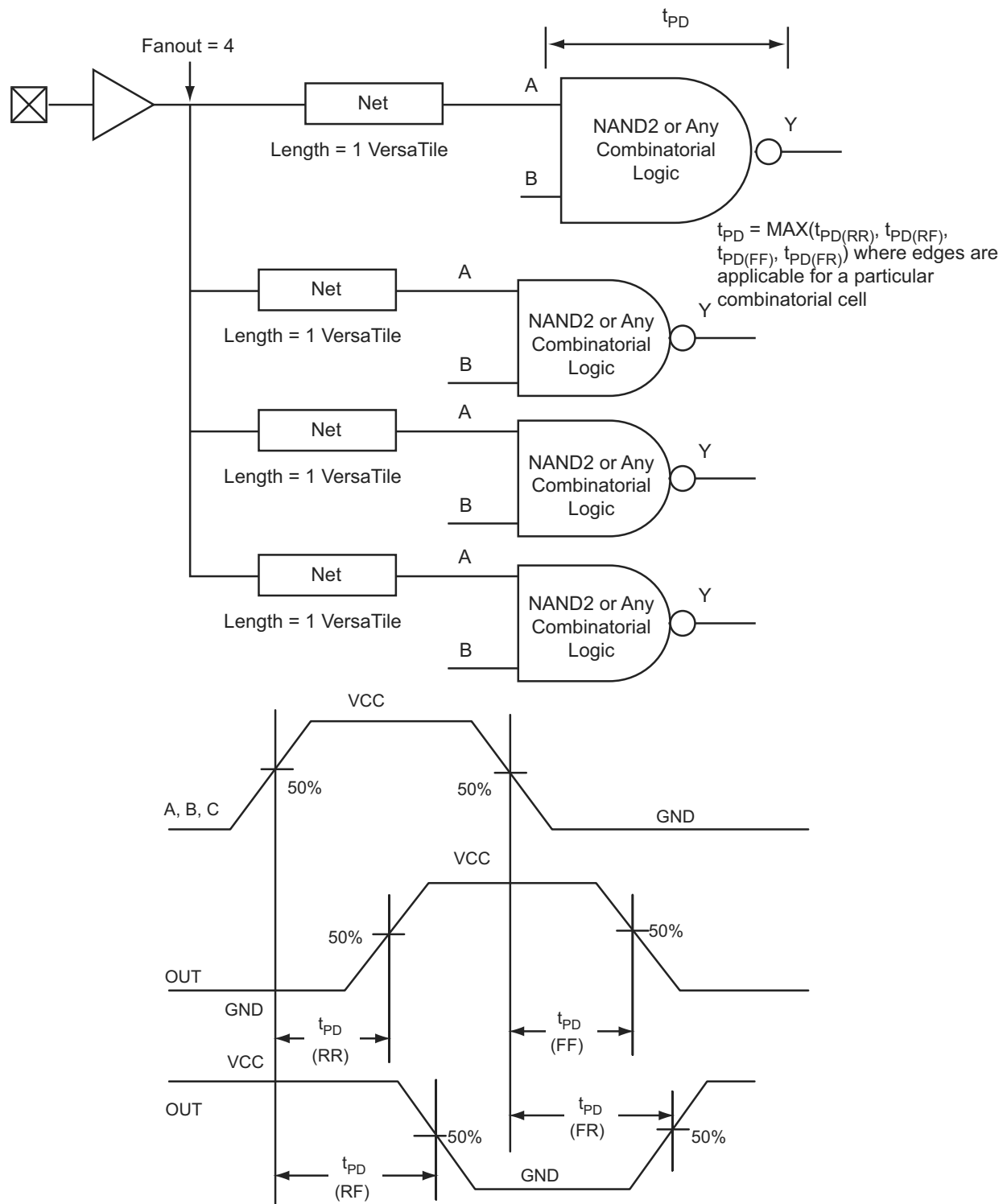


Figure 2-22 • Timing Model and Waveforms

Table 2-92 • AGLN125 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-93 • AGLN250 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-102 • RAM4K9

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.68	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{BKS}	BLK setup time	1.37	ns
t_{BKH}	BLK hold time	0.13	ns
t_{DS}	Input data (DIN) setup time	0.59	ns
t_{DH}	Input data (DIN) hold time	0.30	ns
t_{CKQ1}	Clock HIGH to new data valid on DOUT (output retained, WMODE = 0)	2.94	ns
	Clock HIGH to new data valid on DOUT (flow-through, WMODE = 1)	2.55	ns
t_{CKQ2}	Clock HIGH to new data valid on DOUT (pipelined)	1.51	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.23	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.41	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.72	ns
	RESET Low to data out Low on DOUT (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	ns
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Waveforms

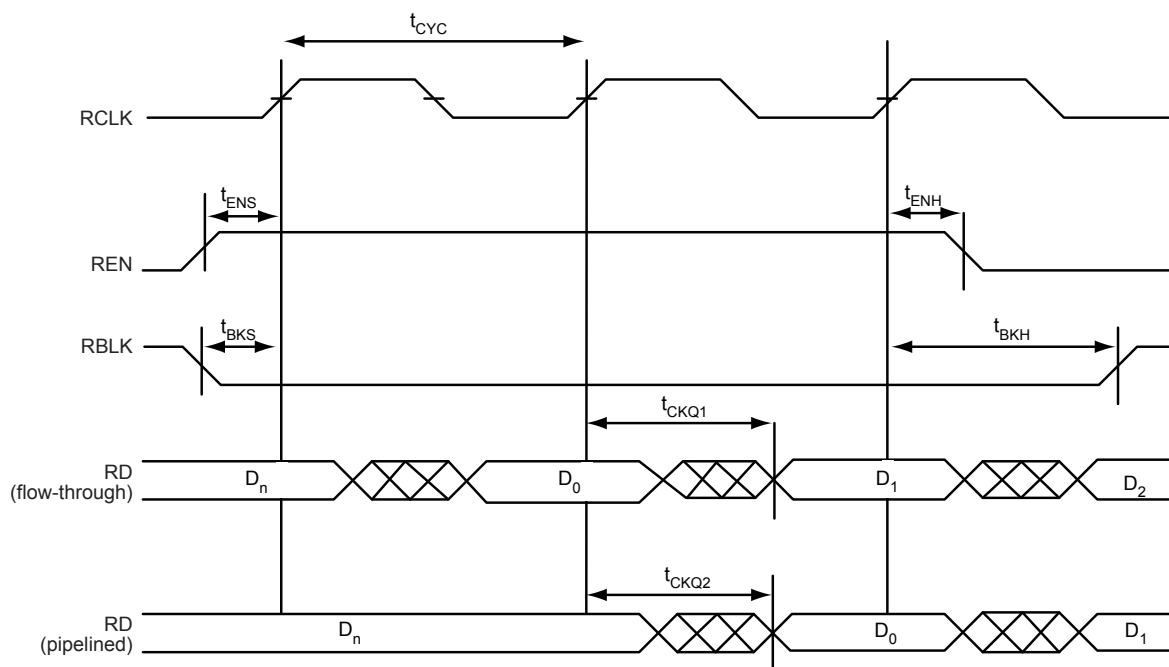


Figure 2-34 • FIFO Read

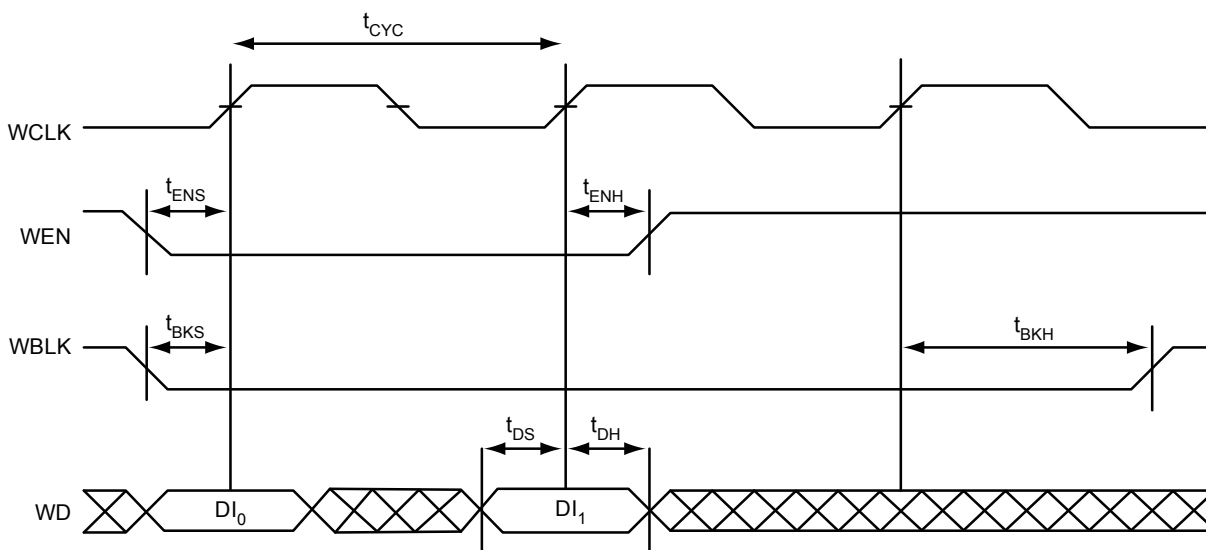


Figure 2-35 • FIFO Write

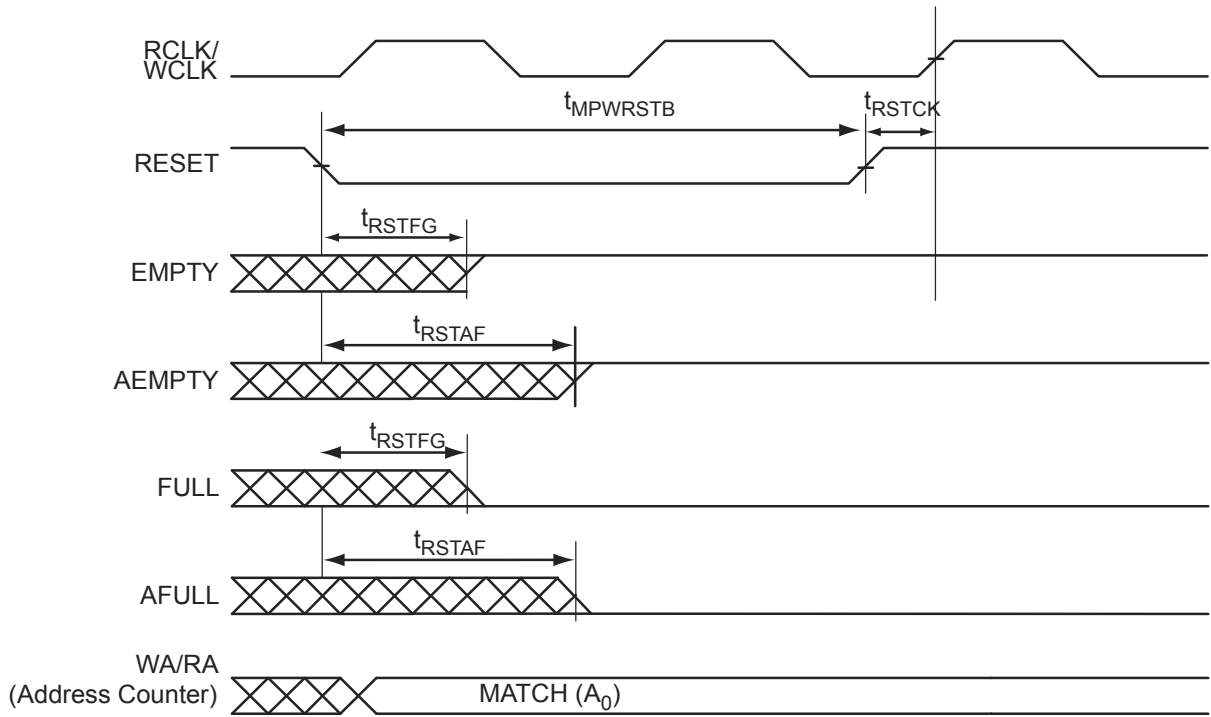


Figure 2-36 • FIFO Reset

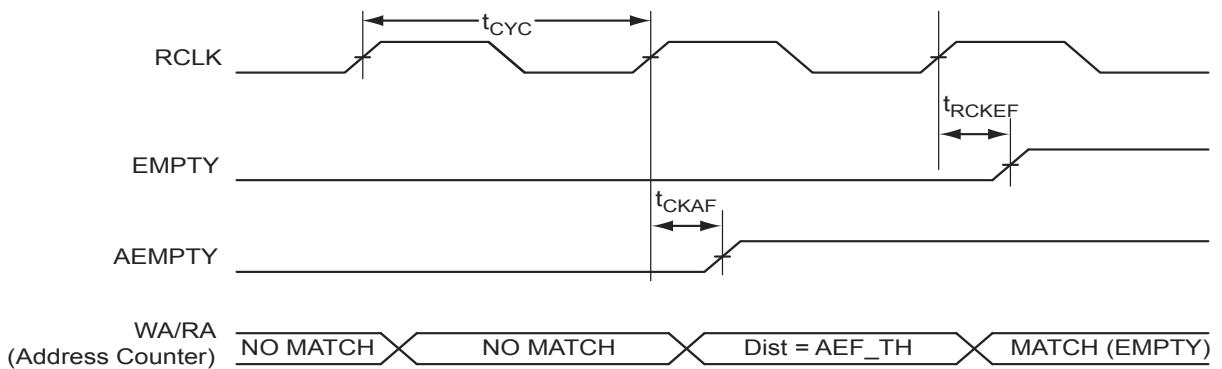


Figure 2-37 • FIFO EMPTY Flag and AEMPTY Flag Assertion

Embedded FlashROM Characteristics

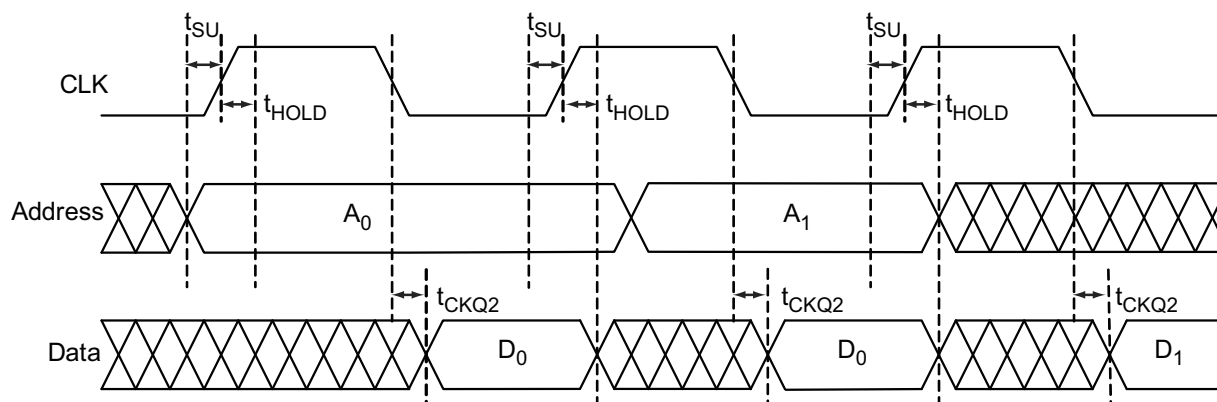


Figure 2-41 • Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-108 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	20.90	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-109 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	35.74	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

CS81	
Pin Number	AGLN030Z Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0

CS81	
Pin Number	AGLN030Z Function
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1

CS81	
Pin Number	AGLN030Z Function
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

QN48	
Pin Number	AGLN030Z Function
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	FF/IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0

QN48	
Pin Number	AGLN030Z Function
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

VQ100		VQ100		VQ100	
Pin Number	AGLN060Z Function	Pin Number	AGLN060Z Function	Pin Number	AGLN060Z Function
1	GND	35	IO62RSB1	69	IO31RSB0
2	GAA2/IO51RSB1	36	IO61RSB1	70	GBC2/IO29RSB0
3	IO52RSB1	37	VCC	71	GBB2/IO27RSB0
4	GAB2/IO53RSB1	38	GND	72	IO26RSB0
5	IO95RSB1	39	VCCIB1	73	GBA2/IO25RSB0
6	GAC2/IO94RSB1	40	IO60RSB1	74	VMV0
7	IO93RSB1	41	IO59RSB1	75	GNDQ
8	IO92RSB1	42	IO58RSB1	76	GBA1/IO24RSB0
9	GND	43	IO57RSB1	77	GBA0/IO23RSB0
10	GFB1/IO87RSB1	44	GDC2/IO56RSB1	78	GBB1/IO22RSB0
11	GFB0/IO86RSB1	45*	GDB2/IO55RSB1	79	GBB0/IO21RSB0
12	VCOMPLF	46	GDA2/IO54RSB1	80	GBC1/IO20RSB0
13	GFA0/IO85RSB1	47	TCK	81	GBC0/IO19RSB0
14	VCCPLF	48	TDI	82	IO18RSB0
15	GFA1/IO84RSB1	49	TMS	83	IO17RSB0
16	GFA2/IO83RSB1	50	VMV1	84	IO15RSB0
17	VCC	51	GND	85	IO13RSB0
18	VCCIB1	52	VPUMP	86	IO11RSB0
19	GEC1/IO77RSB1	53	NC	87	VCCIB0
20	GEB1/IO75RSB1	54	TDO	88	GND
21	GEB0/IO74RSB1	55	TRST	89	VCC
22	GEA1/IO73RSB1	56	VJTAG	90	IO10RSB0
23	GEA0/IO72RSB1	57	GDA1/IO49RSB0	91	IO09RSB0
24	VMV1	58	GDC0/IO46RSB0	92	IO08RSB0
25	GNDQ	59	GDC1/IO45RSB0	93	GAC1/IO07RSB0
26	GEA2/IO71RSB1	60	GCC2/IO43RSB0	94	GAC0/IO06RSB0
27	FF/GEB2/IO70RSB1	61	GCB2/IO42RSB0	95	GAB1/IO05RSB0
28	GEC2/IO69RSB1	62	GCA0/IO40RSB0	96	GAB0/IO04RSB0
29	IO68RSB1	63	GCA1/IO39RSB0	97	GAA1/IO03RSB0
30	IO67RSB1	64	GCC0/IO36RSB0	98	GAA0/IO02RSB0
31	IO66RSB1	65	GCC1/IO35RSB0	99	IO01RSB0
32	IO65RSB1	66	VCCIB0	100	IO00RSB0
33	IO64RSB1	67	GND		
34	IO63RSB1	68	VCC		

Note: *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin 45 in AGLN060Z-VQ100.