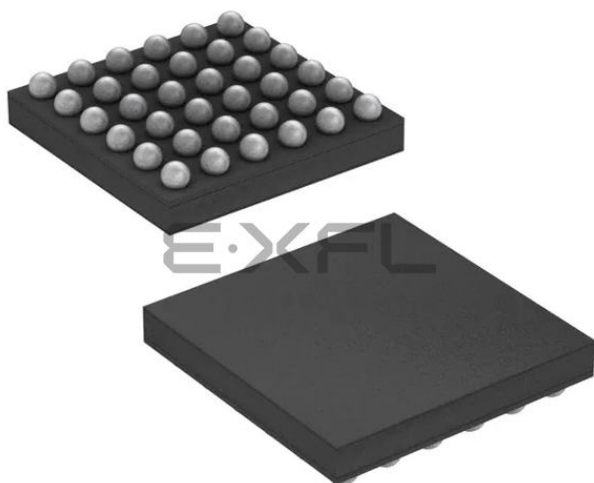




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	260
Total RAM Bits	-
Number of I/O	23
Number of Gates	10000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-WFBGA, CSPBGA
Supplier Device Package	36-UCSP (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln010v5-ucg36i

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The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% $\pm$ 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% $\times$ clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μ s (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps $\times$ 250 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

IGLOO nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

IGLOO nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.2 V, 1.2 V wide range, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V).

The I/Os are organized into banks with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the AGLN060, AGLN125, and AGLN250 devices.

IGLOO nano devices support LVTTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO nano devices support JEDEC-defined wide range I/O operation. IGLOO nano devices support both the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$ for V5 devices, and $0.75\text{ V} \pm 0.2\text{ V}$ for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

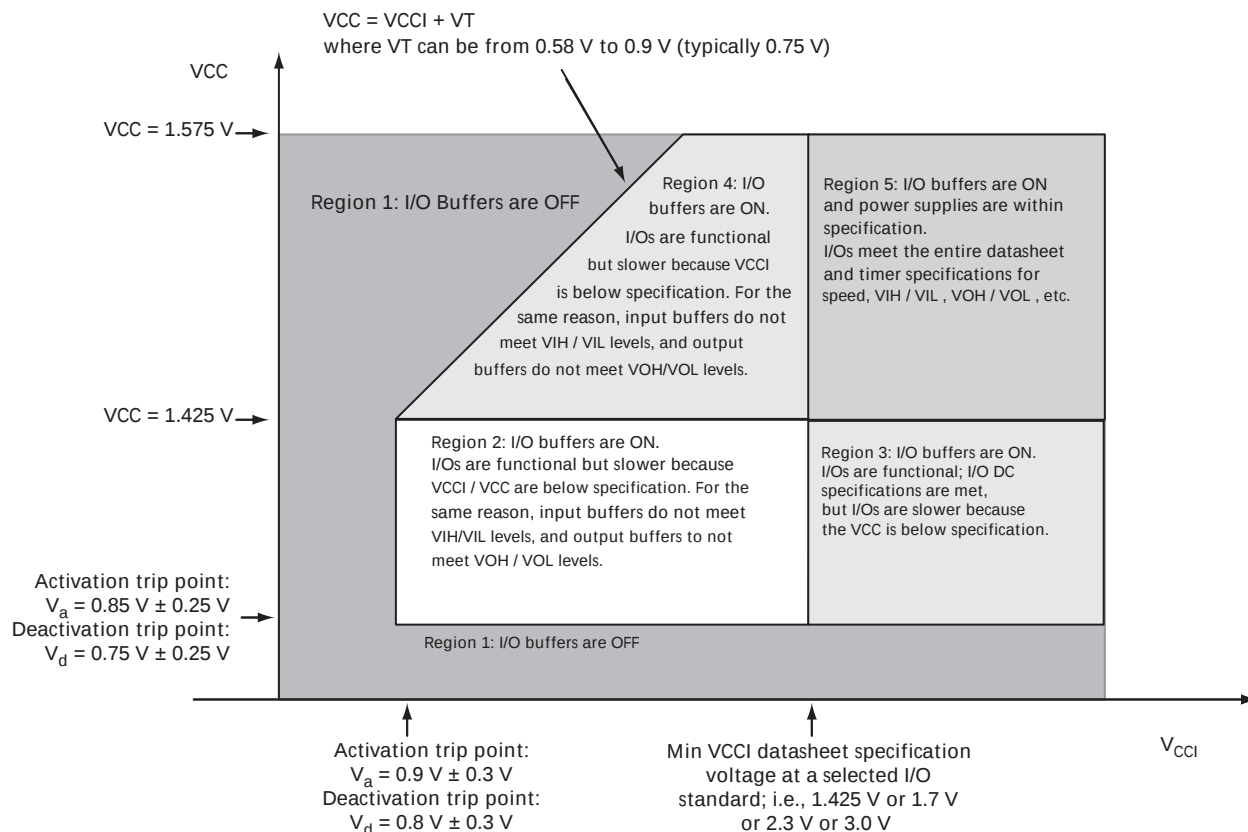


Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

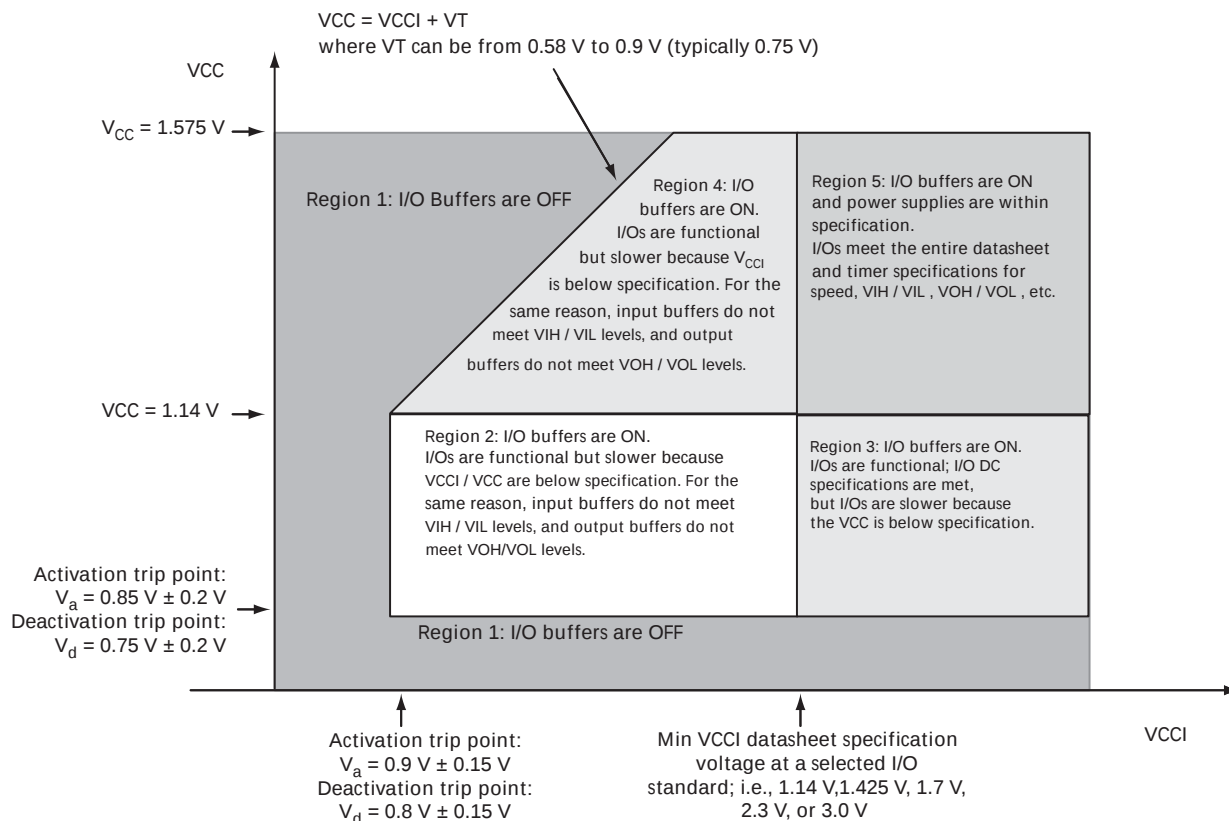


Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

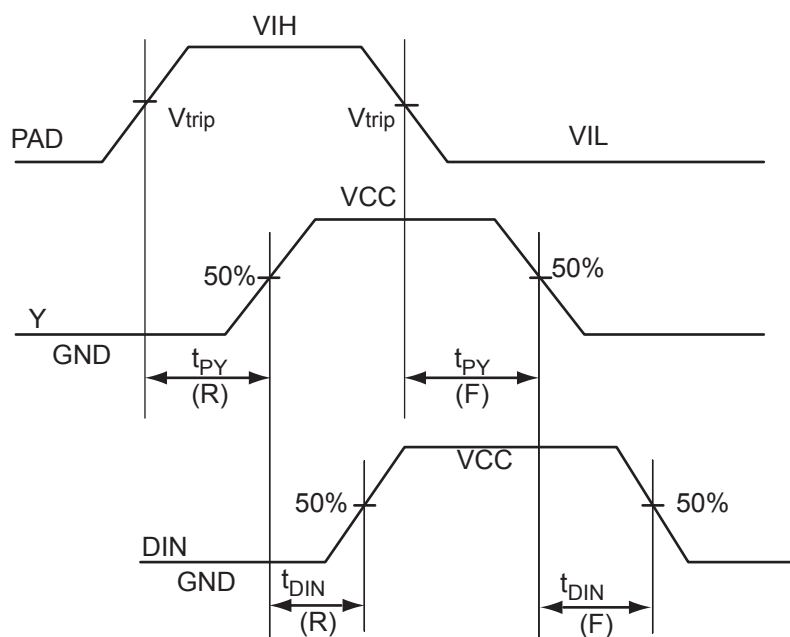
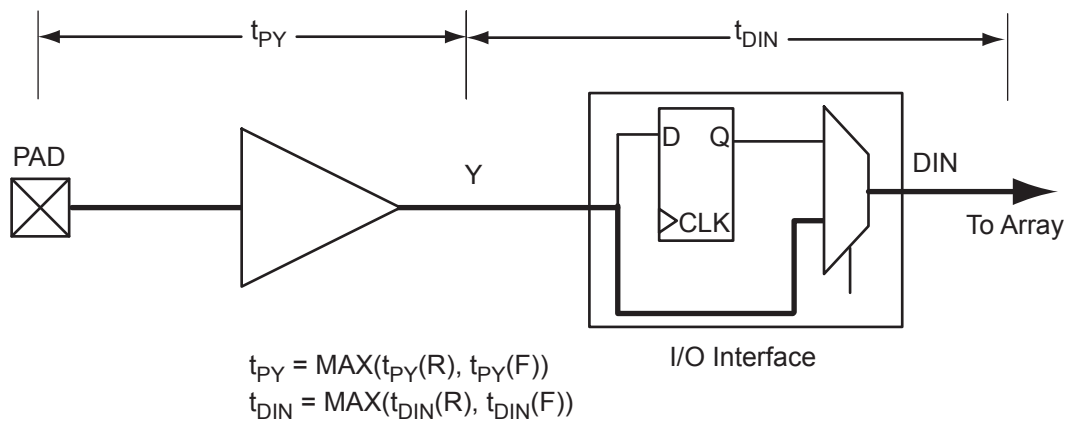


Figure 2-4 • Input Buffer Timing Model and Delays (example)

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-34 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

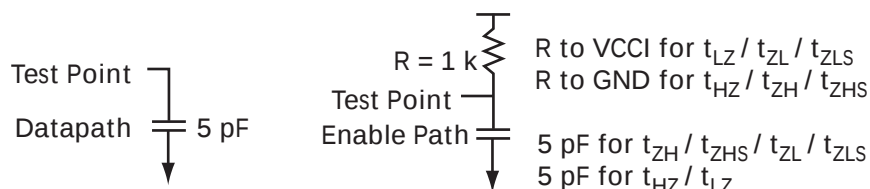


Figure 2-7 • AC Loading

Table 2-35 • 3.3 V LVTTL/LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	5

Note: *Measuring point = V_{trip} . See [Table 2-23 on page 2-20](#) for a complete table of trip points.

Applies to 1.2 V DC Core Voltage

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
4 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
6 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns
8 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
4 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
6 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
8 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

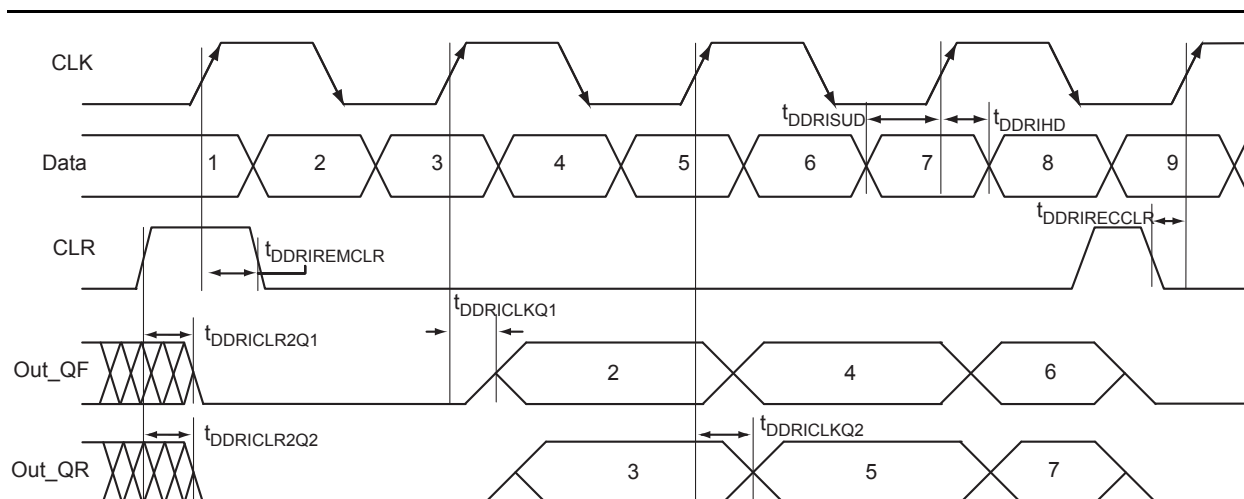


Figure 2-18 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-79 • Input DDR Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.25\text{ V}$

Parameter	Description	Std.	Units
t_{DDRCLKQ1}	Clock-to-Out Out_QR for Input DDR	0.48	ns
t_{DDRCLKQ2}	Clock-to-Out Out_QF for Input DDR	0.65	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.50	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.40	ns
t_{DDRHD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRHD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
t_{DDRWCCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Output DDR Module

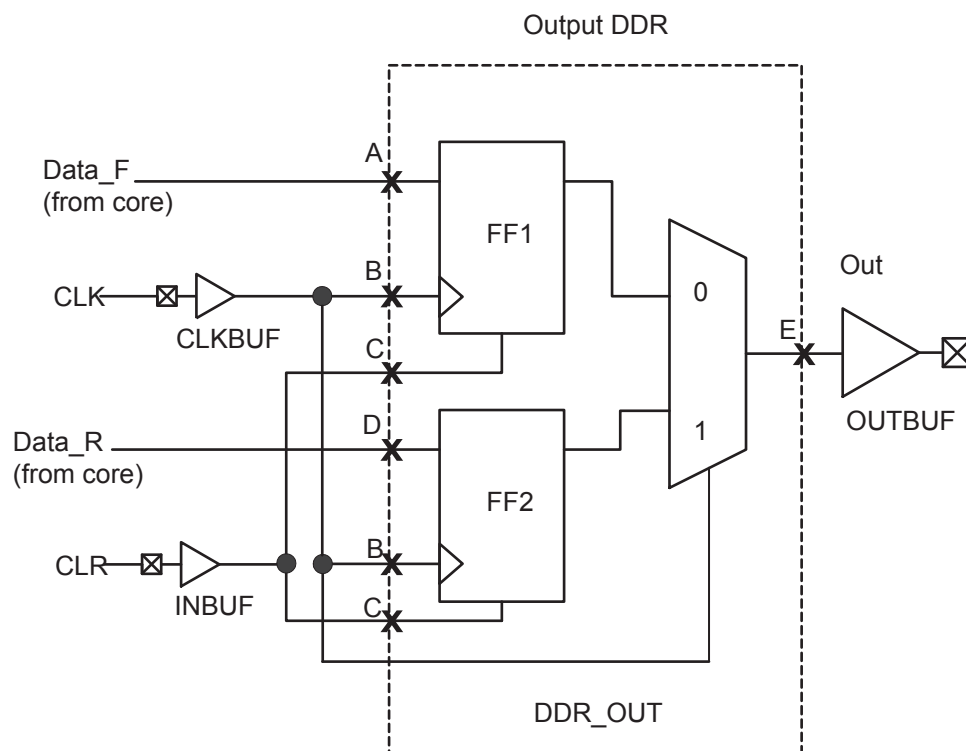


Figure 2-19 • Output DDR Timing Model

Table 2-81 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-70. Table 2-88 to Table 2-96 on page 2-68 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-88 • AGLN010 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.13	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.15	1.50	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-89 • AGLN015 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-96 • AGLN020 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.81	2.26	ns
t_{RCKH}	Input High Delay for Global Clock	1.90	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Table 2-97 • AGLN060 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

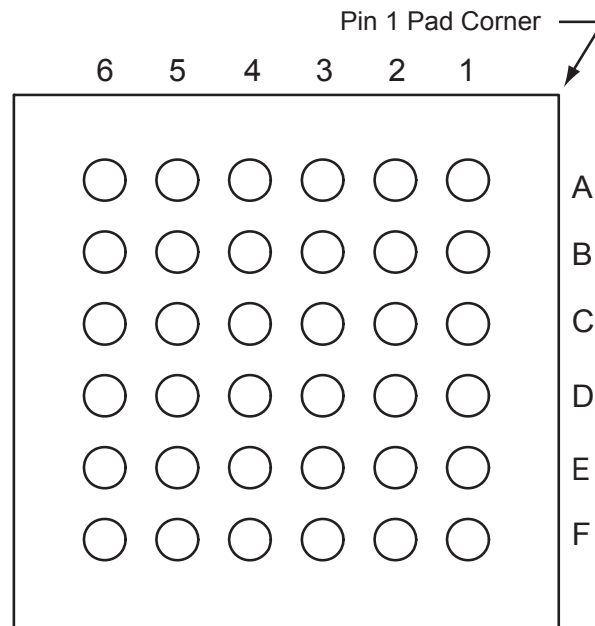
Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.42	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

4 – Package Pin Assignments

UC36



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

CS81		CS81		CS81	
Pin Number	AGLN020 Function	Pin Number	AGLN020 Function	Pin Number	AGLN020 Function
A1	IO64RSB2	E1	GEC0/IO48RSB2	J1	IO38RSB1
A2	IO54RSB2	E2	GEA0/IO47RSB2	J2	IO37RSB1
A3	IO57RSB2	E3	NC	J3	IO33RSB1
A4	IO36RSB1	E4	VCCIB1	J4	IO30RSB1
A5	IO32RSB1	E5	VCC	J5	IO27RSB1
A6	IO24RSB1	E6	VCCIB0	J6	IO23RSB1
A7	IO20RSB1	E7	NC	J7	TCK
A8	IO04RSB0	E8	GDA0/IO15RSB0	J8	TMS
A9	IO08RSB0	E9	GDC0/IO14RSB0	J9	VPUMP
B1	IO59RSB2	F1	IO46RSB2		
B2	IO55RSB2	F2	IO45RSB2		
B3	IO62RSB2	F3	NC		
B4	IO34RSB1	F4	GND		
B5	IO28RSB1	F5	VCCIB1		
B6	IO22RSB1	F6	NC		
B7	IO18RSB1	F7	NC		
B8	IO00RSB0	F8	IO16RSB0		
B9	IO03RSB0	F9	IO17RSB0		
C1	IO51RSB2	G1	IO43RSB2		
C2	IO50RSB2	G2	IO42RSB2		
C3	NC	G3	IO41RSB2		
C4	NC	G4	IO31RSB1		
C5	NC	G5	NC		
C6	NC	G6	IO21RSB1		
C7	NC	G7	NC		
C8	IO10RSB0	G8	VJTAG		
C9	IO07RSB0	G9	TRST		
D1	IO49RSB2	H1	IO40RSB2		
D2	IO44RSB2	H2	FF/IO39RSB1		
D3	NC	H3	IO35RSB1		
D4	VCC	H4	IO29RSB1		
D5	VCCIB2	H5	IO26RSB1		
D6	GND	H6	IO25RSB1		
D7	NC	H7	IO19RSB1		
D8	IO13RSB0	H8	TDI		
D9	IO12RSB0	H9	TDO		

CS81	
Pin Number	AGLN060Z Function
A1	GAA0/IO02RSB0
A2	GAA1/IO03RSB0
A3	GAC0/IO06RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO18RSB0
A7	GBB0/IO21RSB0
A8	GBA1/IO24RSB0
A9	GBA2/IO25RSB0
B1	GAA2/IO95RSB1
B2	GAB0/IO04RSB0
B3	GAC1/IO07RSB0
B4	IO08RSB0
B5	IO15RSB0
B6	GBC0/IO19RSB0
B7	GBB1/IO22RSB0
B8	IO26RSB0
B9	GBB2/IO27RSB0
C1	GAB2/IO93RSB1
C2	IO94RSB1
C3	GND
C4	IO10RSB0
C5	IO17RSB0
C6	GND
C7	GBA0/IO23RSB0
C8	GBC2/IO29RSB0
C9	IO31RSB0
D1	GAC2/IO91RSB1
D2	IO92RSB1
D3	GFA2/IO80RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO43RSB0

CS81	
Pin Number	AGLN060Z Function
D8	GCC1/IO35RSB0
D9	GCC0/IO36RSB0
E1	GFB0/IO83RSB1
E2	GFB1/IO84RSB1
E3	GFA1/IO81RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GCA1/IO39RSB0
E8	GCA0/IO40RSB0
E9	GCB2/IO42RSB0
F1 ¹	VCCPLF
F2 ¹	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO49RSB0
F8	GDC1/IO45RSB0
F9	GDC0/IO46RSB0
G1	GEA0/IO69RSB1
G2	GEC1/IO74RSB1
G3	GEB1/IO72RSB1
G4	IO63RSB1
G5	IO60RSB1
G6	IO54RSB1
G7	GDB2/IO52RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO70RSB1
H2	FF/GEB2/IO67RSB1
H3	IO65RSB1
H4	IO62RSB1
H5	IO59RSB1

CS81	
Pin Number	AGLN060Z Function
H6	IO56RSB1
H7 ²	GDA2/IO51RSB1
H8	TDI
H9	TDO
J1	GEA2/IO68RSB1
J2	GEC2/IO66RSB1
J3	IO64RSB1
J4	IO61RSB1
J5	IO58RSB1
J6	IO55RSB1
J7	TCK
J8	TMS
J9	VPUMP

Notes:

1. Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN060Z-CS81.
2. The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin H7 in AGLN060Z-CS81.

CS81		CS81		CS81	
Pin Number	AGLN125 Function	Pin Number	AGLN125 Function	Pin Number	AGLN125 Function
A1	GAA0/IO00RSB0	E1	GFB0/IO120RSB1	J1	GEA2/IO103RSB1
A2	GAA1/IO01RSB0	E2	GFB1/IO121RSB1	J2	GEC2/IO101RSB1
A3	GAC0/IO04RSB0	E3	GFA1/IO118RSB1	J3	IO97RSB1
A4	IO13RSB0	E4	VCCIB1	J4	IO93RSB1
A5	IO22RSB0	E5	VCC	J5	IO90RSB1
A6	IO32RSB0	E6	VCCIB0	J6	IO78RSB1
A7	GBB0/IO37RSB0	E7	GCA0/IO56RSB0	J7	TCK
A8	GBA1/IO40RSB0	E8	GCA1/IO55RSB0	J8	TMS
A9	GBA2/IO41RSB0	E9	GCB2/IO58RSB0	J9	VPUMP
B1	GAA2/IO132RSB1	F1*	VCCPLF		
B2	GAB0/IO02RSB0	F2*	VCOMPLF		
B3	GAC1/IO05RSB0	F3	GND		
B4	IO11RSB0	F4	GND		
B5	IO25RSB0	F5	VCCIB1		
B6	GBC0/IO35RSB0	F6	GND		
B7	GBB1/IO38RSB0	F7	GDA1/IO65RSB0		
B8	IO42RSB0	F8	GDC1/IO61RSB0		
B9	GBB2/IO43RSB0	F9	GDC0/IO62RSB0		
C1	GAB2/IO130RSB1	G1	GEA0/IO104RSB1		
C2	IO131RSB1	G2	GEC0/IO108RSB1		
C3	GND	G3	GEB1/IO107RSB1		
C4	IO15RSB0	G4	IO96RSB1		
C5	IO28RSB0	G5	IO92RSB1		
C6	GND	G6	IO72RSB1		
C7	GBA0/IO39RSB0	G7	GDB2/IO68RSB1		
C8	GBC2/IO45RSB0	G8	VJTAG		
C9	IO47RSB0	G9	TRST		
D1	GAC2/IO128RSB1	H1	GEA1/IO105RSB1		
D2	IO129RSB1	H2	FF/GEB2/IO102RSB1		
D3	GFA2/IO117RSB1	H3	IO99RSB1		
D4	VCC	H4	IO94RSB1		
D5	VCCIB0	H5	IO91RSB1		
D6	GND	H6	IO81RSB1		
D7	GCC2/IO59RSB0	H7	GDA2/IO67RSB1		
D8	GCC1/IO51RSB0	H8	TDI		
D9	GCC0/IO52RSB0	H9	TDO		

Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN125-CS81.

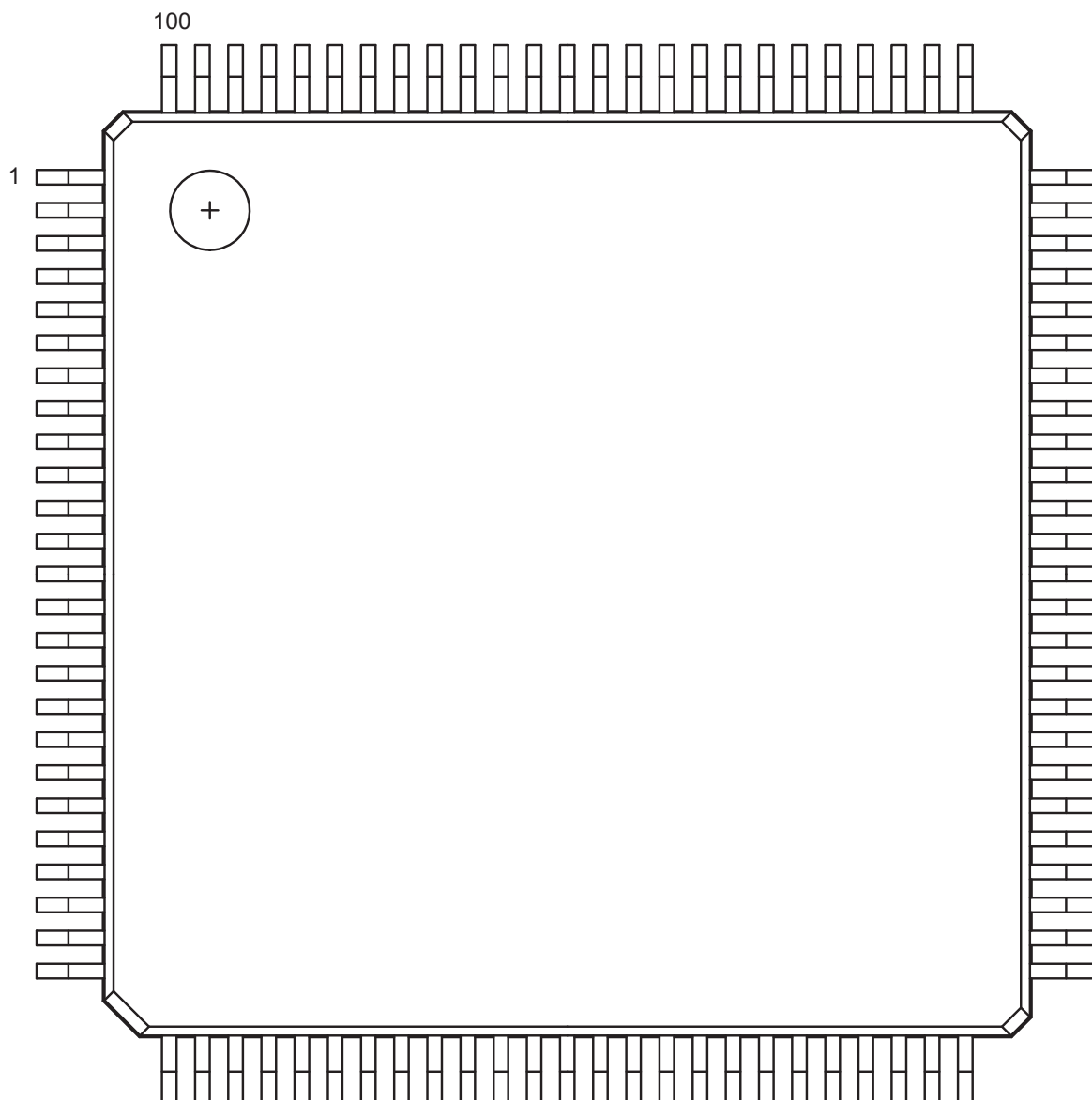
QN48	
Pin Number	AGLN010 Function
1	GEC0/IO37RSB1
2	IO36RSB1
3	GEA0/IO34RSB1
4	IO22RSB1
5	GND
6	VCCIB1
7	IO24RSB1
8	IO33RSB1
9	IO26RSB1
10	IO32RSB1
11	IO27RSB1
12	IO29RSB1
13	IO30RSB1
14	FF/IO31RSB1
15	IO28RSB1
16	IO25RSB1
17	IO23RSB1
18	VCC
19	VCCIB1
20	IO17RSB1
21	IO14RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO11RSB0
30	IO10RSB0
31	IO09RSB0
32	IO08RSB0
33	VCCIB0
34	GND
35	VCC

QN48	
Pin Number	AGLN010 Function
36	IO07RSB0
37	IO06RSB0
38	GDA0/IO05RSB0
39	IO03RSB0
40	GDC0/IO01RSB0
41	IO12RSB1
42	IO13RSB1
43	IO15RSB1
44	IO16RSB1
45	IO18RSB1
46	IO19RSB1
47	IO20RSB1
48	IO21RSB1

QN68	
Pin Number	AGLN015 Function
1	IO60RSB2
2	IO54RSB2
3	IO52RSB2
4	IO50RSB2
5	IO49RSB2
6	GEC0/IO48RSB2
7	GEA0/IO47RSB2
8	VCC
9	GND
10	VCCIB2
11	IO46RSB2
12	IO45RSB2
13	IO44RSB2
14	IO43RSB2
15	IO42RSB2
16	IO41RSB2
17	IO40RSB2
18	FF/IO39RSB1
19	IO37RSB1
20	IO35RSB1
21	IO33RSB1
22	IO31RSB1
23	IO30RSB1
24	VCC
25	GND
26	VCCIB1
27	IO27RSB1
28	IO25RSB1
29	IO23RSB1
30	IO21RSB1
31	IO19RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP

QN68	
Pin Number	AGLN015 Function
36	TDO
37	TRST
38	VJTAG
39	IO17RSB0
40	IO16RSB0
41	GDA0/IO15RSB0
42	GDC0/IO14RSB0
43	IO13RSB0
44	VCCIB0
45	GND
46	VCC
47	IO12RSB0
48	IO11RSB0
49	IO09RSB0
50	IO05RSB0
51	IO00RSB0
52	IO07RSB0
53	IO03RSB0
54	IO18RSB1
55	IO20RSB1
56	IO22RSB1
57	IO24RSB1
58	IO28RSB1
59	NC
60	GND
61	NC
62	IO32RSB1
63	IO34RSB1
64	IO36RSB1
65	IO61RSB2
66	IO58RSB2
67	IO56RSB2
68	IO63RSB2

VQ100



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

VQ100	
Pin Number	AGLN125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1

VQ100	
Pin Number	AGLN125 Function
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0

VQ100	
Pin Number	AGLN125 Function
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

VQ100	
Pin Number	AGLN125Z Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1

VQ100	
Pin Number	AGLN125Z Function
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0

VQ100	
Pin Number	AGLN125Z Function
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0