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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	384
Total RAM Bits	-
Number of I/O	49
Number of Gates	15000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-20°C ~ 85°C (TJ)
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln015v2-qng68

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – IGLOO nano DC and Switching Characteristics

General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash*Freeze bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, and hot-swap I/O capability. Refer to "IGLOO nano Ordering Information" on page IV for more information.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI ¹	I/O input voltage	–0.3 V to 3.6 V	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.
2. For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.

Table 2-2 • Recommended Operating Conditions ¹

Symbol	Parameter		Extended Commercial	Industrial	Units
T _J	Junction temperature		–20 to + 85 ²	–40 to +100 ²	°C
VCC	1.5 V DC core supply voltage ³		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage ^{4,5}		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP ⁶	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL ⁷	Analog power supply (PLL)	1.5 V DC core supply voltage ³	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core supply voltage ⁴	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV ^{8,9}	1.2 V DC supply voltage ⁴		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage ⁴		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V DC wide range supply voltage ¹⁰		2.7 to 3.6	2.7 to 3.6	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.
3. For IGLOO® nano V5 devices
4. For IGLOO nano V2 devices only, operating at VCCI ≥ VCC
5. IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.
6. V_{PUMP} can be left floating during operation (not programming mode).
7. VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.
8. VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.
9. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.
10. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature¹

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T _{STG} (°C) ²	Maximum Operating Junction Temperature T _J (°C) ²
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.

Table 2-4 • Overshoot and Undershoot Limits ¹

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO nano device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO nano I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V

Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V

Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V

Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC Trip Point:

Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V

Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V

Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V

Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode*

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	μA

Note: $*I_{DD} = N_{BANKS} * I_{CCI}$

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Shutdown Mode

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	0	0	0	μA

Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode¹

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
ICCA Current²								
Typical (25°C)	1.2 V	3.7	5	5	10	13	18	μA
	1.5 V	8	14	14	20	28	44	μA
ICCI or JTAG Current								
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	μA

Notes:

1. $IDD = N_{BANKS} * ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC, VCCPLL, and VPUMP currents.

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to IGLOO nano I/O Banks

	VCCI (V)	Dynamic Power PAC9 (μW/MHz) ¹
Single-Ended		
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	16.38
3.3 V LVTTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.89
3.3 V LVCMOS Wide Range ²	3.3	16.38
3.3 V LVCMOS Wide Range – Schmitt Trigger	3.3	18.89
2.5 V LVCMOS	2.5	4.71
2.5 V LVCMOS – Schmitt Trigger	2.5	6.13
1.8 V LVCMOS	1.8	1.64
1.8 V LVCMOS – Schmitt Trigger	1.8	1.79
1.5 V LVCMOS (JESD8-11)	1.5	0.97
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.96
1.2 V LVCMOS ³	1.2	0.57
1.2 V LVCMOS – Schmitt Trigger ³	1.2	0.52
1.2 V LVCMOS Wide Range ³	1.2	0.57
1.2 V LVCMOS Wide Range – Schmitt Trigger ³	1.2	0.52

Notes:

1. PAC9 is the total dynamic power measured on V_{CCI}.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.

Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to IGLOO nano I/O Banks

	C _{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	107.98
3.3 V LVCMOS Wide Range ³	5	3.3	107.98
2.5 V LVCMOS	5	2.5	61.24
1.8 V LVCMOS	5	1.8	31.28
1.5 V LVCMOS (JESD8-11)	5	1.5	21.50
1.2 V LVCMOS ⁴	5	1.2	15.22

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PAC10 is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
4. Applicable for IGLOO nano V2 devices operating at VCCI ≥ VCC.

3.3 V LVCMOS Wide Range

Table 2-40 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range

3.3 V LVCMOS Wide Range ¹	Equivalent Software Default Drive Strength Option ⁴	VIL		VIH		VOL	VOH	IOL	I _{OH}	IIL ²	IIH ³
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	100	100	10	10

Notes:

1. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V Wide Range, as specified in the JEDEC JESD8-B specification.
2. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu A$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
5. Currents are measured at 85°C junction temperature.
6. Software default selection is highlighted in gray.

Output Register

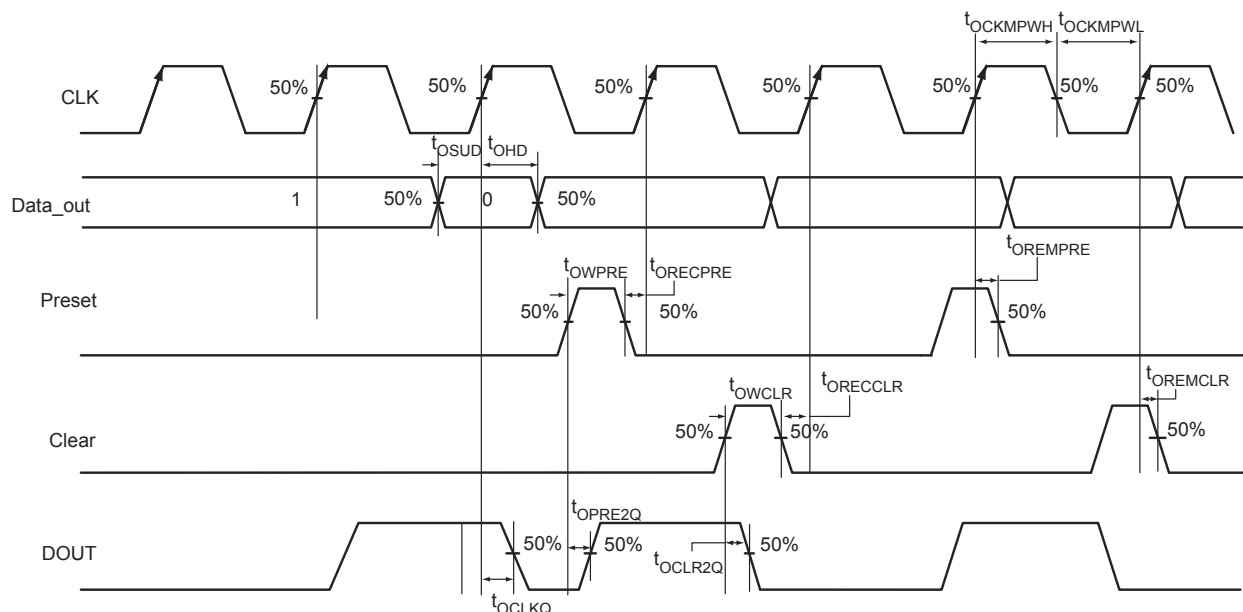


Figure 2-15 • Output Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-74 • Output Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OCKMPWH}	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
t_{OCKMPWL}	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-92 • AGLN125 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-93 • AGLN250 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-96 • AGLN020 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.81	2.26	ns
t_{RCKH}	Input High Delay for Global Clock	1.90	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-97 • AGLN060 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.42	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-100 • IGLOO nano CCC/PLL Specification
For IGLOO nano V2 OR V5 Devices, 1.5 V DC Core Supply Voltage

Parameter		Min.	Typ.	Max.	Units	
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		250	MHz	
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		250	MHz	
Delay Increments in Programmable Delay Blocks ^{1, 2}			360 ³		ps	
Number of Programmable Values in Each Programmable Delay Block				32		
Serial Clock (SCLK) for Dynamic PLL ^{4,9}				100	MHz	
Input Cycle-to-Cycle Jitter (peak magnitude)				1	ns	
Acquisition Time	LockControl = 0 LockControl = 1					
				300	μs	
				6.0	ms	
Tracking Jitter ⁵	LockControl = 0 LockControl = 1					
				2.5	ns	
				1.5	ns	
Output Duty Cycle		48.5		51.5	%	
Delay Range in Block: Programmable Delay 1 ^{1, 2}		1.25		15.65	ns	
Delay Range in Block: Programmable Delay 2 ^{1, 2,}		0.025		15.65	ns	
Delay Range in Block: Fixed Delay ^{1, 2}			3.5		ns	
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} ⁶		Max Peak-to-Peak Jitter Data ^{6,7,8}				
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16		
0.75 MHz to 50 MHz		0.50	0.60	0.80	1.20	%
50 MHz to 250 MHz		2.50	4.00	6.00	12.00	%

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
4. Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
6. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.
7. Measurements done with LVTTTL 3.3 V 8 mA I/O drive strength and high slew rate. $V_{CC}/V_{CCPLL} = 1.425\text{ V}$, $V_{CCI} = 3.3\text{ V}$, VQ/PQ/TQ type of packages, 20 pF load.
8. SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within $\pm 200\text{ ps}$ of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO nano FPGA Fabric User's Guide.
9. The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.

FIFO

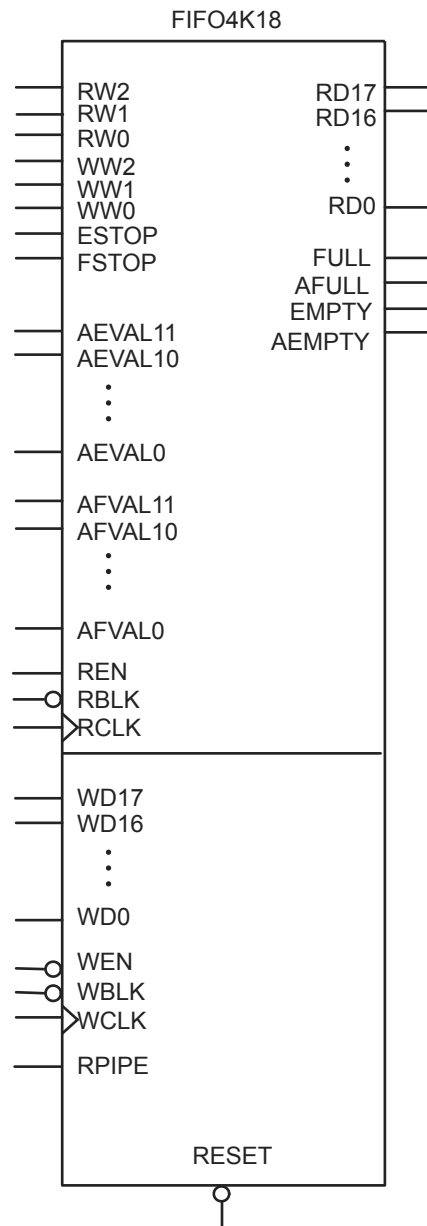
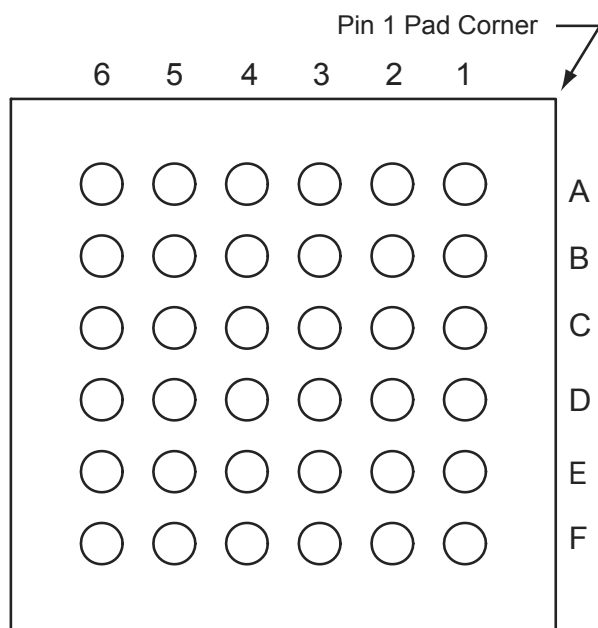


Figure 2-33 • FIFO Model

4 – Package Pin Assignments

UC36

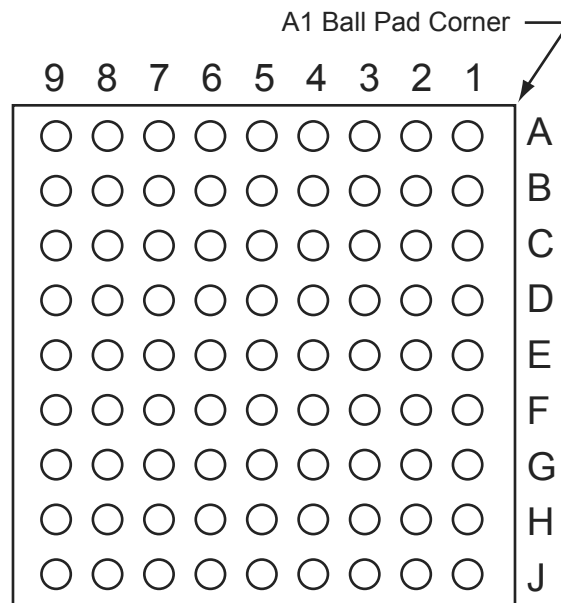


Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

UC81



Note: This is the bottom view of the package.

Note

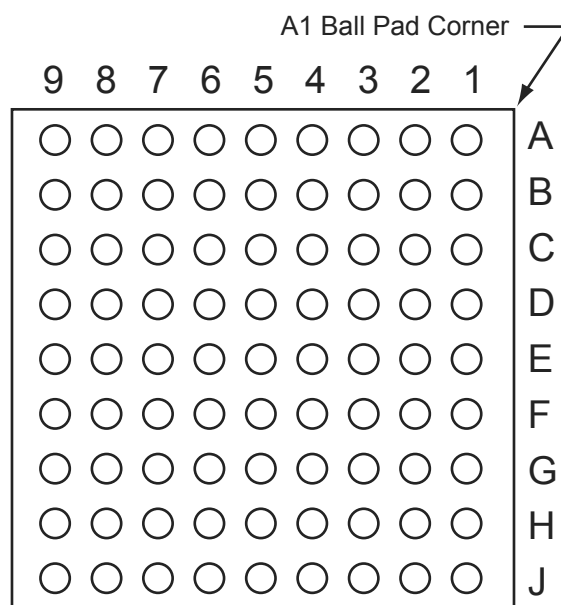
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

UC81	
Pin Number	AGLN020 Function
A1	IO64RSB2
A2	IO54RSB2
A3	IO57RSB2
A4	IO36RSB1
A5	IO32RSB1
A6	IO24RSB1
A7	IO20RSB1
A8	IO04RSB0
A9	IO08RSB0
B1	IO59RSB2
B2	IO55RSB2
B3	IO62RSB2
B4	IO34RSB1
B5	IO28RSB1
B6	IO22RSB1
B7	IO18RSB1
B8	IO00RSB0
B9	IO03RSB0
C1	IO51RSB2
C2	IO50RSB2
C3	NC
C4	NC
C5	NC
C6	NC
C7	NC
C8	IO10RSB0
C9	IO07RSB0
D1	IO49RSB2
D2	IO44RSB2
D3	NC
D4	VCC
D5	VCCIB2
D6	GND
D7	NC
D8	IO13RSB0
D9	IO12RSB0

UC81	
Pin Number	AGLN020 Function
E1	GEC0/IO48RSB2
E2	GEA0/IO47RSB2
E3	NC
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	NC
E8	GDA0/IO15RSB0
E9	GDC0/IO14RSB0
F1	IO46RSB2
F2	IO45RSB2
F3	NC
F4	GND
F5	VCCIB1
F6	NC
F7	NC
F8	IO16RSB0
F9	IO17RSB0
G1	IO43RSB2
G2	IO42RSB2
G3	IO41RSB2
G4	IO31RSB1
G5	NC
G6	IO21RSB1
G7	NC
G8	VJTAG
G9	TRST
H1	IO40RSB2
H2	FF/IO39RSB1
H3	IO35RSB1
H4	IO29RSB1
H5	IO26RSB1
H6	IO25RSB1
H7	IO19RSB1
H8	TDI
H9	TDO

UC81	
Pin Number	AGLN020 Function
J1	IO38RSB1
J2	IO37RSB1
J3	IO33RSB1
J4	IO30RSB1
J5	IO27RSB1
J6	IO23RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81

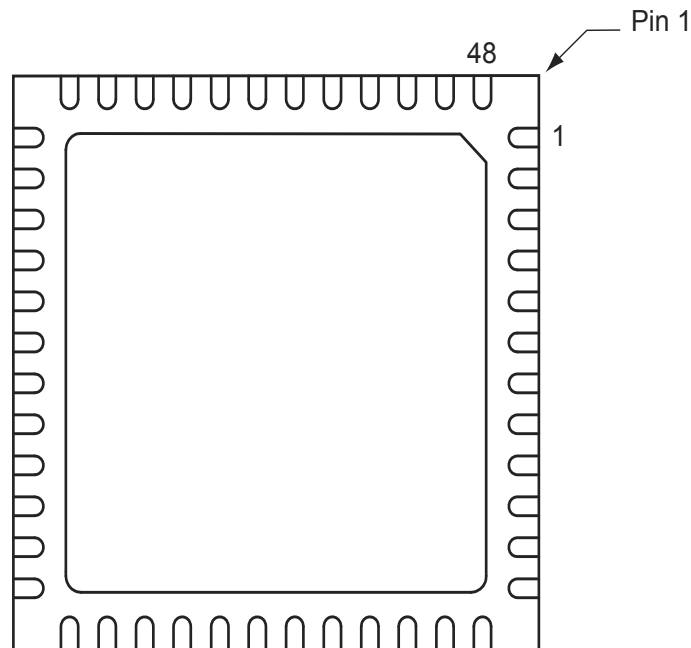


Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

QN48



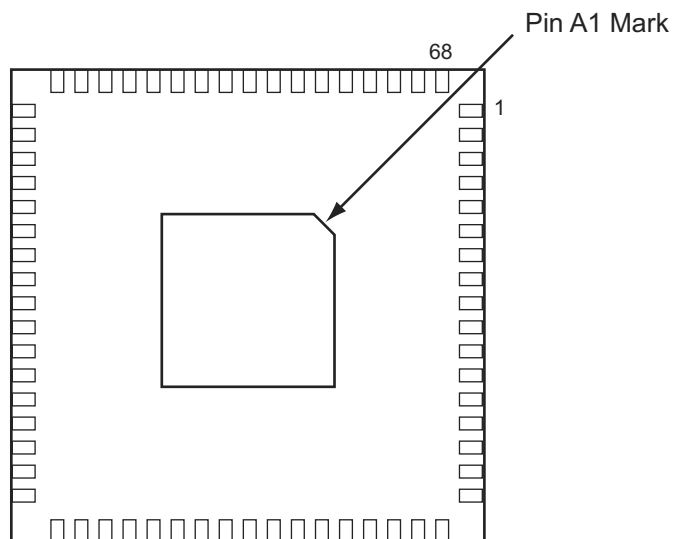
Notes:

1. *This is the bottom view of the package.*
 2. *The die attach paddle of the package is tied to ground (GND).*
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Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

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Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle of the package is tied to ground (GND).*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

Revision	Changes	Page
Revision 10 (continued)	The following tables were updated with current available information. The equivalent software default drive strength option was added. Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-28 • I/O Output Buffer Maximum Resistances ¹ Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances Table 2-30 • I/O Short Currents IOSH/IOSL Timing tables in the "Single-Ended I/O Characteristics" section, including new tables for 3.3 V and 1.2 V LVCMOS wide range. Table 2-40 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Table 2-63 • Minimum and Maximum DC Input and Output Levels Table 2-67 • Minimum and Maximum DC Input and Output Levels (new)	2-19 through 2-40
	The formulas in the notes to Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised (SAR 21348).	2-24
	The text introducing Table 2-31 • Duration of Short Circuit Event before Failure was revised to state six months at 100° instead of three months at 110° for reliability concerns. The row for 110° was removed from the table.	2-25
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5-V tolerant input buffer and push-pull output buffer."	2-32
	The F _{DDRIMAX} and F _{DDOMAX} values were added to tables in the "DDR Module Specifications" section (SAR 23919). A note was added stating that DDR is not supported for AGLN010, AGLN015, and AGLN020.	2-51
	Tables in the "Global Tree Timing Characteristics" section were updated with new information available.	2-64
	Table 2-100 • IGLOO nano CCC/PLL Specification and Table 2-101 • IGLOO nano CCC/PLL Specification were revised (SAR 79390).	2-70, 2-71
	Tables in the SRAM "Timing Characteristics" section and FIFO "Timing Characteristics" section were updated with new information available.	2-77, 2-85
	Table 3-3 • TRST and TCK Pull-Down Recommendations is new.	3-4
	A note was added to the "CS81" pin tables for AGLN060, AGLN060Z, AGLN125, AGLN125Z, AGLN250, and AGLN250Z indicating that pins F1 and F2 must be grounded (SAR 25007).	4-9, through 4-14
	A note was added to the "CS81" and "VQ100" pin tables for AGLN060 and AGLN060Z stating that bus hold is not available for pin H7 or pin 45 (SAR 24079).	4-9, 4-24
	The AGLN250 function for pin C8 in the "CS81" table was revised (SAR 22134).	4-13

Revision / Version	Changes	Page
Revision 2 (Dec 2008) Product Brief Advance v0.4 Packaging Advance v0.3	The second table note in "IGLOO nano Devices" table was revised to state, "AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. AGLN030 and smaller devices do not support this feature."	II
	The I/Os per package for CS81 were revised to 60 for AGLN060, AGLN125, and AGLN250 in the "I/Os Per Package" table.	II
	The "UC36" pin table is new.	4-2
Revision 1 (Nov 2008) Product Brief Advance v0.3	The "Advanced I/Os" section was updated to include wide power supply voltage support for 1.14 V to 1.575 V.	I
	The AGLN030 device was added to product tables and replaces AGL030 entries that were formerly in the tables.	VI
	The "I/Os Per Package" table was updated for the CS81 package to change the number of I/Os for AGLN060, AGLN125, and AGLN250 from 66 to 64.	II
	The "Wide Range I/O Support" section is new.	1-8
	The table notes and references were revised in Table 2-2 • Recommended Operating Conditions ¹ . VMV was included with VCCI and a table note was added stating, "VMV pins must be connected to the corresponding VCCI pins. See <i>Pin Descriptions</i> for further information." Please review carefully.	2-2
	VJTAG was added to the list in the table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Flash*Freeze Mode*. Values were added for AGLN010, AGLN015, and AGLN030 for 1.5 V.	2-7
	VCCI was removed from the list in the table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode*.	2-8
	Values for I _{CCA} current were updated for AGLN010, AGLN015, and AGLN030 in Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode ¹ .	2-8
	Values for PAC1 and PAC2 were added to Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices and Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices.	2-10, 2-11
	Table notes regarding wide range support were added to Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels.	2-19
	1.2 V LVCMOS wide range values were added to Table 2-22 • Summary of Maximum and Minimum DC Input Levels and Table 2-23 • Summary of AC Measuring Points.	2-19, 2-20
	The following table note was added to Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings and Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings: "All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification."	2-21
	3.3 V LVCMOS Wide Range and 1.2 V Wide Range were added to Table 2-28 • I/O Output Buffer Maximum Resistances ¹ and Table 2-30 • I/O Short Currents IOSH/IOSL.	2-23, 2-24