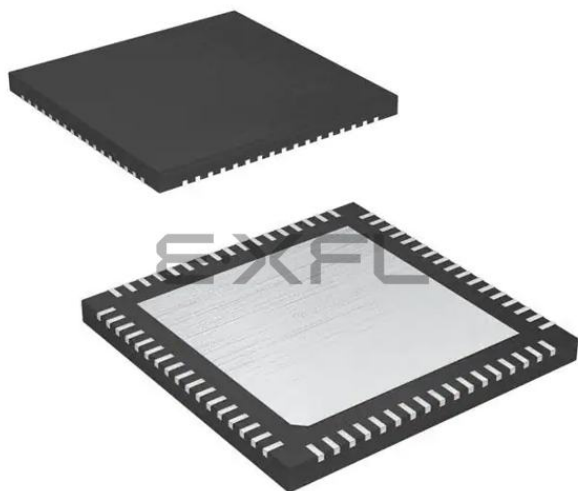




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	384
Total RAM Bits	-
Number of I/O	49
Number of Gates	15000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln015v5-qng68i

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – IGLOO nano DC and Switching Characteristics

General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash*Freeze bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, and hot-swap I/O capability. Refer to "IGLOO nano Ordering Information" on page IV for more information.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI ¹	I/O input voltage	–0.3 V to 3.6 V	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.
2. For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$ for V5 devices, and $0.75\text{ V} \pm 0.2\text{ V}$ for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

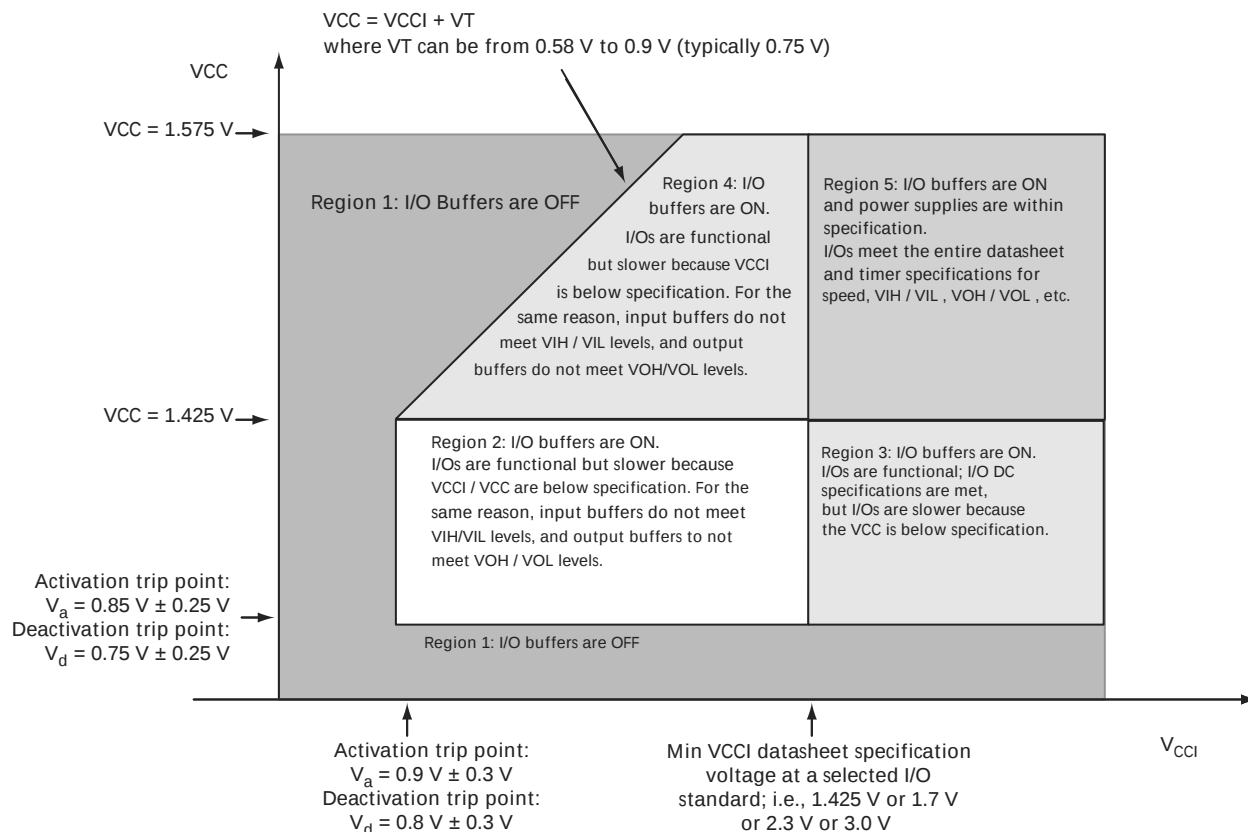


Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

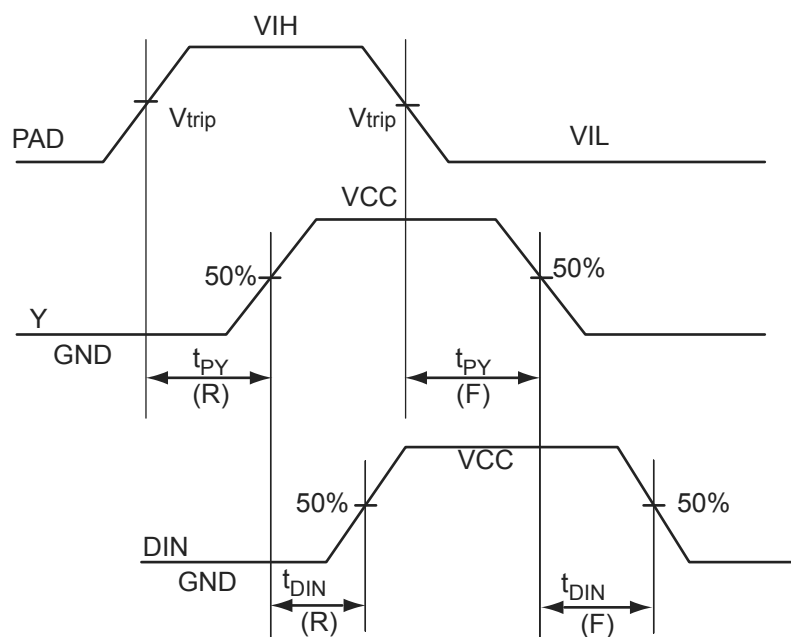
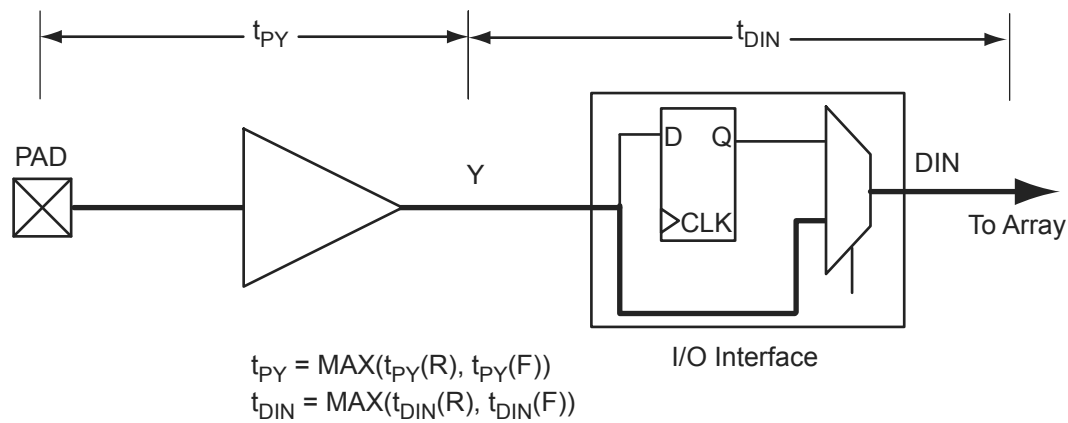


Figure 2-4 • Input Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels
Applicable to Commercial and Industrial Conditions—Software Default Settings

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹	IOH ¹
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
3.3 V LVCMOS Wide Range ³	100 μ A	8 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100 μ A	100 μ A
2.5 V LVCMOS	8 mA	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5 V LVCMOS	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS ⁴	1 mA	1 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1
1.2 V LVCMOS Wide Range ^{4,5}	100 μ A	1 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	100 μ A	100 μ A

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.
4. Applicable to IGLOO nano V2 devices operating at VCCI $\geq$ VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range, as specified in the JESD8-12 specification.

Table 2-22 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions

DC I/O Standards	Commercial ¹		Industrial ²	
	IIL ³	IIH ⁴	IIL ³	IIH ⁴
	μ A	μ A	μ A	μ A
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCOMS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS ⁵	10	10	15	15
1.2 V LVCMOS Wide Range ⁵	10	10	15	15

Notes:

1. Commercial range ($-20^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions, where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. I_{IL} is the input leakage current per I/O pin over recommended operating conditions, where $-0.3 \text{ V} < V_{IN} < V_{IL}$.
5. Applicable to IGLOO nano V2 devices operating at VCCI $\geq$ VCC.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	3.52	0.19	0.86	1.16	0.66	3.59	3.42	1.75	1.90	ns
4 mA	STD	0.97	3.52	0.19	0.86	1.16	0.66	3.59	3.42	1.75	1.90	ns
6 mA	STD	0.97	2.90	0.19	0.86	1.16	0.66	2.96	2.83	1.98	2.29	ns
8 mA	STD	0.97	2.90	0.19	0.86	1.16	0.66	2.96	2.83	1.98	2.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.16	0.19	0.86	1.16	0.66	2.20	1.80	1.75	1.99	ns
4 mA	STD	0.97	2.16	0.19	0.86	1.16	0.66	2.20	1.80	1.75	1.99	ns
6 mA	STD	0.97	1.79	0.19	0.86	1.16	0.66	1.83	1.45	1.98	2.38	ns
8 mA	STD	0.97	1.79	0.19	0.86	1.16	0.66	1.83	1.45	1.98	2.38	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-53 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.44	0.19	1.03	1.44	0.66	5.25	5.44	1.69	1.35	ns
4 mA	STD	0.97	4.44	0.19	1.03	1.44	0.66	4.37	4.44	1.99	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-54 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.64	0.19	1.03	1.44	0.66	2.59	2.64	1.69	1.40	ns
4 mA	STD	0.97	2.08	0.19	1.03	1.44	0.66	2.12	1.95	1.99	2.19	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-55 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	5.92	0.26	1.13	1.59	1.10	5.72	5.92	2.11	1.95	ns
4 mA	STD	1.55	4.91	0.26	1.13	1.59	1.10	4.82	4.91	2.42	2.73	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-56 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	3.05	0.26	1.13	1.59	1.10	3.01	3.05	2.10	2.00	ns
4 mA	STD	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Input Register

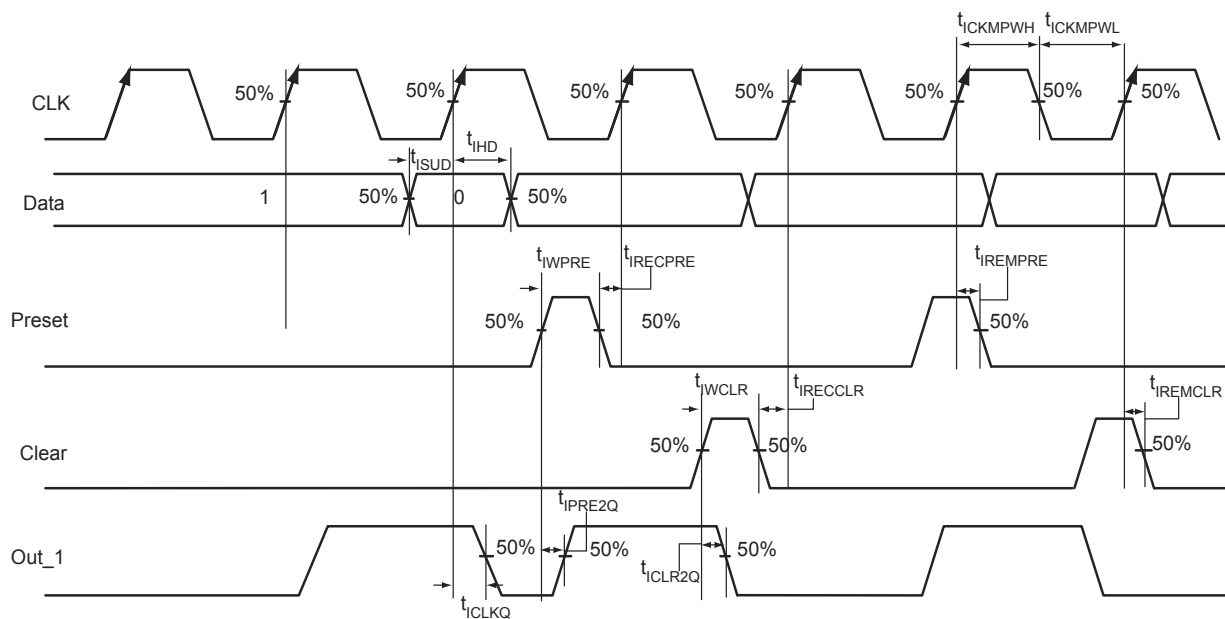


Figure 2-14 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-72 • Input Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output Enable Register

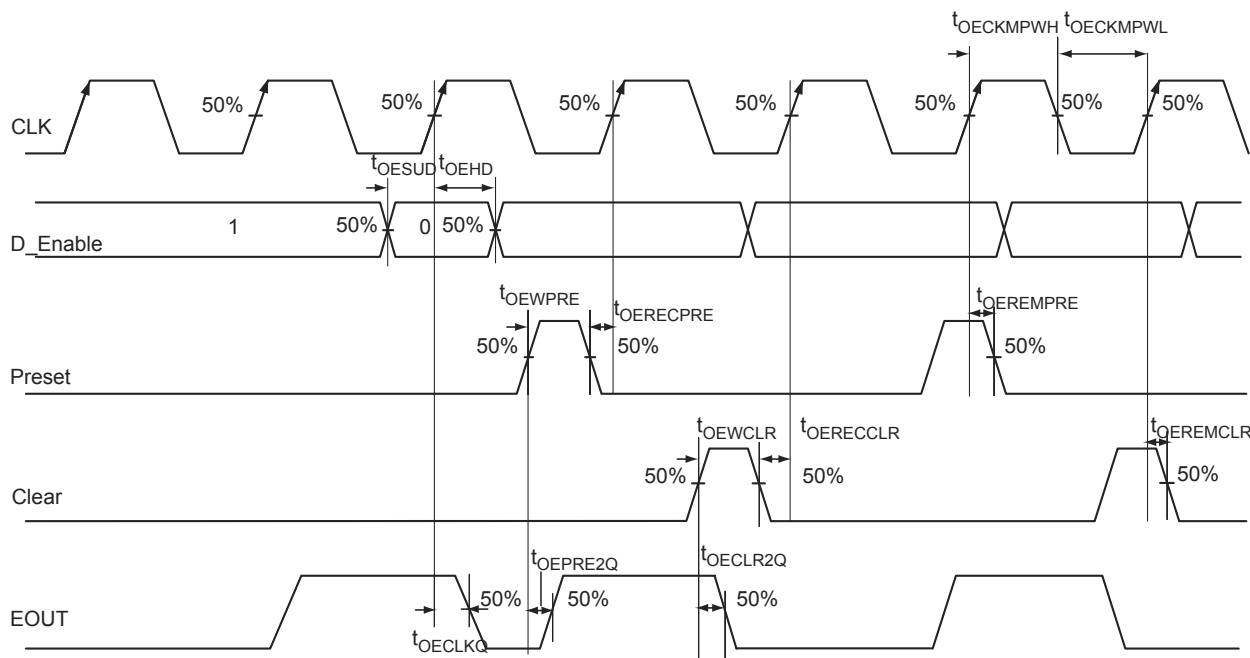


Figure 2-16 • Output Enable Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-76 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.75	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

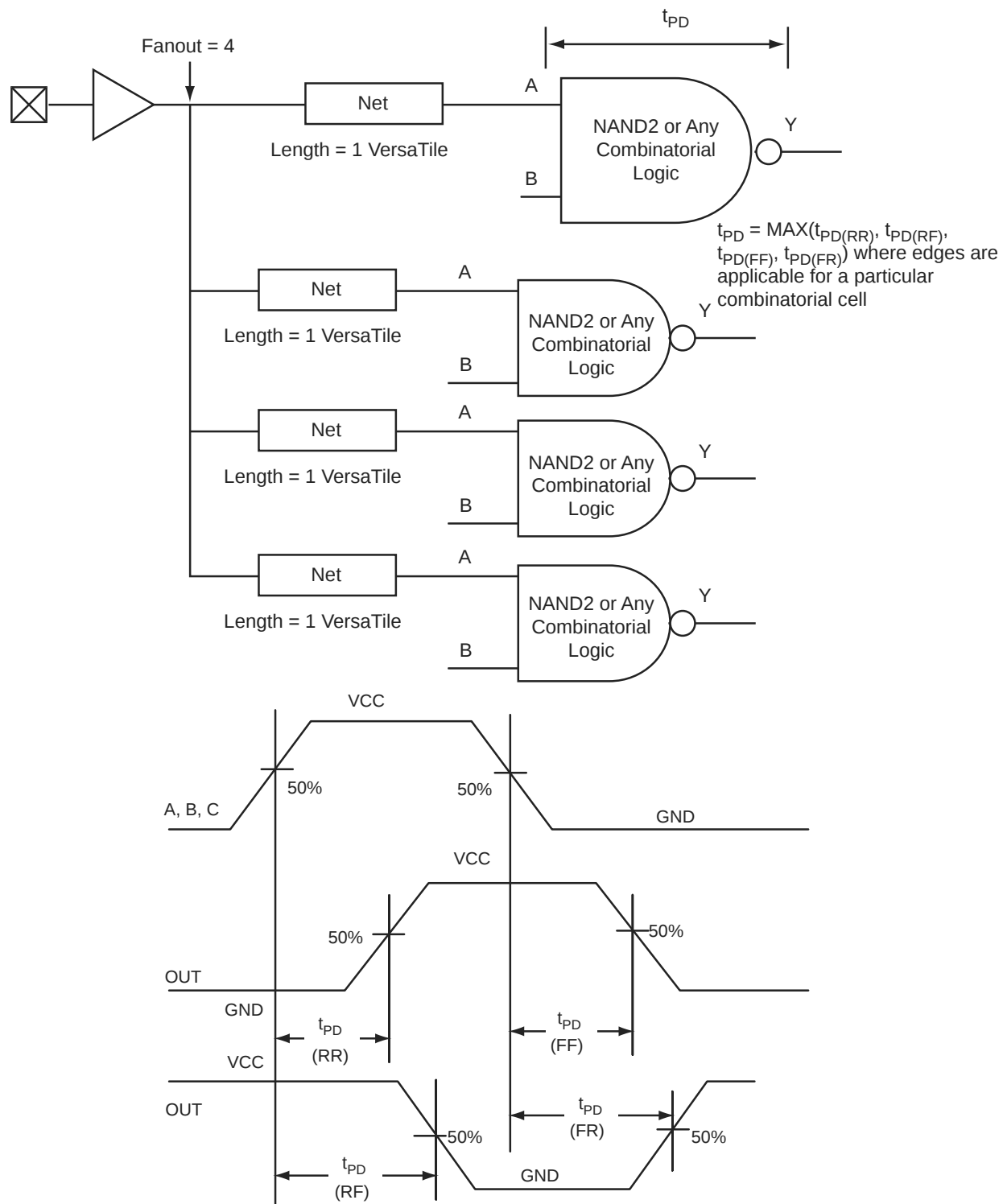


Figure 2-22 • Timing Model and Waveforms

Table 2-92 • AGLN125 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-93 • AGLN250 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

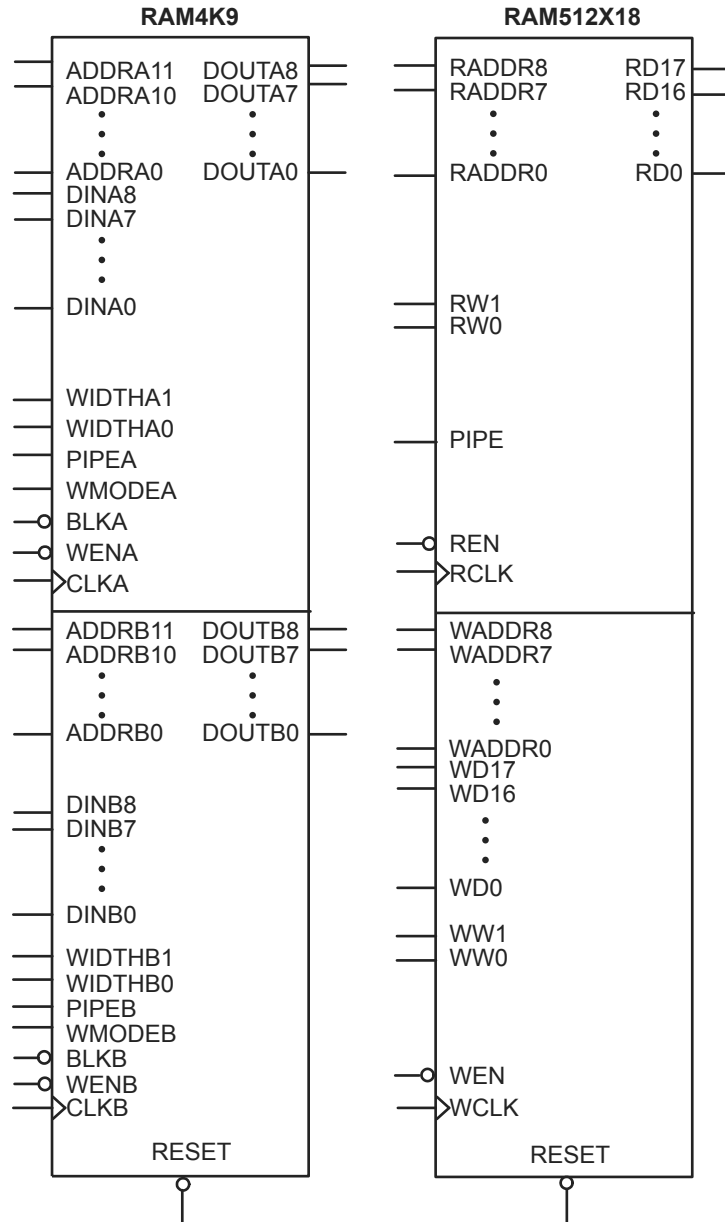


Figure 2-27 • RAM Models

Timing Waveforms

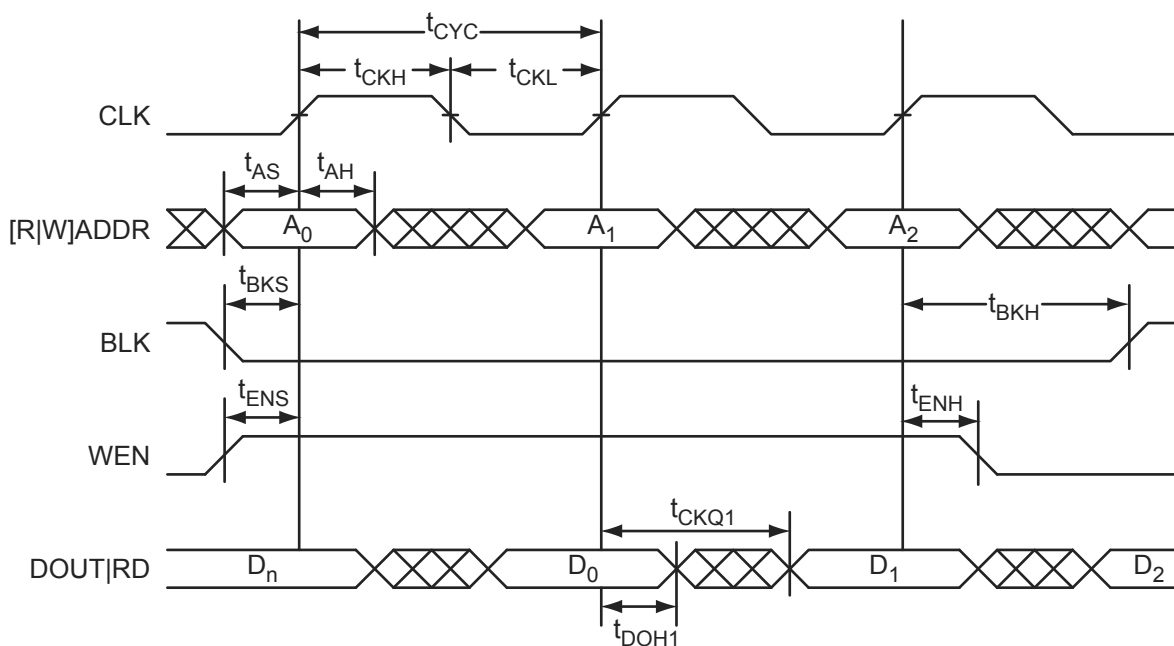


Figure 2-28 • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.

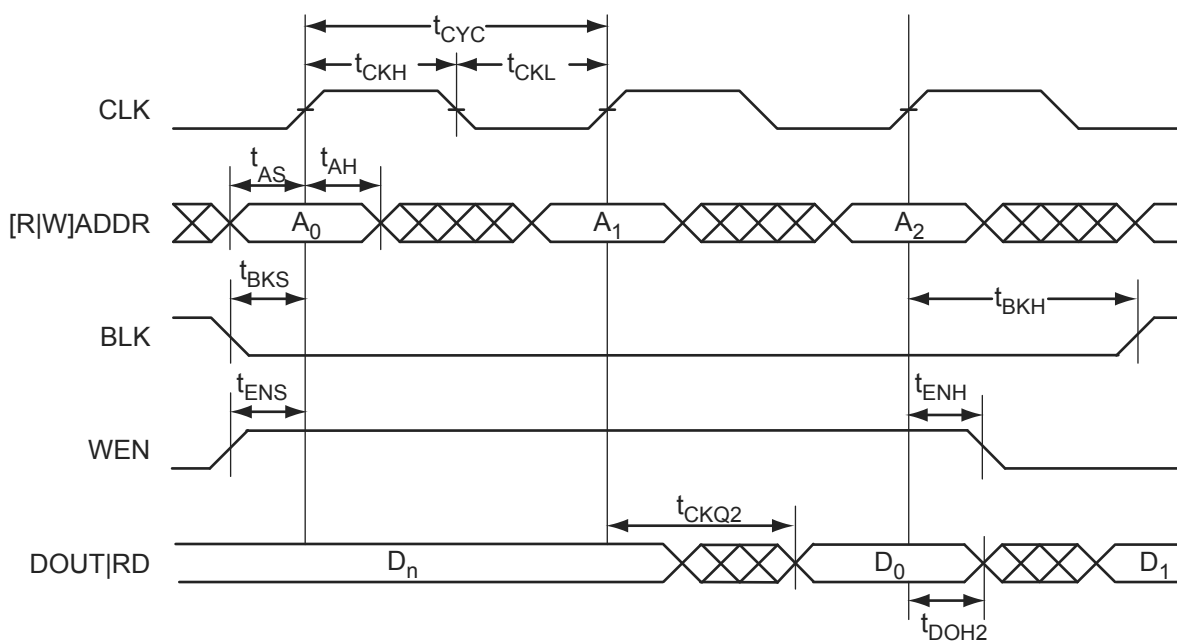


Figure 2-29 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.

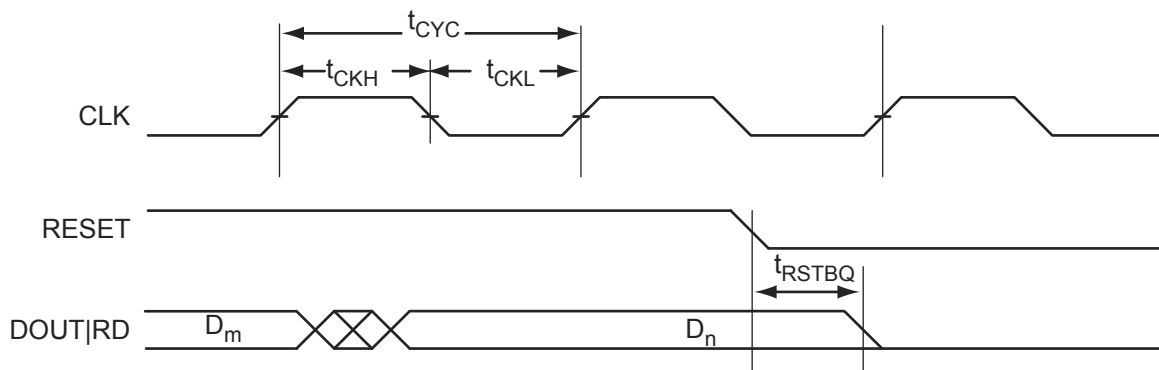


Figure 2-32 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.

Related Documents

User Guides

IGLOO nano FPGA Fabric User's Guide

Packaging Documents

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

FPGA and SoC Product Catalog

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are on the Microsemi SoC Products Group website:

<http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

UC81	
Pin Number	AGLN030Z Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0

UC81	
Pin Number	AGLN030Z Function
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1

UC81	
Pin Number	AGLN030Z Function
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	AGLN125Z Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO13RSB0
A5	IO22RSB0
A6	IO32RSB0
A7	GBB0/IO37RSB0
A8	GBA1/IO40RSB0
A9	GBA2/IO41RSB0
B1	GAA2/IO132RSB1
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO11RSB0
B5	IO25RSB0
B6	GBC0/IO35RSB0
B7	GBB1/IO38RSB0
B8	IO42RSB0
B9	GBB2/IO43RSB0
C1	GAB2/IO130RSB1
C2	IO131RSB1
C3	GND
C4	IO15RSB0
C5	IO28RSB0
C6	GND
C7	GBA0/IO39RSB0
C8	GBC2/IO45RSB0
C9	IO47RSB0
D1	GAC2/IO128RSB1
D2	IO129RSB1
D3	GFA2/IO117RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO59RSB0
D8	GCC1/IO51RSB0
D9	GCC0/IO52RSB0

CS81	
Pin Number	AGLN125Z Function
E1	GFB0/IO120RSB1
E2	GFB1/IO121RSB1
E3	GFA1/IO118RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GCA0/IO56RSB0
E8	GCA1/IO55RSB0
E9	GCB2/IO58RSB0
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO65RSB0
F8	GDC1/IO61RSB0
F9	GDC0/IO62RSB0
G1	GEA0/IO104RSB1
G2	GEC0/IO108RSB1
G3	GEB1/IO107RSB1
G4	IO96RSB1
G5	IO92RSB1
G6	IO72RSB1
G7	GDB2/IO68RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO105RSB1
H2	FF/GEB2/IO102RSB1
H3	IO99RSB1
H4	IO94RSB1
H5	IO91RSB1
H6	IO81RSB1
H7	GDA2/IO67RSB1
H8	TDI
H9	TDO

CS81	
Pin Number	AGLN125Z Function
J1	GEA2/IO103RSB1
J2	GEC2/IO101RSB1
J3	IO97RSB1
J4	IO93RSB1
J5	IO90RSB1
J6	IO78RSB1
J7	TCK
J8	TMS
J9	VPUMP

Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN125Z-CS81.

CS81		CS81		CS81	
Pin Number	AGLN250 Function	Pin Number	AGLN250 Function	Pin Number	AGLN250 Function
A1	GAA0/IO00RSB0	E1	GFB0/IO59RSB3	J1	GEA2/IO50RSB2
A2	GAA1/IO01RSB0	E2	GFB1/IO60RSB3	J2	GEC2/IO48RSB2
A3	GAC0/IO04RSB0	E3	GFA1/IO58RSB3	J3	IO46RSB2
A4	IO07RSB0	E4	VCCIB3	J4	IO43RSB2
A5	IO09RSB0	E5	VCC	J5	IO40RSB2
A6	IO12RSB0	E6	VCCIB1	J6	IO38RSB2
A7	GBB0/IO16RSB0	E7	GCA0/IO28RSB1	J7	TCK
A8	GBA1/IO19RSB0	E8	GCA1/IO27RSB1	J8	TMS
A9	GBA2/IO20RSB1	E9	GCB2/IO29RSB1	J9	VPUMP
B1	GAA2/IO67RSB3	F1	VCCPLF		
B2	GAB0/IO02RSB0	F2	VCOMPLF		
B3	GAC1/IO05RSB0	F3	GND		
B4	IO06RSB0	F4	GND		
B5	IO10RSB0	F5	VCCIB2		
B6	GBC0/IO14RSB0	F6	GND		
B7	GBB1/IO17RSB0	F7	GDA1/IO33RSB1		
B8	IO21RSB1	F8	GDC1/IO31RSB1		
B9	GBB2/IO22RSB1	F9	GDC0/IO32RSB1		
C1	GAB2/IO65RSB3	G1	GEA0/IO51RSB3		
C2	IO66RSB3	G2	GEC1/IO54RSB3		
C3	GND	G3	GEC0/IO53RSB3		
C4	IO08RSB0	G4	IO45RSB2		
C5	IO11RSB0	G5	IO42RSB2		
C6	GND	G6	IO37RSB2		
C7	GBA0/IO18RSB0	G7	GDB2/IO35RSB2		
C8	GBC2/IO23RSB1	G8	VJTAG		
C9	IO24RSB1	G9	TRST		
D1	GAC2/IO63RSB3	H1	GEA1/IO52RSB3		
D2	IO64RSB3	H2	FF/GEB2/IO49RSB2		
D3	GFA2/IO56RSB3	H3	IO47RSB2		
D4	VCC	H4	IO44RSB2		
D5	VCCIB0	H5	IO41RSB2		
D6	GND	H6	IO39RSB2		
D7	IO30RSB1	H7	GDA2/IO34RSB2		
D8	GCC1/IO25RSB1	H8	TDI		
D9	GCC0/IO26RSB1	H9	TDO		

Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250-CS81.

VQ100	
Pin Number	AGLN030Z Function
1	GND
2	IO82RSB1
3	IO81RSB1
4	IO80RSB1
5	IO79RSB1
6	IO78RSB1
7	IO77RSB1
8	IO76RSB1
9	GND
10	IO75RSB1
11	IO74RSB1
12	GEC0/IO73RSB1
13	GEA0/IO72RSB1
14	GEB0/IO71RSB1
15	IO70RSB1
16	IO69RSB1
17	VCC
18	VCCIB1
19	IO68RSB1
20	IO67RSB1
21	IO66RSB1
22	IO65RSB1
23	IO64RSB1
24	IO63RSB1
25	IO62RSB1
26	IO61RSB1
27	FF/IO60RSB1
28	IO59RSB1
29	IO58RSB1
30	IO57RSB1
31	IO56RSB1
32	IO55RSB1
33	IO54RSB1
34	IO53RSB1
35	IO52RSB1

VQ100	
Pin Number	AGLN030Z Function
36	IO51RSB1
37	VCC
38	GND
39	VCCIB1
40	IO49RSB1
41	IO47RSB1
42	IO46RSB1
43	IO45RSB1
44	IO44RSB1
45	IO43RSB1
46	IO42RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	IO41RSB0
58	IO40RSB0
59	IO39RSB0
60	IO38RSB0
61	IO37RSB0
62	IO36RSB0
63	GDB0/IO34RSB0
64	GDA0/IO33RSB0
65	GDC0/IO32RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	IO30RSB0

VQ100	
Pin Number	AGLN030Z Function
71	IO29RSB0
72	IO28RSB0
73	IO27RSB0
74	IO26RSB0
75	IO25RSB0
76	IO24RSB0
77	IO23RSB0
78	IO22RSB0
79	IO21RSB0
80	IO20RSB0
81	IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO16RSB0
85	IO15RSB0
86	IO14RSB0
87	VCCIB0
88	GND
89	VCC
90	IO12RSB0
91	IO10RSB0
92	IO08RSB0
93	IO07RSB0
94	IO06RSB0
95	IO05RSB0
96	IO04RSB0
97	IO03RSB0
98	IO02RSB0
99	IO01RSB0
100	IO00RSB0

VQ100	
Pin Number	AGLN060 Function
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1

VQ100	
Pin Number	AGLN060 Function
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45*	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	GBC2/IO29RSB0

VQ100	
Pin Number	AGLN060 Function
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

Note: *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin 45 in AGLN060-VQ100.