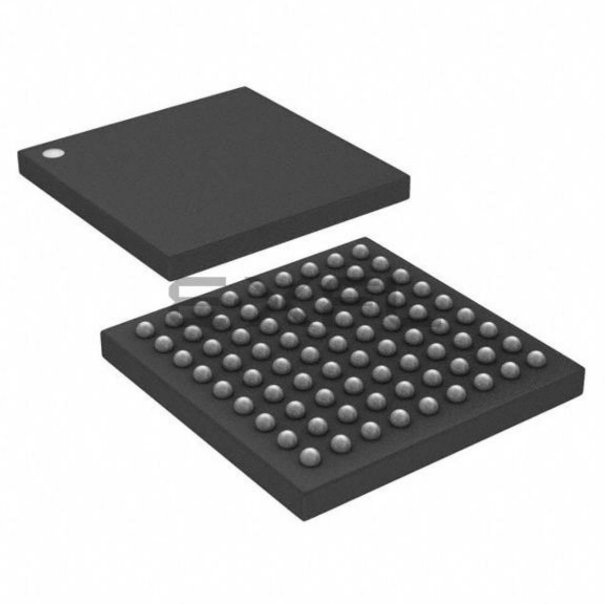


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	520
Total RAM Bits	-
Number of I/O	52
Number of Gates	20000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	81-WFBGA, CSBGA
Supplier Device Package	81-CSP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln020v5-csg81i

IGLOO nano Devices	AGLN010	AGLN015[1]	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices[1]				AGLN030Z[1]	AGLN060Z[1]	AGLN125Z[1]	AGLN250Z[1]
Package Pins UC/CS QFN VQFP	UC36 QN48	QN68	UC81, CS81 QN68	UC81, CS81 QN48, QN68 VQ100	CS81 VQ100	CS81 VQ100	CS81 VQ100

Notes:

1. *Not recommended for new designs. Few devices/packages are obsoleted. For more information on obsoleted devices/packages, refer to the PDN 1503 - IGLOO nano Z and ProASIC3 nano Z Families.*
2. *AGLN030 and smaller devices do not support this feature.*
3. *AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs.*
4. *For higher densities and support of additional features, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOOe Low-Power Flash FPGAs Datasheet .*

I/Os Per Package

IGLOO nano Devices	AGLN010	AGLN015[1]	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices[1]				AGLN030Z[1]	AGLN060Z[1]	AGLN125Z[1]	AGLN250Z[1]
Known Good Die	34	–	52	83	71	71	68
UC36	23	–	–	–	–	–	–
QN48	34	–	–	34	–	–	–
QN68	–	49	49	49	–	–	–
UC81	–	–	52	66	–	–	–
CS81	–	–	52	66	60	60	60
VQ100	–	–	–	77	71	71	68

Notes:

1. *Not recommended for new designs.*
2. *When considering migrating your design to a lower- or higher-density device, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOO FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.*
3. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
4. *"G" indicates RoHS-compliant packages. Refer to "IGLOO nano Ordering Information" on page IV for the location of the "G" in the part number. For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.*

Table 1 • **IGLOO nano FPGAs Package Sizes Dimensions**

Packages	UC36	UC81	CS81	QN48	QN68	VQ100
Length × Width (mm\mm)	3 x 3	4 x 4	5 x 5	6 x 6	8 x 8	14 x 14
Nominal Area (mm^2)	9	16	25	36	64	196
Pitch (mm)	0.4	0.4	0.5	0.4	0.4	0.5
Height (mm)	0.80	0.80	0.80	0.90	0.90	1.20

IGLOO nano Device Status

IGLOO nano Devices	Status	IGLOO nano-Z Devices	Status
AGLN010	Production		
AGLN015	Not recommended for new designs.		
AGLN020	Production		
		AGLN030Z	Not recommended for new designs.
AGLN060	Production	AGLN060Z	Not recommended for new designs.
AGLN125	Production	AGLN125Z	Not recommended for new designs.
AGLN250	Production	AGLN250Z	Not recommended for new designs.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

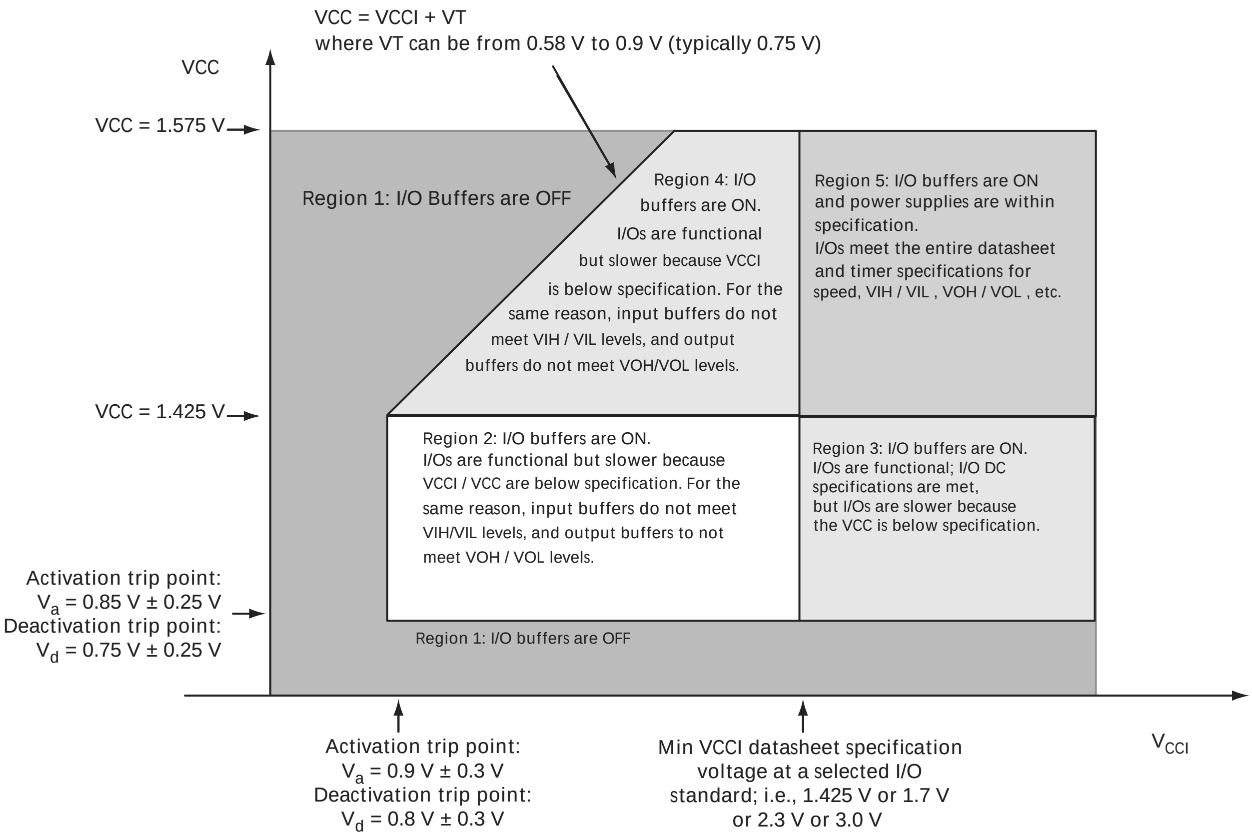


Figure 2-1 • **V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (^\circ C) - \text{Max. ambient temp. } (^\circ C)}{\theta_{ja}(^\circ C/W)} = \frac{100^\circ C - 70^\circ C}{20.5^\circ C/W} = 1.46\ W$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Chip Scale Package (CSP)	36	TBD	TBD	TBD	TBD	C/W
	81	TBD	TBD	TBD	TBD	C/W
Quad Flat No Lead (QFN)	48	TBD	TBD	TBD	TBD	C/W
	68	TBD	TBD	TBD	TBD	C/W
	100	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**
For IGLOO nano V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C) –40°C	–20°C	0°C	25°C	70°C	85°C	100°C
1.425	0.947	0.956	0.965	0.978	1.000	1.009	1.013
1.5	0.875	0.883	0.892	0.904	0.925	0.932	0.937
1.575	0.821	0.829	0.837	0.848	0.868	0.875	0.879

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = (PDC1 or PDC2 or PDC3) + N_{BANKS} * PDC5

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL}* PAC4) * F_{CLK}

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—P_{S-CELL}

$P_{S-CELL} = N_{S-CELL}$ * (PAC5 + α_1 / 2 * PAC6) * F_{CLK}

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
3.3 V LVCMOS Wide Range[3]	100 µA	8 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100 µA	100 µA
2.5 V LVCMOS	8 mA	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5 V LVCMOS	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS[4]	1 mA	1 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1
1.2 V LVCMOS Wide Range[4,5]	100 µA	1 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	100 µA	100 µA

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
4. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range, as specified in the JESD8-12 specification.*

Table 2-22 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

DC I/O Standards	Commercial[1]		Industrial[2]	
	IIL [3]	IIH [4]	IIL [3]	IIH [4]
	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCOMS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[5]	10	10	15	15
1.2 V LVCMOS Wide Range[5]	10	10	15	15

Notes:

1. *Commercial range (–20°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions, where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions, where –0.3 V < VIN < VIL.*
5. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-34 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

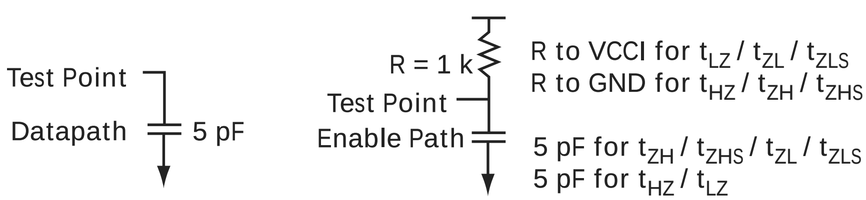


Figure 2-7 • **AC Loading**

Table 2-35 • **3.3 V LVTTL/LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Applies to 1.2 V DC Core Voltage

Table 2-49 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
4 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
6 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns
8 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-50 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
4 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
6 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
8 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-77 • Output Enable Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

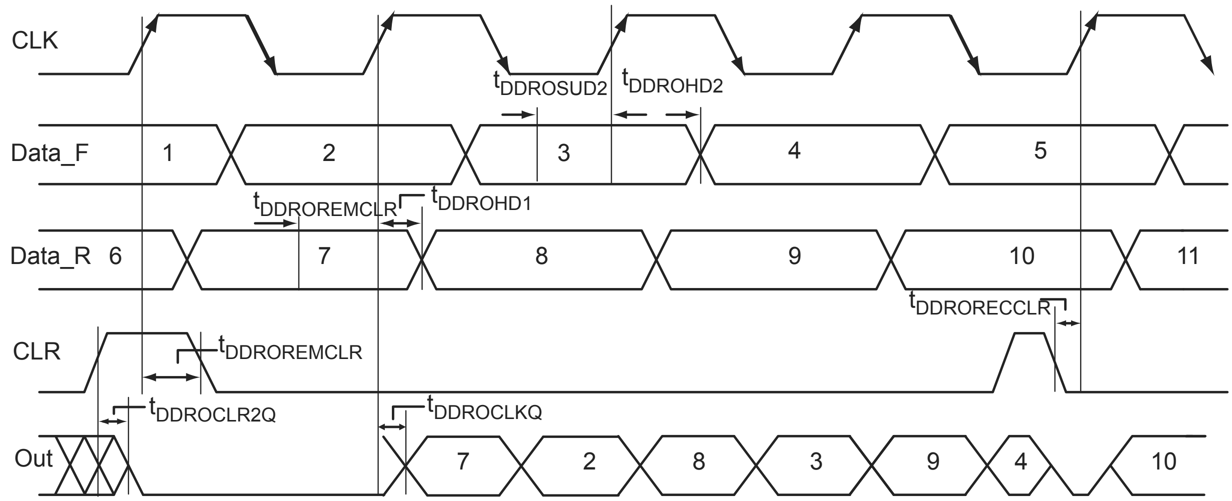


Figure 2-20 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

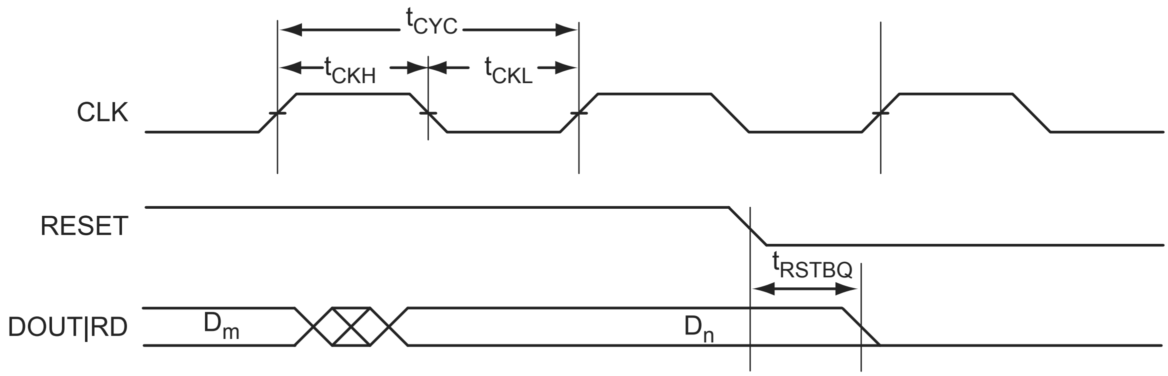


Figure 2-32 • **RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

1.2 V DC Core Voltage

Table 2-104 • **RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.25	ns
t_{ENH}	REN, WEN hold time	0.25	ns
t_{BKS}	BLK setup time	2.54	ns
t_{BKH}	BLK hold time	0.25	ns
t_{DS}	Input data (DIN) setup time	1.10	ns
t_{DH}	Input data (DIN) hold time	0.55	ns
t_{CKQ1}	Clock HIGH to new data valid on DOUT (output retained, WMODE = 0)	5.51	ns
	Clock HIGH to new data valid on DOUT (flow-through, WMODE = 1)	4.77	ns
t_{CKQ2}	Clock HIGH to new data valid on DOUT (pipelined)	2.82	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.89	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.01	ns
t_{RSTBQ}	RESET LOW to data out LOW on DOUT (flow-through)	3.21	ns
	RESET LOW to data out LOW on DO (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

FIFO

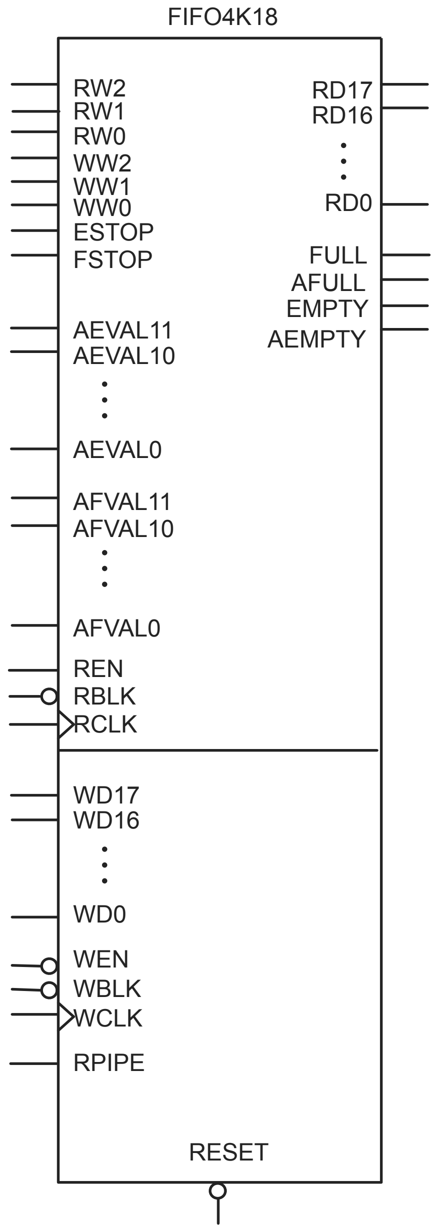


***Figure 2-33* • FIFO Model**

1.2 V DC Core Voltage

***Table 2-107* • FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.30	ns
t_{DH}	Input Data (DI) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET LOW to Data Out Low on RD (flow-through)	3.41	ns
	RESET LOW to Data Out Low on RD (pipelined)	4.09	3.41
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

UC81	
Pin Number	AGLN030Z Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0

UC81	
Pin Number	AGLN030Z Function
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1

UC81	
Pin Number	AGLN030Z Function
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

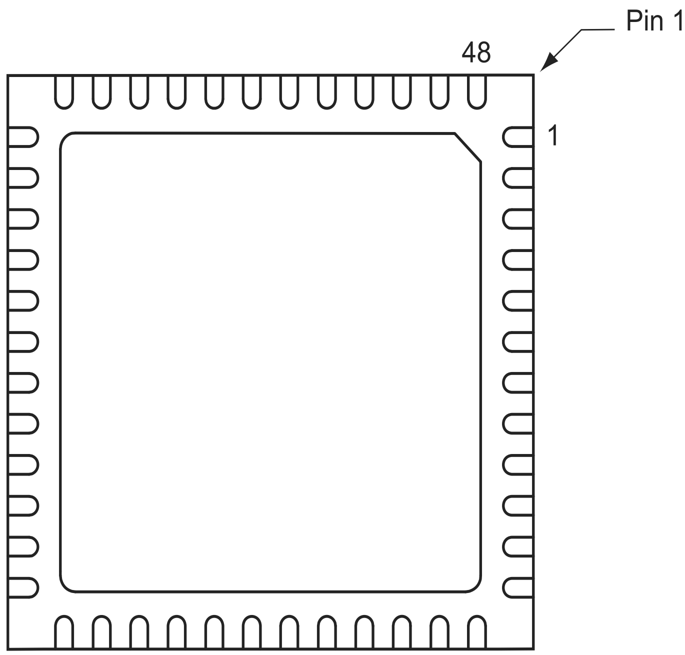
CS81	
Pin Number	AGLN250Z Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO12RSB0
A7	GBB0/IO16RSB0
A8	GBA1/IO19RSB0
A9	GBA2/IO20RSB1
B1	GAA2/IO67RSB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO06RSB0
B5	IO10RSB0
B6	GBC0/IO14RSB0
B7	GBB1/IO17RSB0
B8	IO21RSB1
B9	GBB2/IO22RSB1
C1	GAB2/IO65RSB3
C2	IO66RSB3
C3	GND
C4	IO08RSB0
C5	IO11RSB0
C6	GND
C7	GBA0/IO18RSB0
C8	GBC2/IO23RSB1
C9	IO24RSB1
D1	GAC2/IO63RSB3
D2	IO64RSB3
D3	GFA2/IO56RSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO30RSB1
D8	GCC1/IO25RSB1
D9	GCC0/IO26RSB1

CS81	
Pin Number	AGLN250Z Function
E1	GFB0/IO59RSB3
E2	GFB1/IO60RSB3
E3	GFA1/IO58RSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1
E7	GCA0/IO28RSB1
E8	GCA1/IO27RSB1
E9	GCB2/IO29RSB1
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO33RSB1
F8	GDC1/IO31RSB1
F9	GDC0/IO32RSB1
G1	GEA0/IO51RSB3
G2	GEC1/IO54RSB3
G3	GEC0/IO53RSB3
G4	IO45RSB2
G5	IO42RSB2
G6	IO37RSB2
G7	GDB2/IO35RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO52RSB3
H2	FF/GEB2/IO49RSB2
H3	IO47RSB2
H4	IO44RSB2
H5	IO41RSB2
H6	IO39RSB2
H7	GDA2/IO34RSB2
H8	TDI
H9	TDO

CS81	
Pin Number	AGLN250Z Function
J1	GEA2/IO50RSB2
J2	GEC2/IO48RSB2
J3	IO46RSB2
J4	IO43RSB2
J5	IO40RSB2
J6	IO38RSB2
J7	TCK
J8	TMS
J9	VPUMP

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250Z-CS81.*

QN48



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle of the package is tied to ground (GND).*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

QN48		QN48	
Pin Number	AGLN030Z Function	Pin Number	AGLN030Z Function
1	IO82RSB1	37	IO24RSB0
2	GEC0/IO73RSB1	38	IO22RSB0
3	GEA0/IO72RSB1	39	IO20RSB0
4	GEB0/IO71RSB1	40	IO18RSB0
5	GND	41	IO16RSB0
6	VCCIB1	42	IO14RSB0
7	IO68RSB1	43	IO10RSB0
8	IO67RSB1	44	IO08RSB0
9	IO66RSB1	45	IO06RSB0
10	IO65RSB1	46	IO04RSB0
11	IO64RSB1	47	IO02RSB0
12	IO62RSB1	48	IO00RSB0
13	IO61RSB1		
14	FF/IO60RSB1		
15	IO57RSB1		
16	IO55RSB1		
17	IO53RSB1		
18	VCC		
19	VCCIB1		
20	IO46RSB1		
21	IO42RSB1		
22	TCK		
23	TDI		
24	TMS		
25	VPUMP		
26	TDO		
27	TRST		
28	VJTAG		
29	IO38RSB0		
30	GDB0/IO34RSB0		
31	GDA0/IO33RSB0		
32	GDC0/IO32RSB0		
33	VCCIB0		
34	GND		
35	VCC		
36	IO25RSB0		

Revision	Changes	Page
Revision 12 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34663).	I, 1-2
	Notes indicating that AGLN015 is not recommended for new designs have been added (SAR 35759). Notes indicating that nano-Z devices are not recommended for new designs have been added. The "Devices Not Recommended For New Designs" section is new (SAR 36759).	III, IV
Revision 12 (continued)	The Y security option and Licensed DPA Logo were added to the "IGLOO nano Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34722).	IV
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry enables rapid, single-voltage (3.3 V) programming of IGLOO nano devices via an IEEE 1532 JTAG interface" (SAR 34683).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 34694).	1-9
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—P_{CLOCK}" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOO nano FPGA Fabric User's Guide* (SAR 34732).	2-12
	Figure 2-4 has been modified for DIN waveform; the Rise and Fall time label has been changed to tDIN (37106).	2-16
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34885).	2-26, 2-20
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34765).	2-20, 2-29, 2-40
	Added values for minimum pulse width and removed the FRMAX row from Table 2-88 through Table 2-99 in the "Global Tree Timing Characteristics" section. Use the software to determine the FRMAX for the device you are using (SAR 36953).	2-64 to 2-69
	Table 2-100 • IGLOO nano CCC/PLL Specification and Table 2-101 • IGLOO nano CCC/PLL Specification were updated. A note was added indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available (SAR 34817).	2-70 and 2-71
	The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-36 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35754). Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34865).	2-74, 2-77, 2-85
	The "Pin Descriptions" chapter has been added (SAR 34770).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34770).	4-1

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