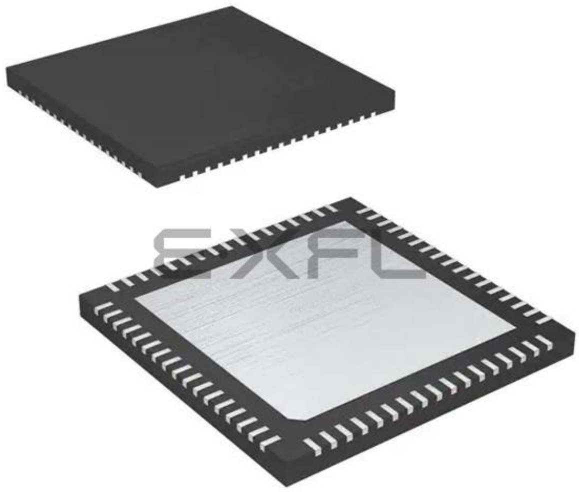

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	520
Total RAM Bits	-
Number of I/O	49
Number of Gates	20000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-20°C ~ 85°C (TJ)
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln020v5-qng68

Device Marking

Microsemi normally topside marks the full ordering part number on each device. There are some exceptions to this, such as some of the Z feature grade nano devices, the V2 designator for IGLOO devices, and packages where space is physically limited. Packages that have limited characters available are UC36, UC81, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

Figure 1 shows an example of device marking based on the AGLN250V2-CSG81. The actual mark will vary by the device/package combination ordered.

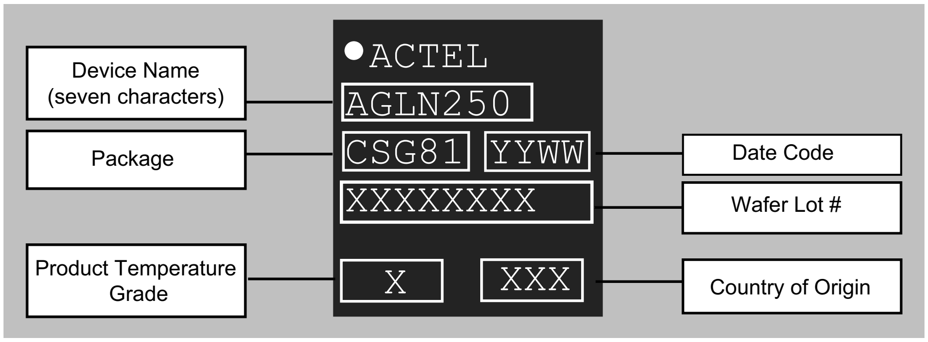

Figure 1 • **Example of Device Marking for Small Form Factor Packages**

IGLOO nano Products Available in the Z Feature Grade

IGLOO nano-Z Devices	AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
	QN48	–	–	–
	QN68	–	–	–
	UC81	–	–	–
	CS81	CS81	CS81	CS81
Packages	VQ100	VQ100	VQ100	VQ100

*Note: *Not recommended for new designs.*

Temperature Grade Offerings

	AGLN010	AGLN015*	AGLN020		AGLN060	AGLN125	AGLN250
Package				AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
UC36	C, I	–	–	–	–	–	–
QN48	C, I	–	–	C, I	–	–	–
QN68	–	C, I	C, I	C, I	–	–	–
UC81	–	–	C, I	C, I	–	–	–
CS81	–	–	C, I	C, I	C, I	C, I	C, I
VQ100	–	–	–	C, I	C, I	C, I	C, I

*Note: * Not recommended for new designs.*

C = Enhanced Commercial temperature range: –20°C to +85°C junction temperature
I = Industrial temperature range: –40°C to +100°C junction temperature

Contact your local Microsemi representative for device availability: http://www.microsemi.com/soc/contact/default.aspx.

Flash Advantages

Low Power

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

Security

Nonvolatile, flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO nano devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO nano device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Microsemi flash-based IGLOO nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano flash FPGAs enable the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (^\circ C) - \text{Max. ambient temp. } (^\circ C)}{\theta_{ja}(^\circ C/W)} = \frac{100^\circ C - 70^\circ C}{20.5^\circ C/W} = 1.46\text{ W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Chip Scale Package (CSP)	36	TBD	TBD	TBD	TBD	C/W
	81	TBD	TBD	TBD	TBD	C/W
Quad Flat No Lead (QFN)	48	TBD	TBD	TBD	TBD	C/W
	68	TBD	TBD	TBD	TBD	C/W
	100	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**
For IGLOO nano V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C) –40°C	–20°C	0°C	25°C	70°C	85°C	100°C
1.425	0.947	0.956	0.965	0.978	1.000	1.009	1.013
1.5	0.875	0.883	0.892	0.904	0.925	0.932	0.937
1.575	0.821	0.829	0.837	0.848	0.868	0.875	0.879

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to IGLOO nano I/O Banks

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3 V LVTTL / 3.3 V LVCMOS	3.3	16.38
3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.89
3.3 V LVCMOS Wide Range[2]	3.3	16.38
3.3 V LVCMOS Wide Range – Schmitt Trigger	3.3	18.89
2.5 V LVCMOS	2.5	4.71
2.5 V LVCMOS – Schmitt Trigger	2.5	6.13
1.8 V LVCMOS	1.8	1.64
1.8 V LVCMOS – Schmitt Trigger	1.8	1.79
1.5 V LVCMOS (JESD8-11)	1.5	0.97
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.96
1.2 V LVCMOS[3]	1.2	0.57
1.2 V LVCMOS – Schmitt Trigger[3]	1.2	0.52
1.2 V LVCMOS Wide Range[3]	1.2	0.57
1.2 V LVCMOS Wide Range – Schmitt Trigger[3]	1.2	0.52

Notes:

1. *PAC9 is the total dynamic power measured on V_{CCI}.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*

Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to IGLOO nano I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	107.98
3.3 V LVCMOS Wide Range[3]	5	3.3	107.98
2.5 V LVCMOS	5	2.5	61.24
1.8 V LVCMOS	5	1.8	31.28
1.5 V LVCMOS (JESD8-11)	5	1.5	21.50
1.2 V LVCMOS[4]	5	1.2	15.22

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
4. *Applicable for IGLOO nano V2 devices operating at VCCI ≥ VCC.*

Power Consumption of Various Internal Resources

Table 2-15 • **Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	4.421	4.493	2.700	0	0	0
PAC2	Clock contribution of a Global Spine	2.704	1.976	1.982	4.002	4.002	2.633
PAC3	Clock contribution of a VersaTile row	1.496	1.504	1.511	1.346	1.346	1.340
PAC4	Clock contribution of a VersaTile used as a sequential module	0.152	0.153	0.153	0.148	0.148	0.143
PAC5	First contribution of a VersaTile used as a sequential module	0.057					
PAC6	Second contribution of a VersaTile used as a sequential module	0.207					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.17					
PAC8	Average contribution of a routing net	0.7					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9.					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14.					
PAC11	Average contribution of a RAM block during a read operation	25.00			N/A		
PAC12	Average contribution of a RAM block during a write operation	30.00			N/A		
PAC13	Dynamic contribution for PLL	2.70			N/A		

Table 2-16 • **Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device -Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8					
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7					
PDC4 [1]	Static PLL contribution	1.84			N/A		
PDC5	Bank quiescent power (VCCI-dependent)[2]	See Table 2-12 on page 2-8					

Notes:

1. *Minimum contribution of the PLL when running at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 8 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
–20°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL / LVCMOS (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Applies to 1.2 V DC Core Voltage

Table 2-49 • **2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
4 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
6 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns
8 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-50 • **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
4 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
6 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
8 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-75 • Output Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-87 • Register Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Global Resource Characteristics

AGLN125 Clock Tree Topology

Clock delays are device-specific. Figure 2-25 is an example of a global tree used for clock routing. The global tree presented in Figure 2-25 is driven by a CCC located on the west side of the AGLN125 device. It is used to drive all D-flip-flops in the device.

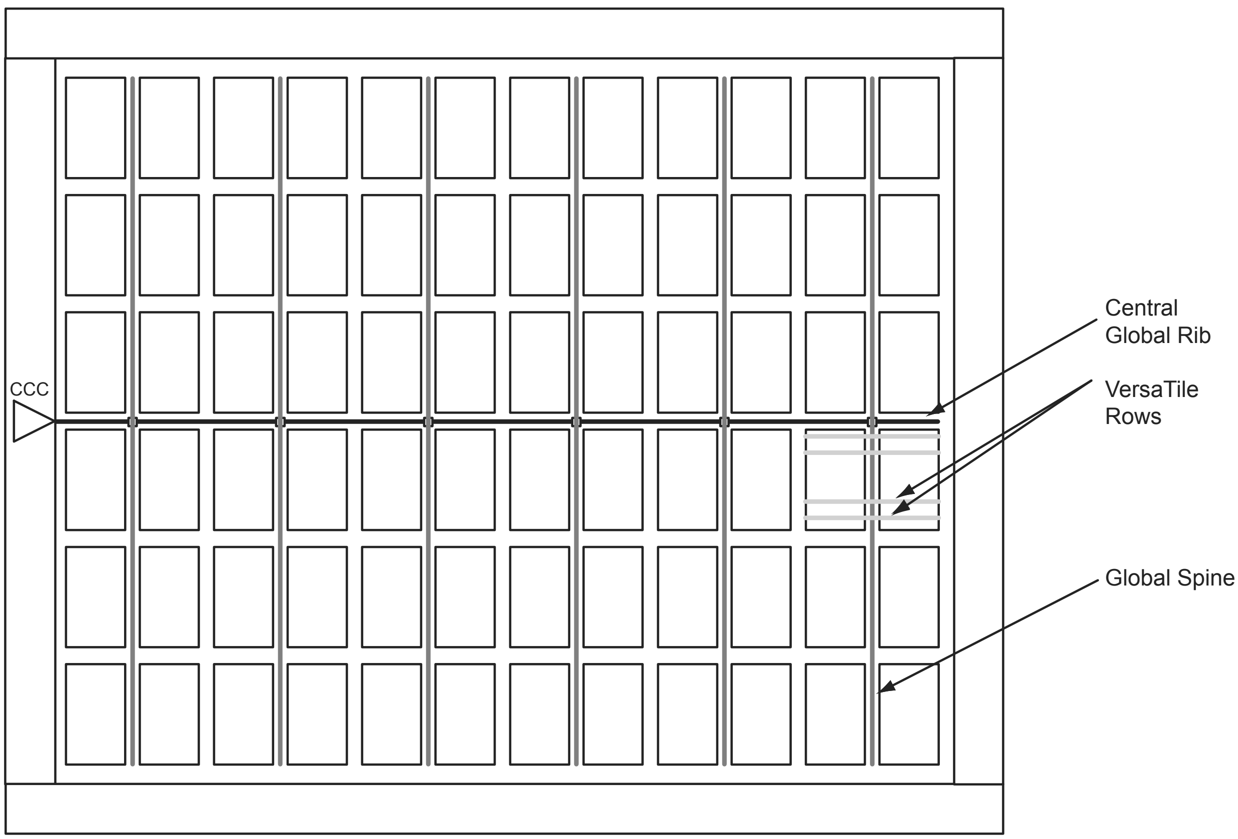

Figure 2-25 • **Example of Global Tree Use in an AGLN125 Device for Clock Routing**

Table 2-92 • AGLN125 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-93 • AGLN250 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-101* • IGLOO nano CCC/PLL Specification For IGLOO nano V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]			580[3]		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Serial Clock (SCLK) for Dynamic PLL [4,9]				60	
Input Cycle-to-Cycle Jitter (peak magnitude)				0.25	ns
Acquisition Time					
	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter [5]					
	LockControl = 0			4	ns
	LockControl = 1			3	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]		2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]		0.025		20.86	ns
Delay Range in Block: Fixed Delay [1, 2]			5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6]		Max Peak-to-Peak Period Jitter [6,7,8]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16	
0.75 MHz to 50MHz	0.50	1.20	2.00	3.00	%
50 MHz to 100 MHz	2.50	5.00	7.00	15.00	%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.2 V.*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.*
7. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
8. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO nano FPGA Fabric User's Guide.*
9. *The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.*

***Table 2-103* • RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.61	ns
t_{ENH}	REN, WEN hold time	0.07	ns
t_{DS}	Input data (WD) setup time	0.59	ns
t_{DH}	Input data (WD) hold time	0.30	ns
t_{CKQ1}	Clock HIGH to new data valid on RD (output retained)	3.51	ns
t_{CKQ2}	Clock HIGH to new data valid on RD (pipelined)	1.43	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	1.72	ns
	RESET Low to data out Low on RD (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	0.51
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

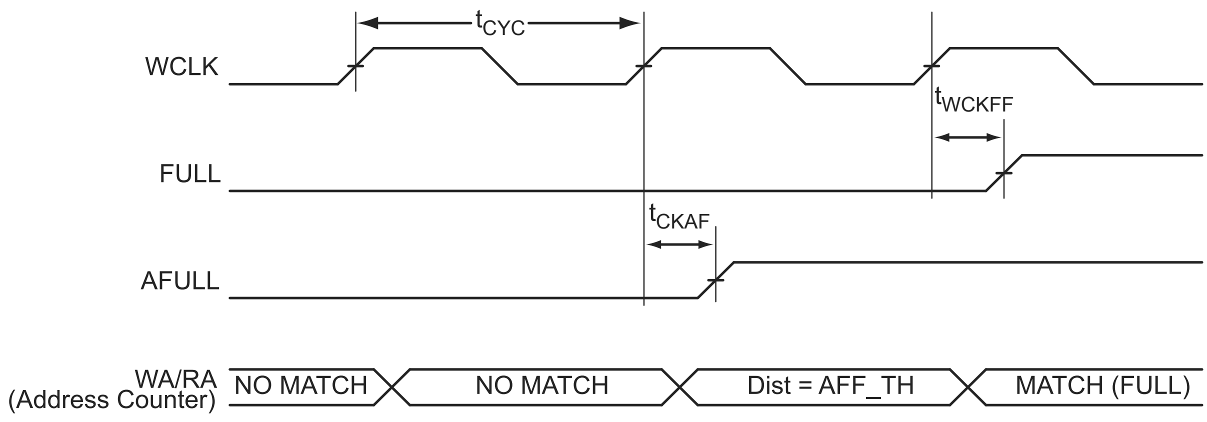

***Figure 2-38* • FIFO FULL Flag and AFULL Flag Assertion**

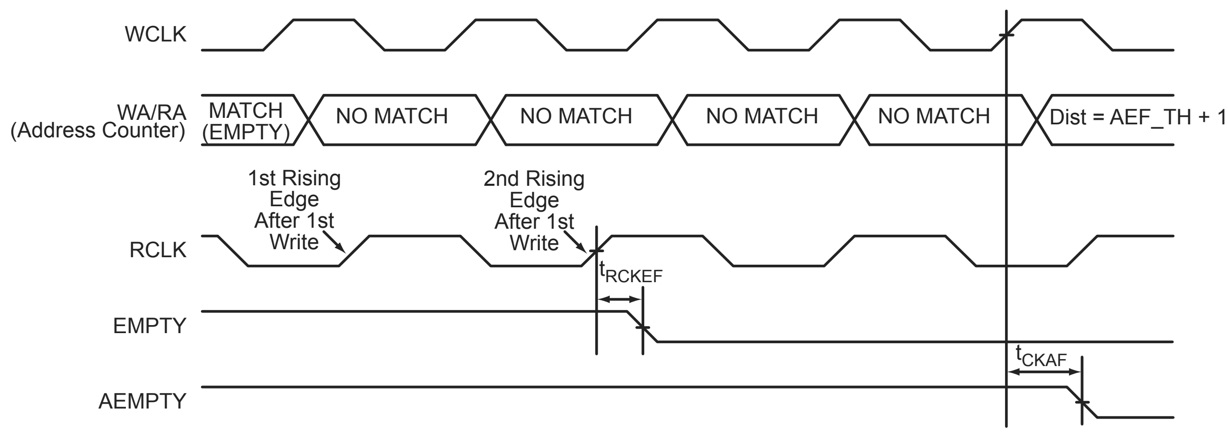

***Figure 2-39* • FIFO EMPTY Flag and AEMPTY Flag Deassertion**

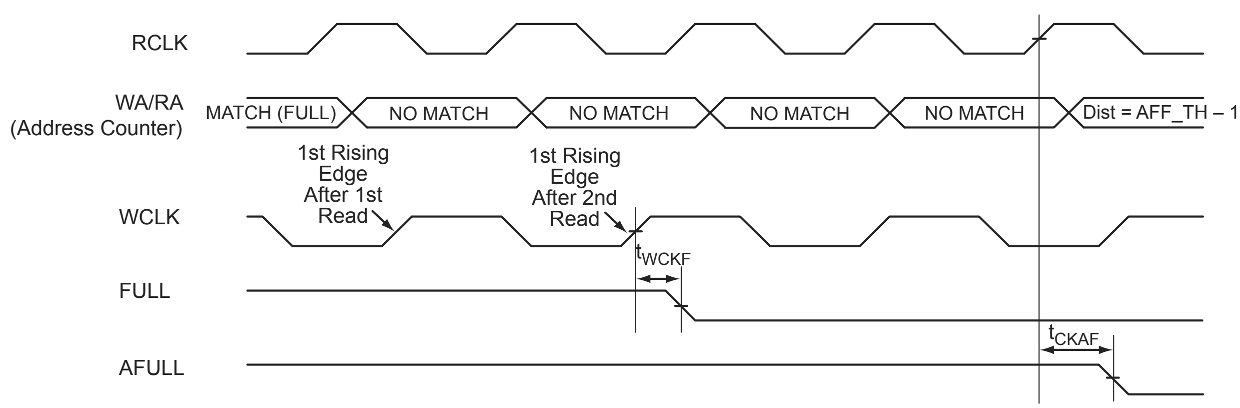

***Figure 2-40* • FIFO FULL Flag and AFULL Flag Deassertion**

Embedded FlashROM Characteristics

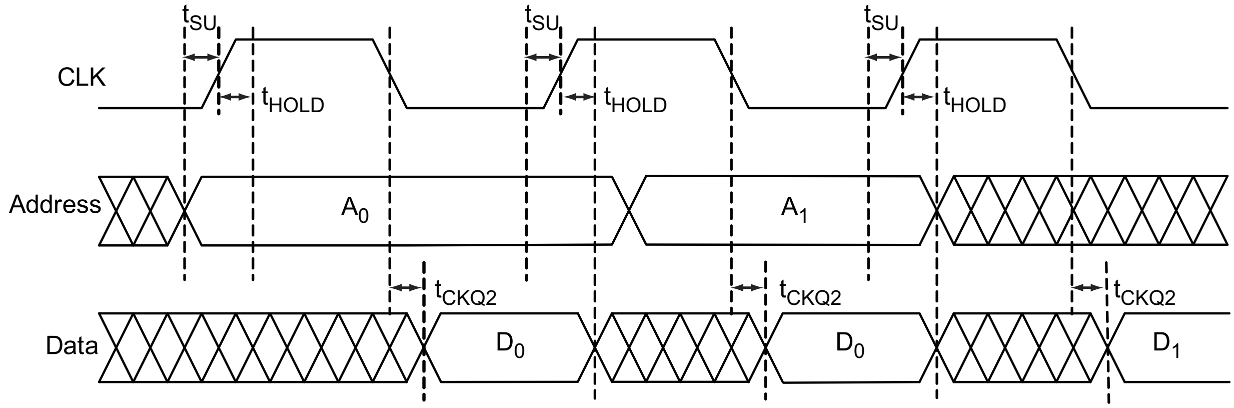

Figure 2-41 **• Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-108 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	20.90	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-109 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	35.74	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-110* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-111* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VQ100	
Pin Number	AGLN125Z Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1

VQ100	
Pin Number	AGLN125Z Function
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0

VQ100	
Pin Number	AGLN125Z Function
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

Revision / Version	Changes	Page
Revision 9 (Mar2010) Product Brief Advance v0.9 Packaging Advance v0.8	All product tables and pin tables were updated to show clearly that AGLN030 is available only in the Z feature grade at this time. The nano-Z feature grade devices are designated with a Z at the end of the part number.	N/A
Revision 8 (Jan 2009)	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance".	I
Product Brief Advance v0.8	The note for AGLN030 in the "IGLOO nano Devices" table and "I/Os Per Package" table was revised to remove the statement regarding package compatibility with lower density nano devices.	II, II
	The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing.	1-8
Packaging Advance v0.7	The "UC81", "CS81", "QN48", and "QN68" pin tables for AGLN030 are new.	4-5, 4-8, 4-17, 4-21
	The "CS81"pin table for AGLN060 is new.	4-9
	The "CS81" and "VQ100" pin tables for AGLN060Z are new.	4-10, 4-25
	The "CS81" and "VQ100" pin tables for AGLN125Z are new.	4-12, 4-27
	The "CS81" and "VQ100" pin tables for AGLN250Z is new.	4-14, 4-29
Revision 7 (Apr 2009) Product Brief Advance v0.7 DC and Switching Characteristics Advance v0.3	The –F speed grade is no longer offered for IGLOO nano devices and was removed from the datasheet.	N/A
Revision 6 (Mar 2009) Packaging Advance v0.6	The "VQ100" pin table for AGLN030 is new.	4-23
Revision 5 (Feb 2009) Packaging Advance v0.5	The "100-Pin QFN" section was removed.	N/A
Revision 4 (Feb 2009)	The QN100 package was removed for all devices.	N/A
Product Brief Advance v0.6	"IGLOO nano Devices" table was updated to change the maximum user I/Os for AGLN030 from 81 to 77.	II
	The "Device Marking" section is new.	V
Revision 3 (Feb 2009) Product Brief Advance v0.5	The following table note was removed from "IGLOO nano Devices" table: "Six chip (main) and three quadrant global networks are available for AGLN060 and above."	II
	The CS81 package was added for AGLN250 in the "IGLOO nano Products Available in the Z Feature Grade" table.	VI
Packaging Advance v0.4	The "UC81" and "CS81" pin tables for AGLN020 are new.	4-4, 4-7
	The "CS81" pin table for AGLN250 is new.	4-13

Revision / Version	Changes	Page
Revision 1 (cont'd)	The "QN48" pin diagram was revised.	4-16
Packaging Advance v0.2	Note 2 for the "QN48", "QN68", and "100-Pin QFN" pin diagrams was changed to "The die attach paddle of the package is tied to ground (GND)."	4-16, 4-19
	The "VQ100" pin diagram was revised to move the pin IDs to the upper left corner instead of the upper right corner.	4-23
Revision 0 (Oct 2008) Product Brief Advance v0.2	The following tables and sections were updated to add the UC81 and CS81 packages for AGL030: "IGLOO nano Devices" "I/Os Per Package" "IGLOO nano Products Available in the Z Feature Grade" "Temperature Grade Offerings"	N/A
	The "I/Os Per Package" table was updated to add the following information to table note 4: "For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only."	II
	The "IGLOO nano Products Available in the Z Feature Grade" section was updated to remove QN100 for AGLN250.	VI
	The device architecture figures, Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125) through Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250), were revised. Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030) is new.	1-4 through 1-5
	The "PLL and CCC" section was revised to include information about CCC-GLs in AGLN020 and smaller devices.	1-7
	The "I/Os with Advanced I/O Standards" section was revised to add information about IGLOO nano devices supporting double-data-rate applications.	1-8