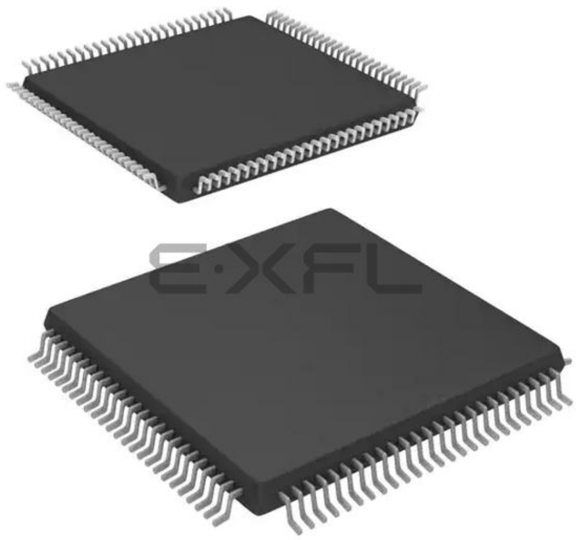

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	71
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln060v2-vqg100i

IGLOO nano Ordering Information

AGLN250 V2 – Z VQ G 100 Y I

- **Application (Temperature Range)**
  - Blank = Enhanced Commercial (–20°C to +85°C Junction Temperature)
  - I = Industrial (–40°C to +100°C Junction Temperature)
  - PP = Pre-Production
  - ES = Engineering Sample (Room Temperature Only)
- **Security Feature**
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
  - Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

  Note: Only devices with packages greater than or equal to 5x5 are supported.
- **Package Lead Count**
- **Lead-Free Packaging**
  - Blank = Standard Packaging
  - G = RoHS-Compliant Packaging
- **Package Type**
  - UC = Micro Chip Scale Package (0.4 mm pitch)
  - CS = Chip Scale Package (0.5 mm pitch)
  - QN = Quad Flat Pack No Leads (0.4 mm and 0.5 mm pitches)
  - VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
  - DIELOT = Known Good Die
- Z = nano devices without enhanced features[1]
  - Blank = Standard
- **Supply Voltage**
  - 2 = 1.2 V to 1.5 V
  - 5 = 1.5 V only
- **Part Number**

IGLOO nano Devices

AGLN010 = 10,000 System Gates
AGLN015 = 15,000 System Gates (AGLN015 is not recommended for new designs)
AGLN020 = 20,000 System Gates
AGLN030 = 30,000 System Gates
AGLN060 = 60,000 System Gates
AGLN125 = 125,000 System Gates
AGLN250 = 250,000 System Gates

Notes:

1. *Z-feature grade devices AGLN060Z, AGLN125Z, and AGLN250Z do not support the enhanced nano features of Schmitt Trigger input, bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, hot-swap I/O capability and 1.2 V programming. The AGLN030 Z feature grade does not support Schmitt trigger input, bus hold and 1.2 V programming. For the VQ100, CS81, UC81, QN68, and QN48 packages, the Z feature grade and the N part number are not marked on the device. Z feature grade devices are not recommended for new designs.*
2. *AGLN030 is available in the Z feature grade only.*
3. *Marking Information: IGLOO nano V2 devices do not have a V2 marking, but IGLOO nano V5 devices are marked with a V5 designator.*

Devices Not Recommended For New Designs

AGLN015, AGLN030Z, AGLN060Z, AGLN125Z, and AGLN250Z are not recommended for new designs. For more information on obsoleted devices/packages, refer to the *PDN1503 - IGLOO nano Z and ProASIC3 nano Z Families*.

Flash Advantages

Low Power

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

Security

Nonvolatile, flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO nano devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO nano device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Microsemi flash-based IGLOO nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano flash FPGAs enable the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO nano devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic.

Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO nano device architecture mitigates the need for ASIC migration at higher user volumes. This makes IGLOO nano devices cost-effective ASIC replacement solutions, especially for applications in the consumer, networking/communications, computing, and avionics markets.

With a variety of devices under $1, IGLOO nano FPGAs enable cost-effective implementation of programmable logic and quick time to market.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO nano flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO nano FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO nano device offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO nano FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO nano architecture provides granularity comparable to standard-cell ASICs. The IGLOO nano device consists of five distinct and programmable architectural features (Figure 1-3 on page 1-5 to Figure 1-4 on page 1-5):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO nano core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

† The AGLN030 and smaller devices do not support PLL or SRAM.

User Nonvolatile FlashROM

IGLOO nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGLN030 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO nano development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Microsemi Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOO nano devices (except the AGLN030 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGLN030 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

Higher density IGLOO nano devices using either the two I/O bank or four I/O bank architectures provide designers with very flexible clock conditioning capabilities. AGLN060, AGLN125, and AGLN250 contain six CCCs. One CCC (center west side) has a PLL. The AGLN030 and smaller devices use different CCCs in their architecture (CCC-GL). These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these are located at the four corners and the centers of the east and west sides. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-7 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

Figure 1-7 • **I/O States During Programming Window**

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.14 V) For IGLOO nano V2, 1.2 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature (°C)						
	–40°C	–20°C	0°C	25°C	70°C	85°C	100°C
1.14	0.968	0.974	0.979	0.991	1.000	1.006	1.009
1.2	0.863	0.868	0.873	0.884	0.892	0.898	0.901
1.26	0.792	0.797	0.801	0.811	0.819	0.824	0.827

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microsemi recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, IGLOO nano Flash*Freeze Mode***

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25°C)	1.2 V	1.9	3.3	3.3	8	13	20	µA
	1.5 V	5.8	6	6	10	18	34	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-9 through Table 2-14 on page 2-9 and Table 2-15 on page 2-10 through Table 2-18 on page 2-11 (PDC6 and PDC7).*

Applies to 1.2 V DC Core Voltage

Table 2-43 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 µA	4 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 µA	6 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns
100 µA	8 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-44 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 µA	4 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 µA	6 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
100 µA	8 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Applies to 1.2 V DC Core Voltage

Table 2-49 • **2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
4 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
6 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns
8 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-50 • **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
4 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
6 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
8 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-59 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.39	0.19	1.19	1.62	0.66	5.48	5.39	2.02	2.06	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-60 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.39	0.19	1.19	1.62	0.66	2.44	2.24	2.02	2.15	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Applies to 1.2 V DC Core Voltage

Table 2-61 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	5.87	0.26	1.27	1.77	1.10	5.92	5.87	2.45	2.65	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-62 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.78	0.26	1.27	1.77	1.10	2.82	2.62	2.44	2.74	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Input Register

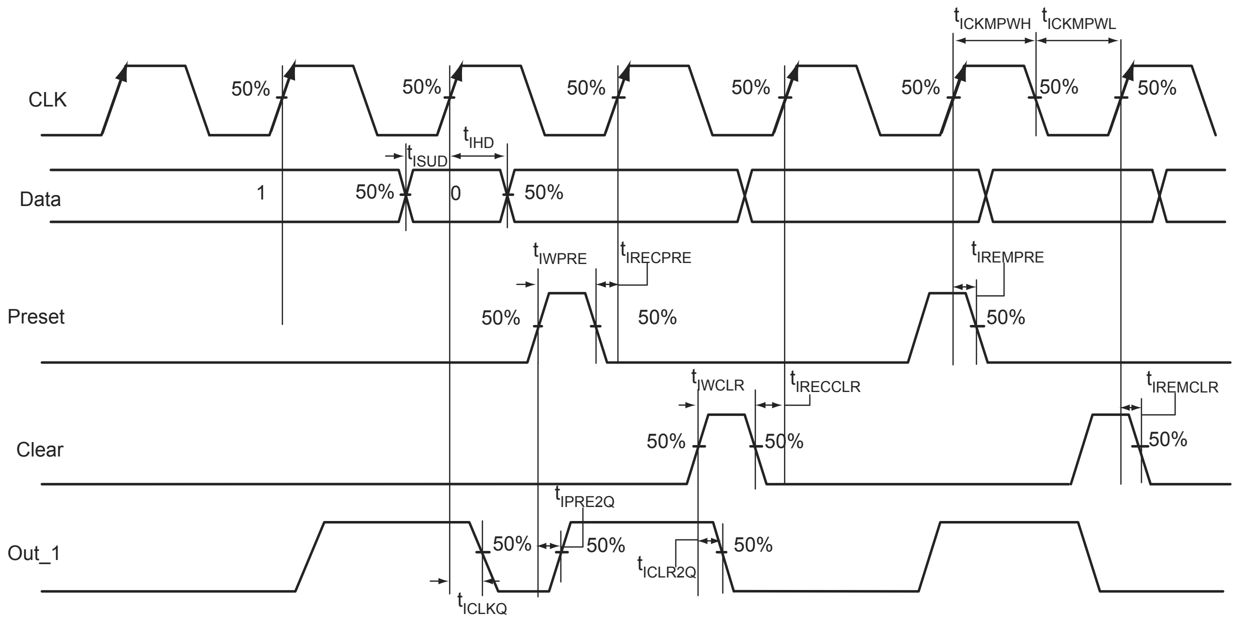


Figure 2-14 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-72 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-83 • Output DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO nano library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for Software v10.1*.

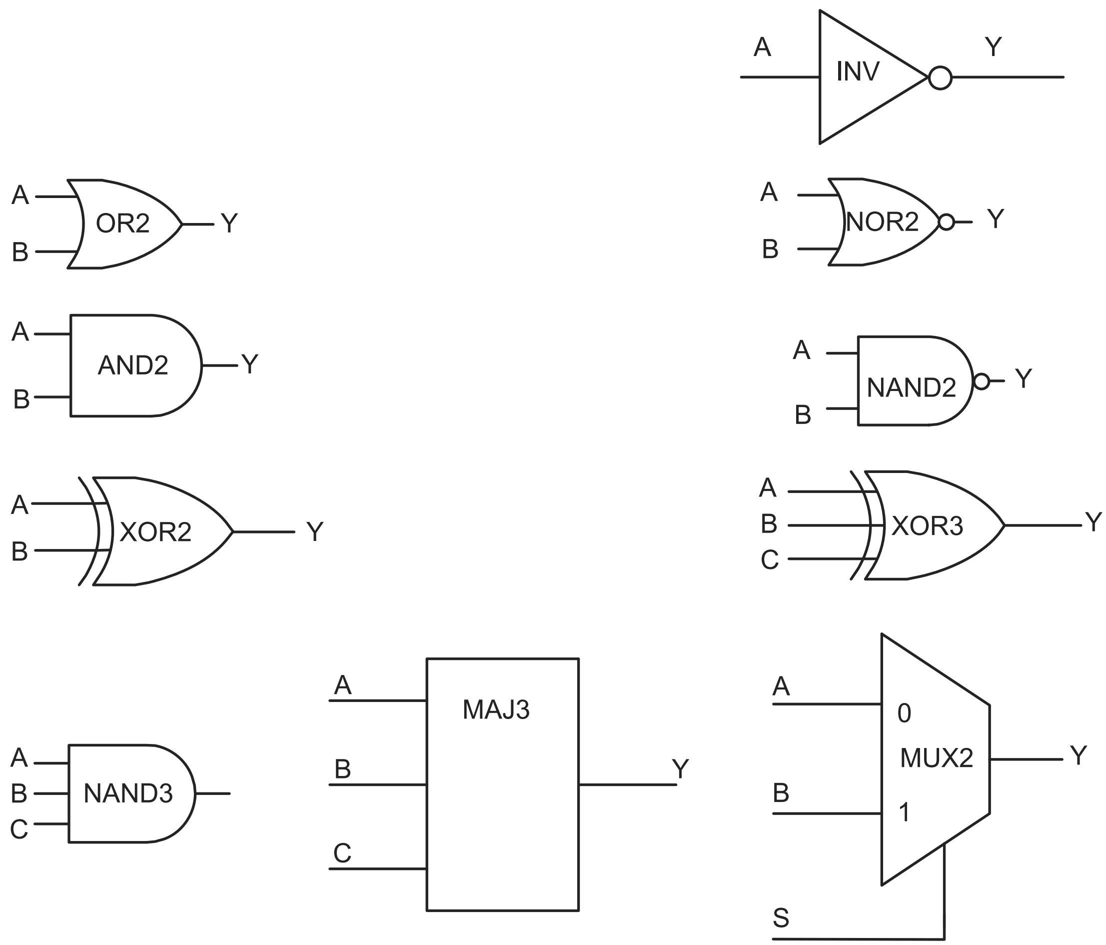


***Figure 2-21 •* Sample of Combinatorial Cells**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-84 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.76	ns
AND2	Y = A · B	t_{PD}	0.87	ns
NAND2	Y = !(A · B)	t_{PD}	0.91	ns
OR2	Y = A + B	t_{PD}	0.90	ns
NOR2	Y = !(A + B)	t_{PD}	0.94	ns
XOR2	Y = A ⊕ B	t_{PD}	1.39	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.44	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.60	ns
MUX2	Y = A !S + B S	t_{PD}	1.17	ns
AND3	Y = A · B · C	t_{PD}	1.18	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-85 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.33	ns
AND2	Y = A · B	t_{PD}	1.48	ns
NAND2	Y = !(A · B)	t_{PD}	1.58	ns
OR2	Y = A + B	t_{PD}	1.53	ns
NOR2	Y = !(A + B)	t_{PD}	1.63	ns
XOR2	Y = A ⊕ B	t_{PD}	2.34	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.59	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	2.74	ns
MUX2	Y = A !S + B S	t_{PD}	2.03	ns
AND3	Y = A · B · C	t_{PD}	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-90 • AGLN020 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-91 • AGLN060 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
t_{RCKH}	Input High Delay for Global Clock	1.34	1.71	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.38	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Embedded SRAM and FIFO Characteristics

SRAM

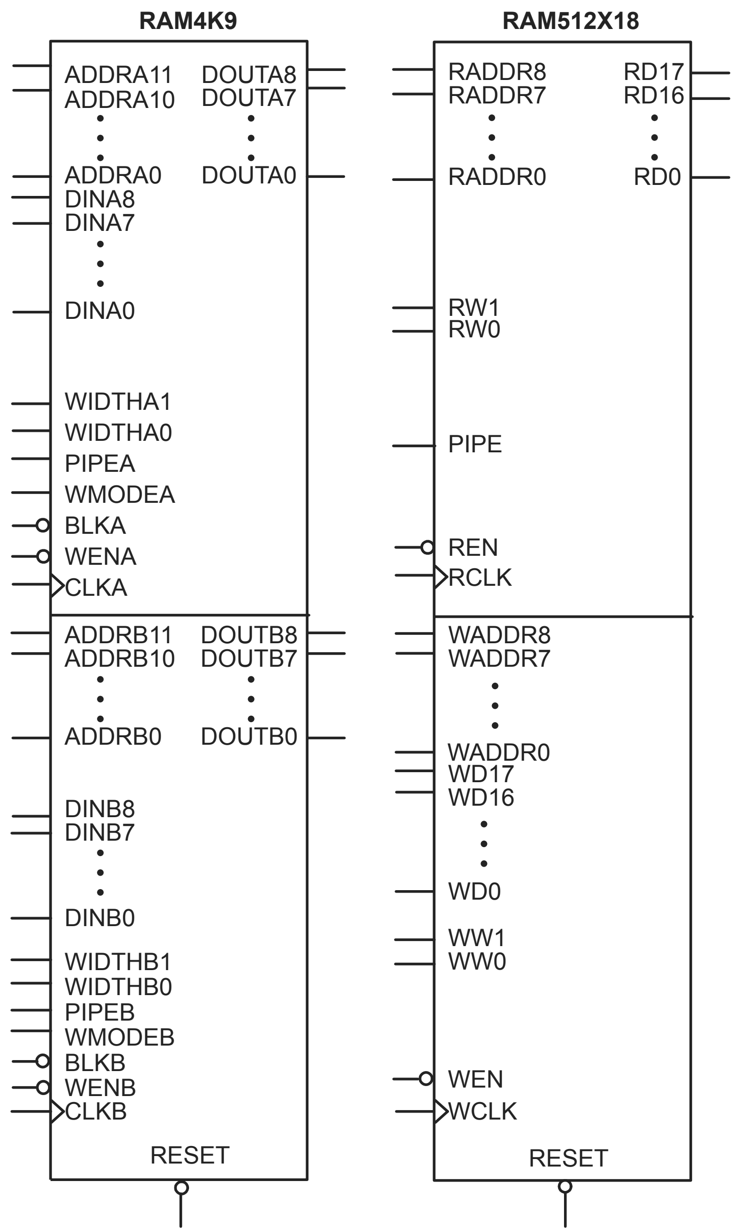


Figure 2-27 • **RAM Models**

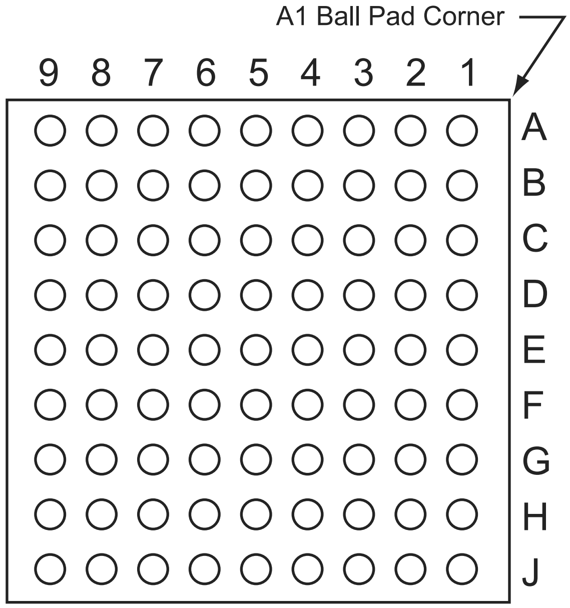
Table 2-105 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.13	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{DS}	Input data (WD) setup time	1.10	ns
t_{DH}	Input data (WD) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	6.56	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	2.67	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.87	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.04	ns
t_{RSTBQ}	RESET LOW to data out LOW on RD (flow through)	3.21	ns
	RESET LOW to data out LOW on RD (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

UC81



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS81	
Pin Number	AGLN020 Function
A1	IO64RSB2
A2	IO54RSB2
A3	IO57RSB2
A4	IO36RSB1
A5	IO32RSB1
A6	IO24RSB1
A7	IO20RSB1
A8	IO04RSB0
A9	IO08RSB0
B1	IO59RSB2
B2	IO55RSB2
B3	IO62RSB2
B4	IO34RSB1
B5	IO28RSB1
B6	IO22RSB1
B7	IO18RSB1
B8	IO00RSB0
B9	IO03RSB0
C1	IO51RSB2
C2	IO50RSB2
C3	NC
C4	NC
C5	NC
C6	NC
C7	NC
C8	IO10RSB0
C9	IO07RSB0
D1	IO49RSB2
D2	IO44RSB2
D3	NC
D4	VCC
D5	VCCIB2
D6	GND
D7	NC
D8	IO13RSB0
D9	IO12RSB0

CS81	
Pin Number	AGLN020 Function
E1	GEC0/IO48RSB2
E2	GEA0/IO47RSB2
E3	NC
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	NC
E8	GDA0/IO15RSB0
E9	GDC0/IO14RSB0
F1	IO46RSB2
F2	IO45RSB2
F3	NC
F4	GND
F5	VCCIB1
F6	NC
F7	NC
F8	IO16RSB0
F9	IO17RSB0
G1	IO43RSB2
G2	IO42RSB2
G3	IO41RSB2
G4	IO31RSB1
G5	NC
G6	IO21RSB1
G7	NC
G8	VJTAG
G9	TRST
H1	IO40RSB2
H2	FF/IO39RSB1
H3	IO35RSB1
H4	IO29RSB1
H5	IO26RSB1
H6	IO25RSB1
H7	IO19RSB1
H8	TDI
H9	TDO

CS81	
Pin Number	AGLN020 Function
J1	IO38RSB1
J2	IO37RSB1
J3	IO33RSB1
J4	IO30RSB1
J5	IO27RSB1
J6	IO23RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	AGLN125 Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO13RSB0
A5	IO22RSB0
A6	IO32RSB0
A7	GBB0/IO37RSB0
A8	GBA1/IO40RSB0
A9	GBA2/IO41RSB0
B1	GAA2/IO132RSB1
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO11RSB0
B5	IO25RSB0
B6	GBC0/IO35RSB0
B7	GBB1/IO38RSB0
B8	IO42RSB0
B9	GBB2/IO43RSB0
C1	GAB2/IO130RSB1
C2	IO131RSB1
C3	GND
C4	IO15RSB0
C5	IO28RSB0
C6	GND
C7	GBA0/IO39RSB0
C8	GBC2/IO45RSB0
C9	IO47RSB0
D1	GAC2/IO128RSB1
D2	IO129RSB1
D3	GFA2/IO117RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO59RSB0
D8	GCC1/IO51RSB0
D9	GCC0/IO52RSB0
E1	GFB0/IO120RSB1
E2	GFB1/IO121RSB1
E3	GFA1/IO118RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GCA0/IO56RSB0
E8	GCA1/IO55RSB0
E9	GCB2/IO58RSB0
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO65RSB0
F8	GDC1/IO61RSB0
F9	GDC0/IO62RSB0
G1	GEA0/IO104RSB1
G2	GEC0/IO108RSB1
G3	GEB1/IO107RSB1
G4	IO96RSB1
G5	IO92RSB1
G6	IO72RSB1
G7	GDB2/IO68RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO105RSB1
H2	FF/GEB2/IO102RSB1
H3	IO99RSB1
H4	IO94RSB1
H5	IO91RSB1
H6	IO81RSB1
H7	GDA2/IO67RSB1
H8	TDI
H9	TDO
J1	GEA2/IO103RSB1
J2	GEC2/IO101RSB1
J3	IO97RSB1
J4	IO93RSB1
J5	IO90RSB1
J6	IO78RSB1
J7	TCK
J8	TMS
J9	VPUMP

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN125-CS81.*

CS81	
Pin Number	AGLN250Z Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO12RSB0
A7	GBB0/IO16RSB0
A8	GBA1/IO19RSB0
A9	GBA2/IO20RSB1
B1	GAA2/IO67RSB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO06RSB0
B5	IO10RSB0
B6	GBC0/IO14RSB0
B7	GBB1/IO17RSB0
B8	IO21RSB1
B9	GBB2/IO22RSB1
C1	GAB2/IO65RSB3
C2	IO66RSB3
C3	GND
C4	IO08RSB0
C5	IO11RSB0
C6	GND
C7	GBA0/IO18RSB0
C8	GBC2/IO23RSB1
C9	IO24RSB1
D1	GAC2/IO63RSB3
D2	IO64RSB3
D3	GFA2/IO56RSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO30RSB1
D8	GCC1/IO25RSB1
D9	GCC0/IO26RSB1

CS81	
Pin Number	AGLN250Z Function
E1	GFB0/IO59RSB3
E2	GFB1/IO60RSB3
E3	GFA1/IO58RSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1
E7	GCA0/IO28RSB1
E8	GCA1/IO27RSB1
E9	GCB2/IO29RSB1
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO33RSB1
F8	GDC1/IO31RSB1
F9	GDC0/IO32RSB1
G1	GEA0/IO51RSB3
G2	GEC1/IO54RSB3
G3	GEC0/IO53RSB3
G4	IO45RSB2
G5	IO42RSB2
G6	IO37RSB2
G7	GDB2/IO35RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO52RSB3
H2	FF/GEB2/IO49RSB2
H3	IO47RSB2
H4	IO44RSB2
H5	IO41RSB2
H6	IO39RSB2
H7	GDA2/IO34RSB2
H8	TDI
H9	TDO

CS81	
Pin Number	AGLN250Z Function
J1	GEA2/IO50RSB2
J2	GEC2/IO48RSB2
J3	IO46RSB2
J4	IO43RSB2
J5	IO40RSB2
J6	IO38RSB2
J7	TCK
J8	TMS
J9	VPUMP

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250Z-CS81.*