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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	60
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-20°C ~ 85°C (TJ)
Package / Case	81-WFBGA, CSBGA
Supplier Device Package	81-CSP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln060v5-csg81

IGLOO nano Device Status

IGLOO nano Devices	Status	IGLOO nano-Z Devices	Status
AGLN010	Production		
AGLN015	Not recommended for new designs.		
AGLN020	Production		
		AGLN030Z	Not recommended for new designs.
AGLN060	Production	AGLN060Z	Not recommended for new designs.
AGLN125	Production	AGLN125Z	Not recommended for new designs.
AGLN250	Production	AGLN250Z	Not recommended for new designs.

Flash*Freeze Technology

The IGLOO nano device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 μ s) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode.

Alternatively, I/Os can be set to a specific state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 2 μ W in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-5 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

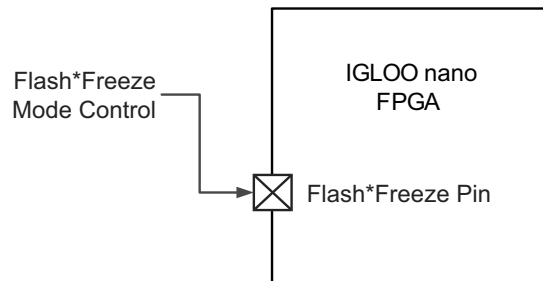


Figure 1-5 • IGLOO nano Flash*Freeze Mode

VersaTiles

The IGLOO nano core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The IGLOO nano VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-6 for VersaTile configurations.

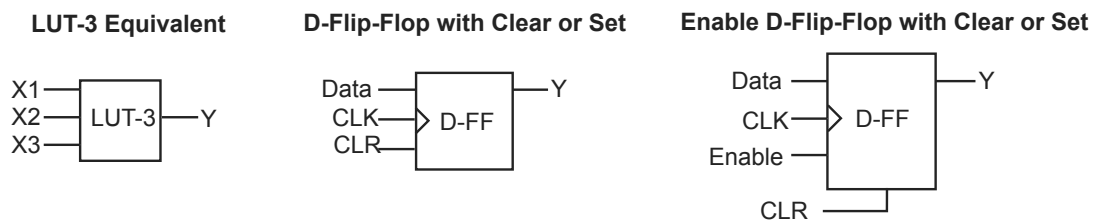


Figure 1-6 • VersaTile Configurations

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage

Parameter	Definition	Device-Specific Dynamic Power ($\mu\text{W}/\text{MHz}$)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	2.829	2.875	1.728	0	0	0
PAC2	Clock contribution of a Global Spine	1.731	1.265	1.268	2.562	2.562	1.685
PAC3	Clock contribution of a VersaTile row	0.957	0.963	0.967	0.862	0.862	0.858
PAC4	Clock contribution of a VersaTile used as a sequential module	0.098	0.098	0.098	0.094	0.094	0.091
PAC5	First contribution of a VersaTile used as a sequential module	0.045					
PAC6	Second contribution of a VersaTile used as a sequential module	0.186					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11					
PAC8	Average contribution of a routing net	0.45					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9					
PAC11	Average contribution of a RAM block during a read operation	25.00			N/A		
PAC12	Average contribution of a RAM block during a write operation	30.00			N/A		
PAC13	Dynamic contribution for PLL	2.10			N/A		

Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage

Parameter	Definition	Device-Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8					
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7					
PDC4 ¹	Static PLL contribution	0.90			N/A		
PDC5	Bank quiescent power (VCCI-dependent) ²	See Table 2-12 on page 2-8					

Notes:

1. Minimum contribution of the PLL when running at lowest frequency.
2. For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-19 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-20 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels
Applicable to Commercial and Industrial Conditions—Software Default Settings

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹	IOH ¹
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8 mA	High	-0.3	0.8	2	3.6	0.4	2.4	8	8
3.3 V LVCMOS Wide Range ³	100 μ A	8 mA	High	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	100 μ A	100 μ A
2.5 V LVCMOS	8 mA	8 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	4	4
1.5 V LVCMOS	2 mA	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS ⁴	1 mA	1 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1
1.2 V LVCMOS Wide Range ^{4,5}	100 μ A	1 mA	High	-0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI - 0.1	100 μ A	100 μ A

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.
4. Applicable to IGLOO nano V2 devices operating at VCCI \geq VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range, as specified in the JESD8-12 specification.

Table 2-22 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions

DC I/O Standards	Commercial ¹		Industrial ²	
	IIL ³	I IH ⁴	IIL ³	I IH ⁴
	μ A	μ A	μ A	μ A
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCOMS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS ⁵	10	10	15	15
1.2 V LVCMOS Wide Range ⁵	10	10	15	15

Notes:

1. Commercial range ($-20^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions, where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. I_{IL} is the input leakage current per I/O pin over recommended operating conditions, where $-0.3 \text{ V} < V_{IN} < V_{IL}$.
5. Applicable to IGLOO nano V2 devices operating at VCCI \geq VCC.

DDR Module Specifications

Note: DDR is not supported for AGLN010, AGLN015, and AGLN020 devices.

Input DDR Module

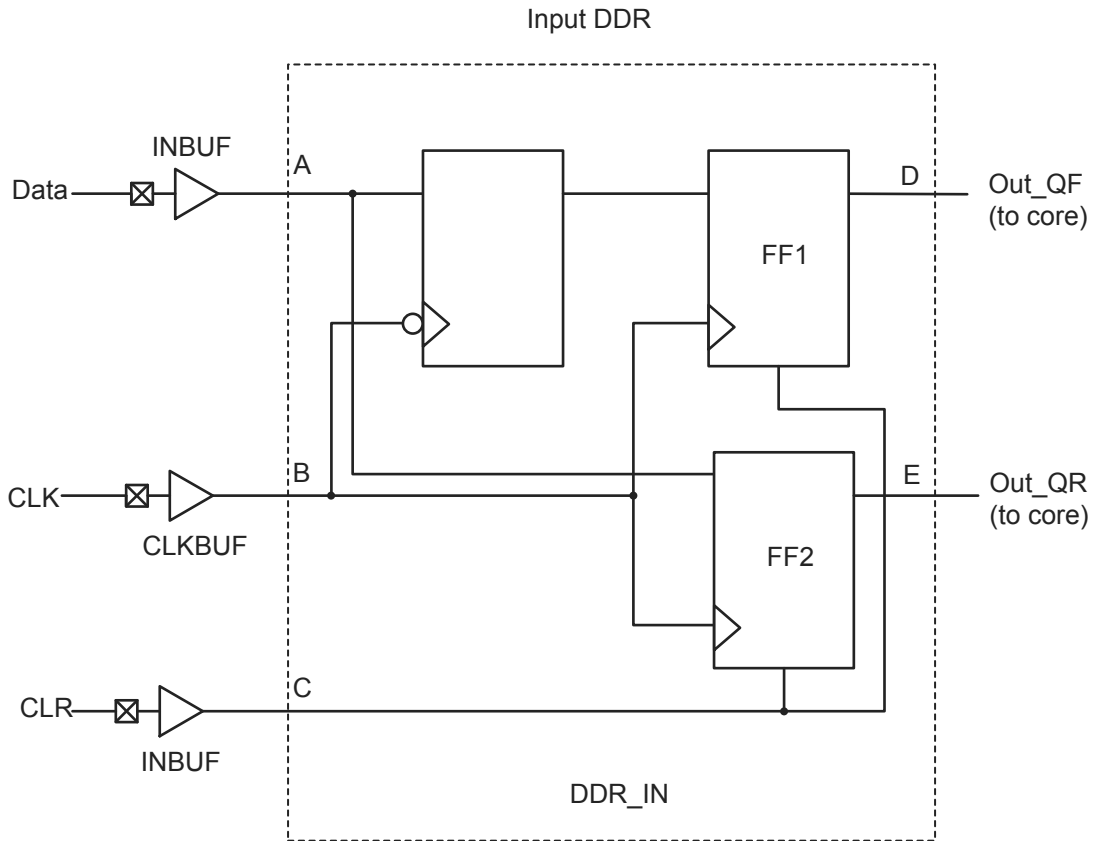


Figure 2-17 • Input DDR Timing Model

Table 2-78 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

1.2 V DC Core Voltage

Table 2-83 • Output DDR Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-92 • AGLN125 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-93 • AGLN250 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-96 • AGLN020 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.81	2.26	ns
t_{RCKH}	Input High Delay for Global Clock	1.90	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-97 • AGLN060 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.42	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Timing Waveforms

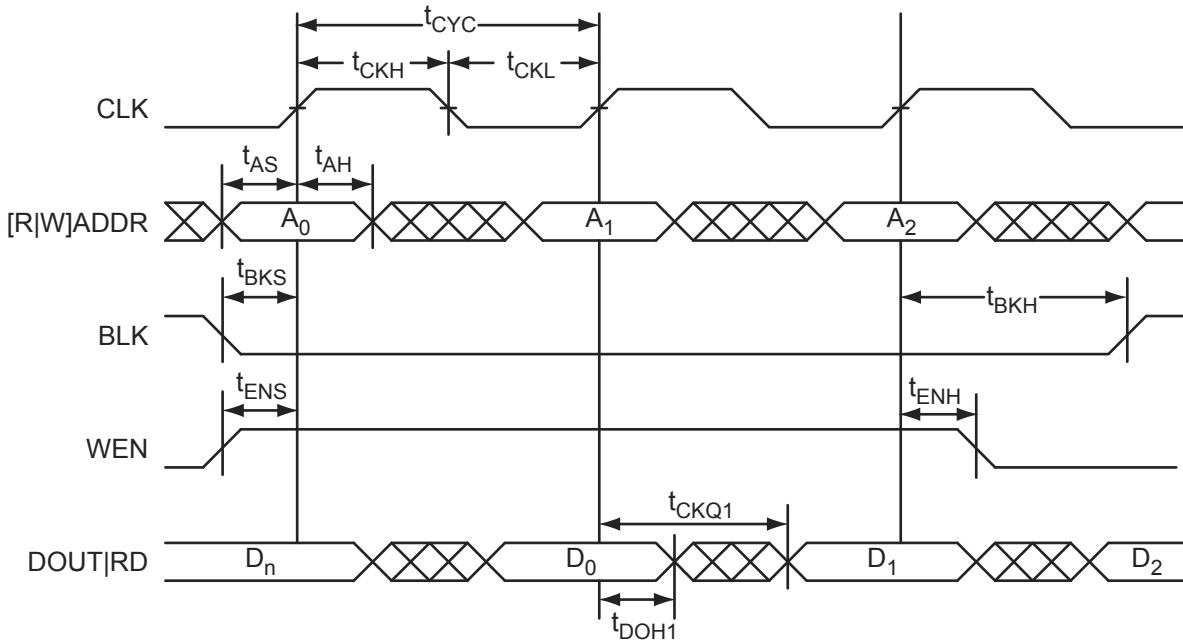


Figure 2-28 • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.

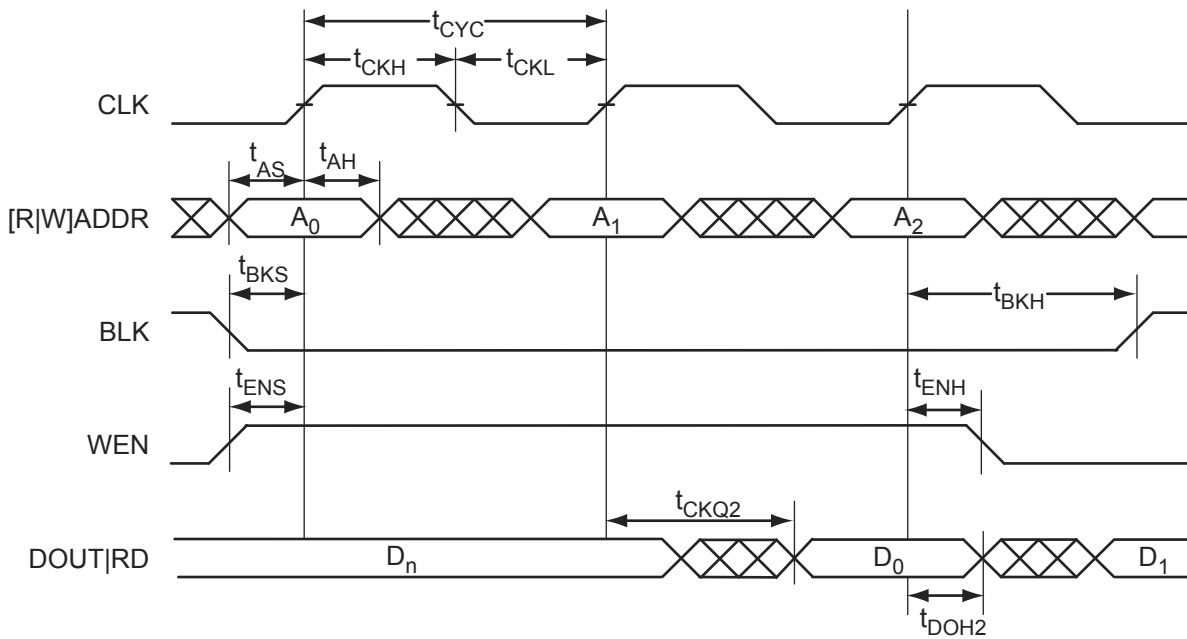


Figure 2-29 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.

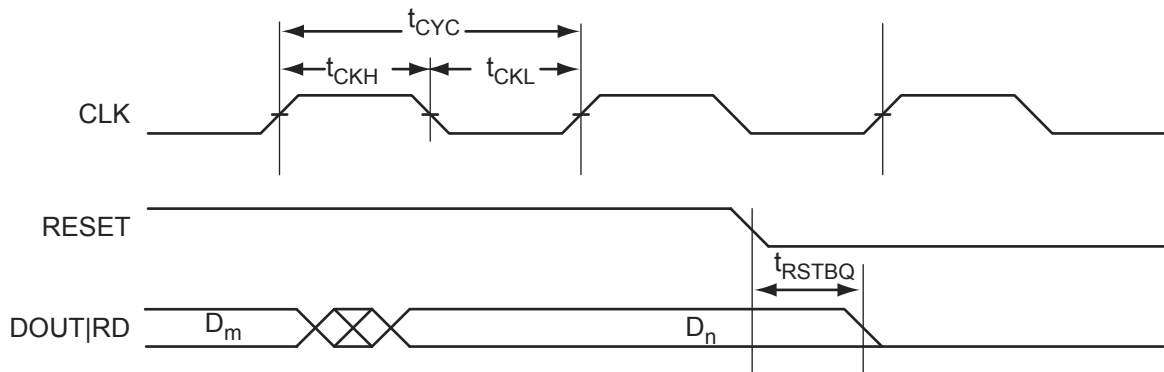


Figure 2-32 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.

Timing Waveforms

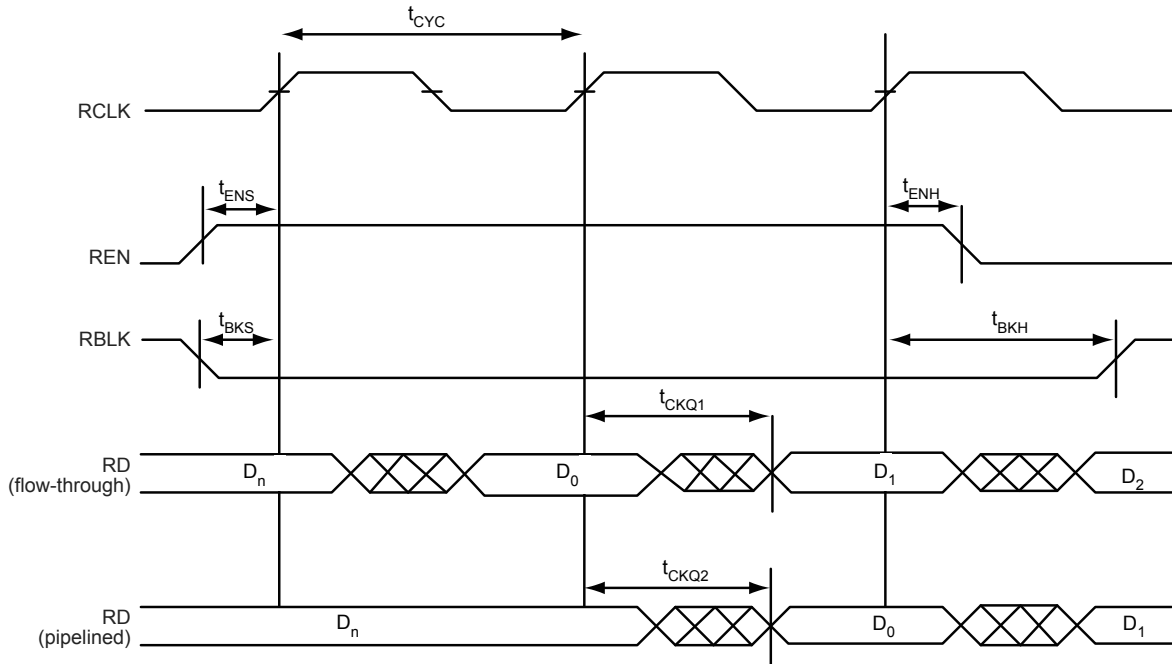


Figure 2-34 • FIFO Read

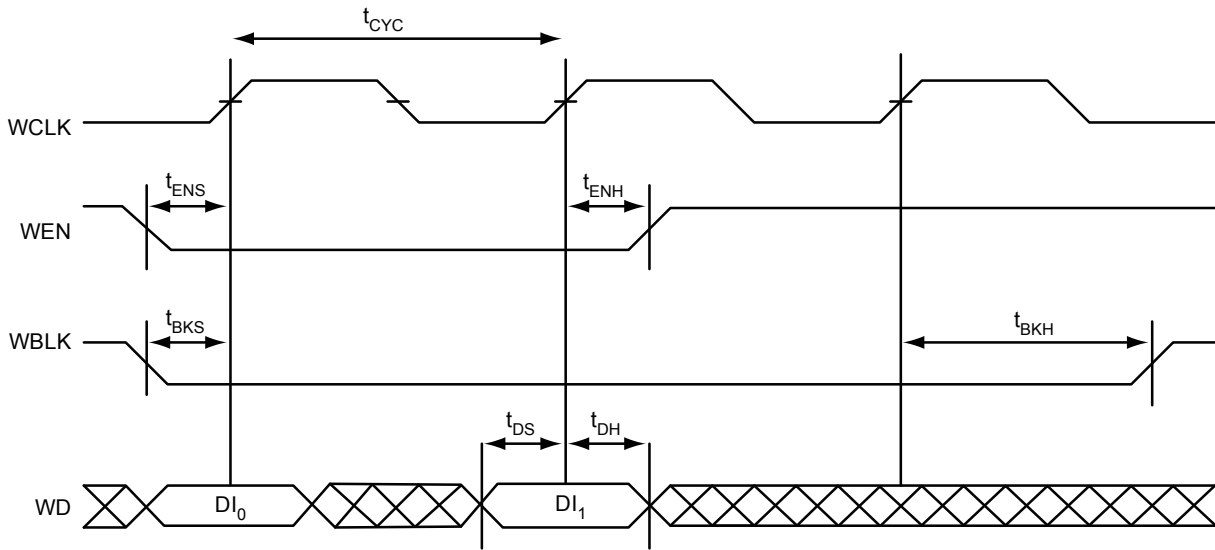


Figure 2-35 • FIFO Write

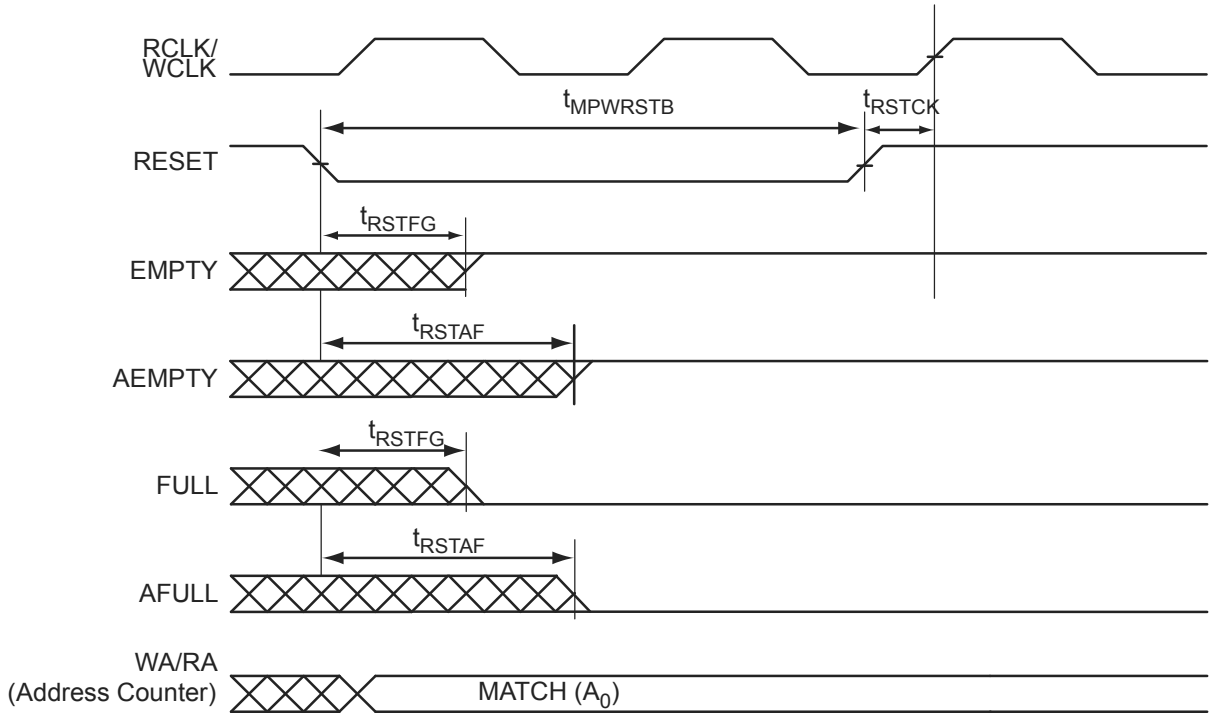


Figure 2-36 • FIFO Reset

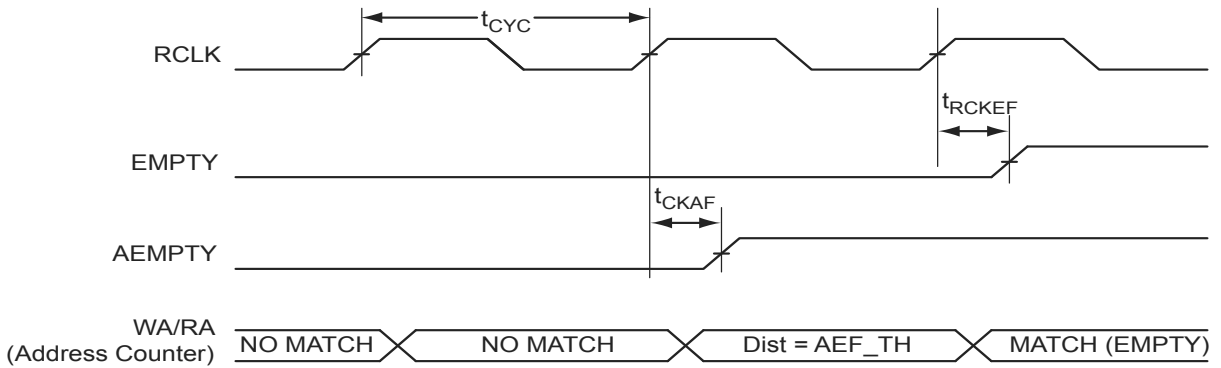


Figure 2-37 • FIFO EMPTY Flag and AEMPTY Flag Assertion

1.2 V DC Core Voltage

Table 2-107 • FIFO
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.30	ns
t_{DH}	Input Data (DI) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET LOW to Data Out Low on RD (flow-through)	3.41	ns
	RESET LOW to Data Out Low on RD (pipelined)	4.09	3.41
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 3-3 • TRST and TCK Pull-Down Recommendations

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Do Not Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

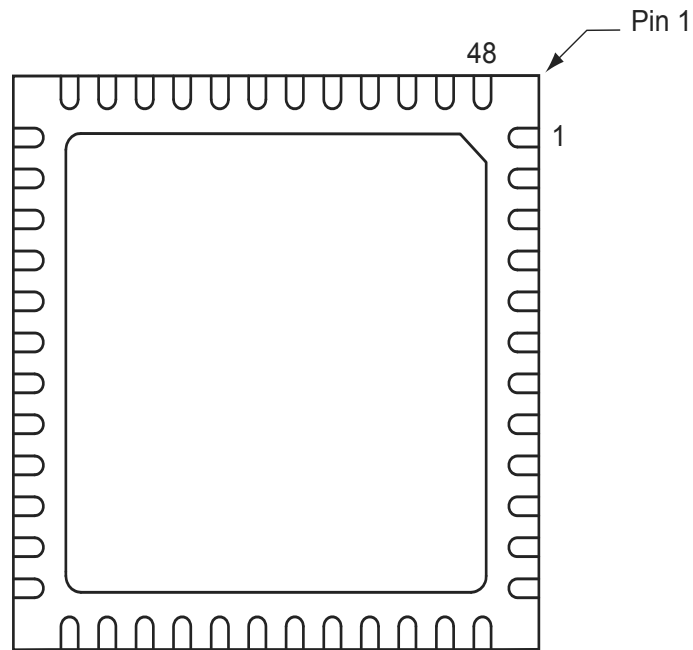
CS81	
Pin Number	AGLN250Z Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO12RSB0
A7	GBB0/IO16RSB0
A8	GBA1/IO19RSB0
A9	GBA2/IO20RSB1
B1	GAA2/IO67RSB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO06RSB0
B5	IO10RSB0
B6	GBC0/IO14RSB0
B7	GBB1/IO17RSB0
B8	IO21RSB1
B9	GBB2/IO22RSB1
C1	GAB2/IO65RSB3
C2	IO66RSB3
C3	GND
C4	IO08RSB0
C5	IO11RSB0
C6	GND
C7	GBA0/IO18RSB0
C8	GBC2/IO23RSB1
C9	IO24RSB1
D1	GAC2/IO63RSB3
D2	IO64RSB3
D3	GFA2/IO56RSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO30RSB1
D8	GCC1/IO25RSB1
D9	GCC0/IO26RSB1

CS81	
Pin Number	AGLN250Z Function
E1	GFB0/IO59RSB3
E2	GFB1/IO60RSB3
E3	GFA1/IO58RSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1
E7	GCA0/IO28RSB1
E8	GCA1/IO27RSB1
E9	GCB2/IO29RSB1
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO33RSB1
F8	GDC1/IO31RSB1
F9	GDC0/IO32RSB1
G1	GEA0/IO51RSB3
G2	GEC1/IO54RSB3
G3	GEC0/IO53RSB3
G4	IO45RSB2
G5	IO42RSB2
G6	IO37RSB2
G7	GDB2/IO35RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO52RSB3
H2	FF/GEB2/IO49RSB2
H3	IO47RSB2
H4	IO44RSB2
H5	IO41RSB2
H6	IO39RSB2
H7	GDA2/IO34RSB2
H8	TDI
H9	TDO

CS81	
Pin Number	AGLN250Z Function
J1	GEA2/IO50RSB2
J2	GEC2/IO48RSB2
J3	IO46RSB2
J4	IO43RSB2
J5	IO40RSB2
J6	IO38RSB2
J7	TCK
J8	TMS
J9	VPUMP

Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250Z-CS81.

QN48



Notes:

1. *This is the bottom view of the package.*
 2. *The die attach paddle of the package is tied to ground (GND).*
-

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the IGLOO nano datasheet.

Revision	Changes	Page
Revision 19 (October 2015)	Modified the note to include device/package obsolescence information in "Features and Benefits" section (SAR 69724).	1-I
	Added a note under Security Feature "Y" in "IGLOO nano Ordering Information" section (SAR 70553).	1-IV
	Modified AGLN250 pin assignment table to match with I/O Attribute Editor tool from Libero in "CS81" Package (SAR 59049).	4-6
	Modified the nominal area to 25 for CS81 Package in Table 1 (SAR 71127).	1-II
	Modified the title of AGLN125Z pin assignment table for "CS81" Package (SAR 71127).	4-6
Revision 18 (November 2013)	Modified the "Device Marking" section and updated Figure 1 • Example of Device Marking for Small Form Factor Packages to reflect updates suggested per CN1004 published on 5/10/2010 (SAR 52036).	V
Revision 17 (May 2013)	Deleted details related to Ambient temperature from "Enhanced Commercial Temperature Range", "IGLOO nano Ordering Information", "Temperature Grade Offerings", and Table 2-2 • Recommended Operating Conditions ¹ to remove ambiguities arising due to the same, and modified Note 2 (SAR 47063).	I, IV, VI, and 2-2
Revision 16 (December 2012)	The "IGLOO nano Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43174).	IV
	The note in Table 2-100 • IGLOO nano CCC/PLL Specification and Table 2-101 • IGLOO nano CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42565).	2-70, 2-71
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 15 (September 2012)	The status of the AGLN125 device has been modified from 'Advance' to 'Production' in the "IGLOO nano Device Status" section (SAR 41416).	III
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40274).	NA
Revision 14 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
Revision 13 (June 2012)	Figure Figure 2-34 • FIFO Read and Figure 2-35 • FIFO Write have been added (SAR 34842).	2-82
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38319). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1



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