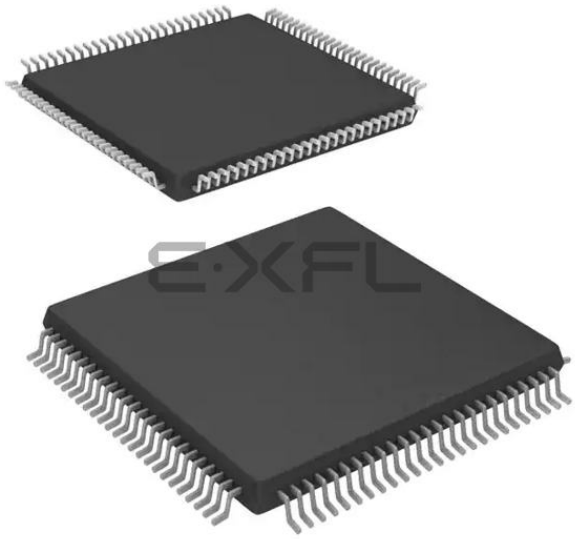


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

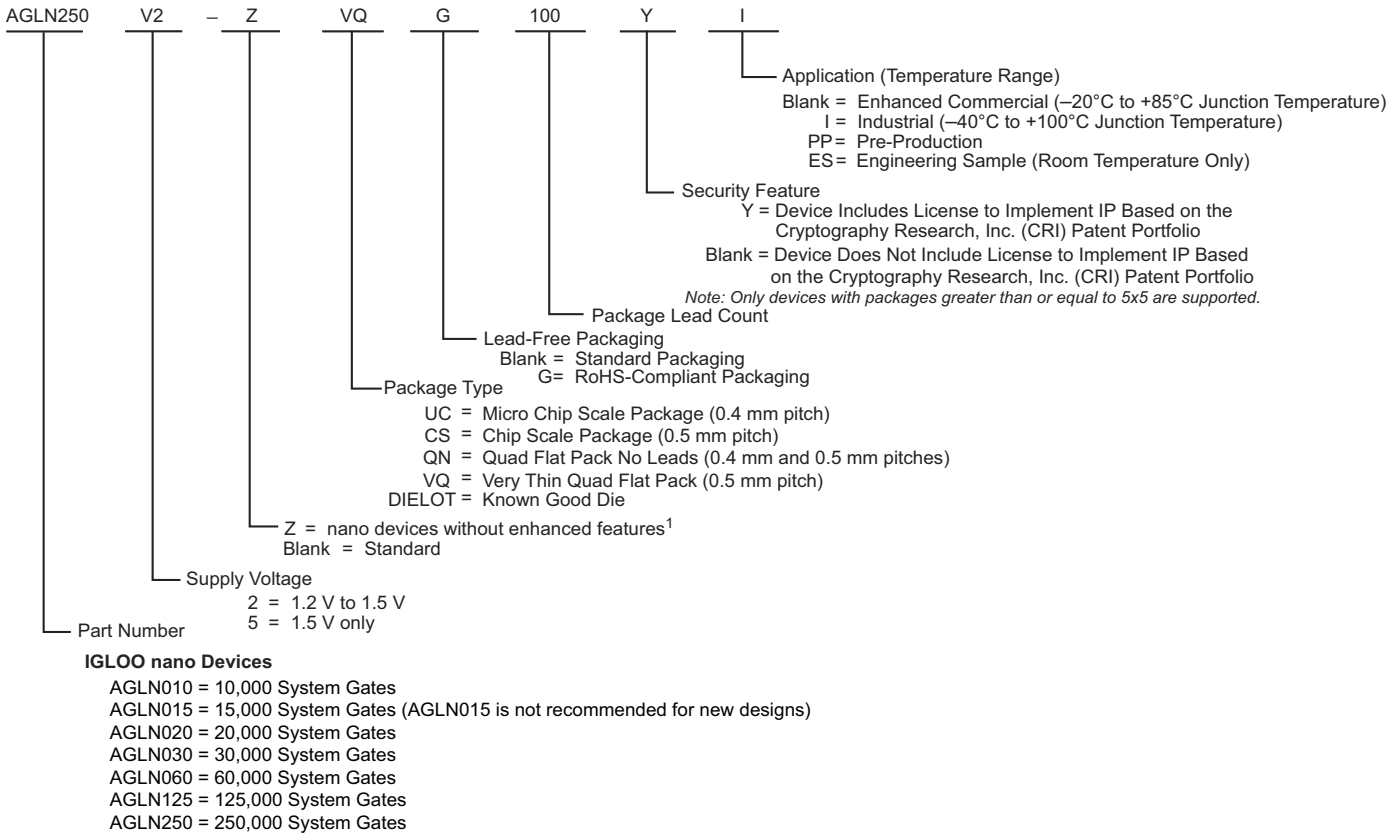
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	71
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln060v5-vq100i

IGLOO nano Ordering Information



IGLOO nano Devices

AGLN010 = 10,000 System Gates
AGLN015 = 15,000 System Gates (AGLN015 is not recommended for new designs)
AGLN020 = 20,000 System Gates
AGLN030 = 30,000 System Gates
AGLN060 = 60,000 System Gates
AGLN125 = 125,000 System Gates
AGLN250 = 250,000 System Gates

Notes:

1. *Z-feature grade devices AGLN060Z, AGLN125Z, and AGLN250Z do not support the enhanced nano features of Schmitt Trigger input, bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, hot-swap I/O capability and 1.2 V programming. The AGLN030 Z feature grade does not support Schmitt trigger input, bus hold and 1.2 V programming. For the VQ100, CS81, UC81, QN68, and QN48 packages, the Z feature grade and the N part number are not marked on the device. Z feature grade devices are not recommended for new designs.*
2. *AGLN030 is available in the Z feature grade only.*
3. *Marking Information: IGLOO nano V2 devices do not have a V2 marking, but IGLOO nano V5 devices are marked with a V5 designator.*

Devices Not Recommended For New Designs

AGLN015, AGLN030Z, AGLN060Z, AGLN125Z, and AGLN250Z are not recommended for new designs. For more information on obsoleted devices/packages, refer to the *PDN1503 - IGLOO nano Z and ProASIC3 nano Z Families*.

Device Marking

Microsemi normally topside marks the full ordering part number on each device. There are some exceptions to this, such as some of the Z feature grade nano devices, the V2 designator for IGLOO devices, and packages where space is physically limited. Packages that have limited characters available are UC36, UC81, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

Figure 1 shows an example of device marking based on the AGLN250V2-CSG81. The actual mark will vary by the device/package combination ordered.

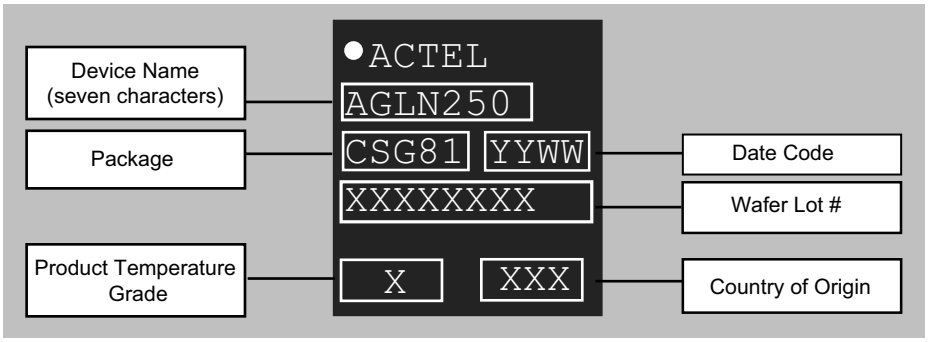


Figure 1 • **Example of Device Marking for Small Form Factor Packages**

IGLOO nano Products Available in the Z Feature Grade

IGLOO nano-Z Devices	AGLN030Z*	AGLN060Z*	AGLN125Z*	AGLN250Z*
	QN48	–	–	–
	QN68	–	–	–
	UC81	–	–	–
	CS81	CS81	CS81	CS81
Packages	VQ100	VQ100	VQ100	VQ100

*Note: *Not recommended for new designs.*

Temperature Grade Offerings

Package	AGLN010	AGLN015*	AGLN020	AGLN030Z*	AGLN060 AGLN060Z*	AGLN125 AGLN125Z*	AGLN250 AGLN250Z*
UC36	C, I	–	–	–	–	–	–
QN48	C, I	–	–	C, I	–	–	–
QN68	–	C, I	C, I	C, I	–	–	–
UC81	–	–	C, I	C, I	–	–	–
CS81	–	–	C, I	C, I	C, I	C, I	C, I
VQ100	–	–	–	C, I	C, I	C, I	C, I

*Note: * Not recommended for new designs.*

C = Enhanced Commercial temperature range: –20°C to +85°C junction temperature
I = Industrial temperature range: –40°C to +100°C junction temperature

Contact your local Microsemi representative for device availability: http://www.microsemi.com/soc/contact/default.aspx.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO nano devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic.

Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO nano device architecture mitigates the need for ASIC migration at higher user volumes. This makes IGLOO nano devices cost-effective ASIC replacement solutions, especially for applications in the consumer, networking/communications, computing, and avionics markets.

With a variety of devices under $1, IGLOO nano FPGAs enable cost-effective implementation of programmable logic and quick time to market.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO nano flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO nano FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO nano device offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO nano FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO nano architecture provides granularity comparable to standard-cell ASICs. The IGLOO nano device consists of five distinct and programmable architectural features (Figure 1-3 on page 1-5 to Figure 1-4 on page 1-5):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO nano core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

† The AGLN030 and smaller devices do not support PLL or SRAM.

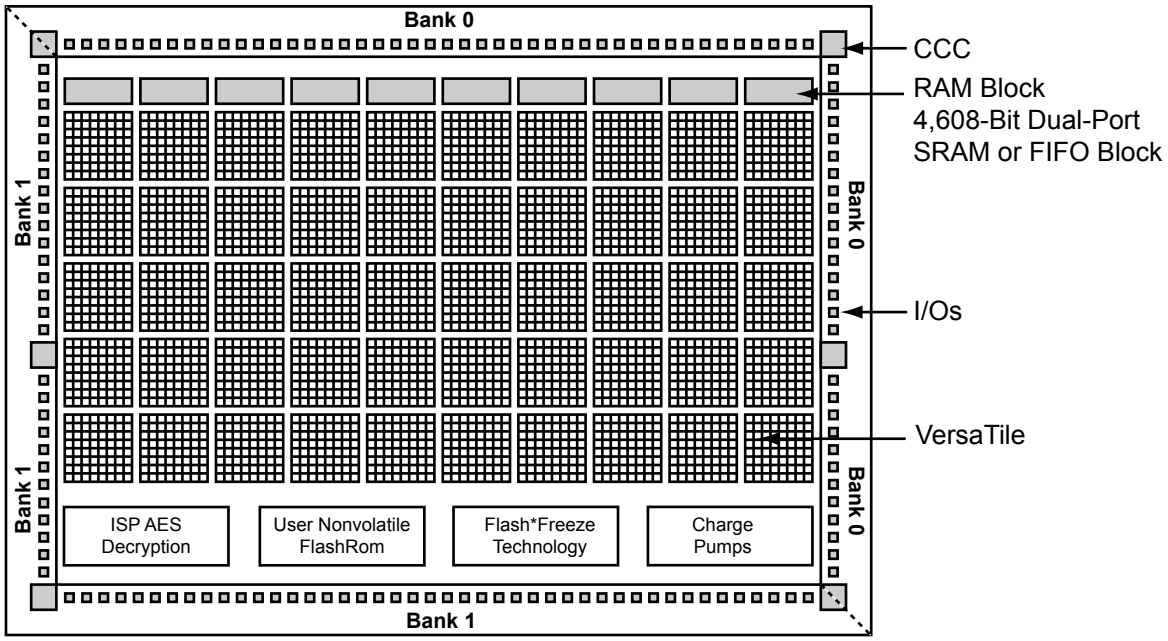


Figure 1-3 • **IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125)**

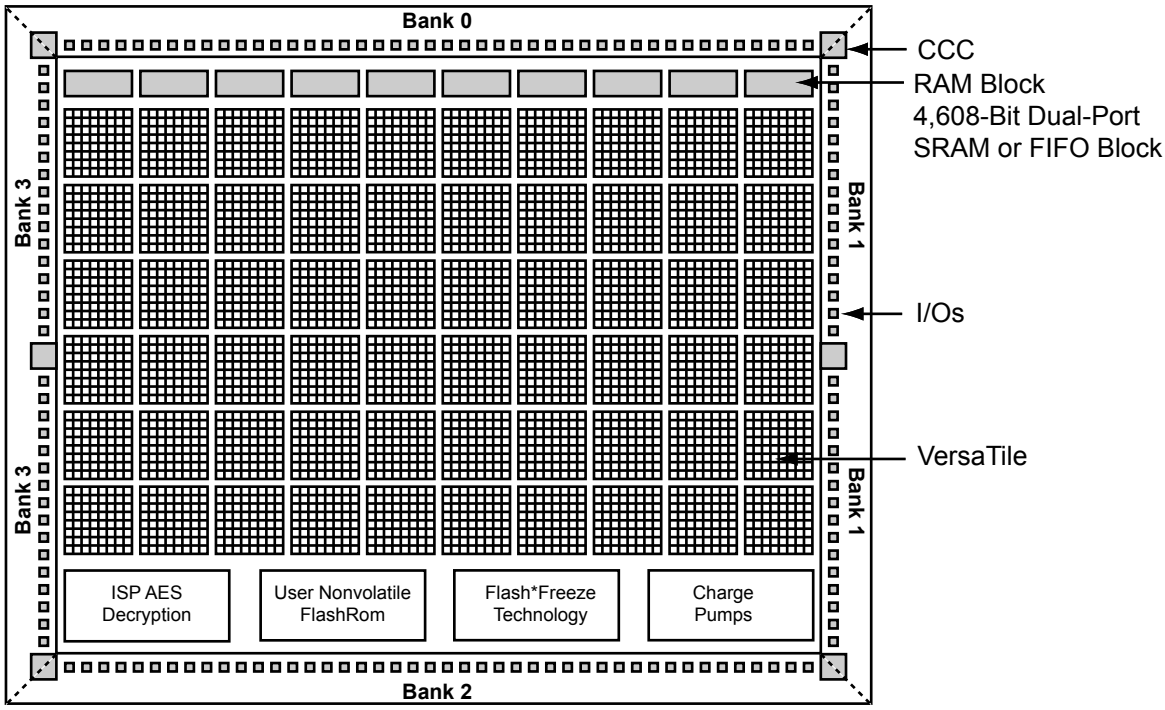


Figure 1-4 • **IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)**

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

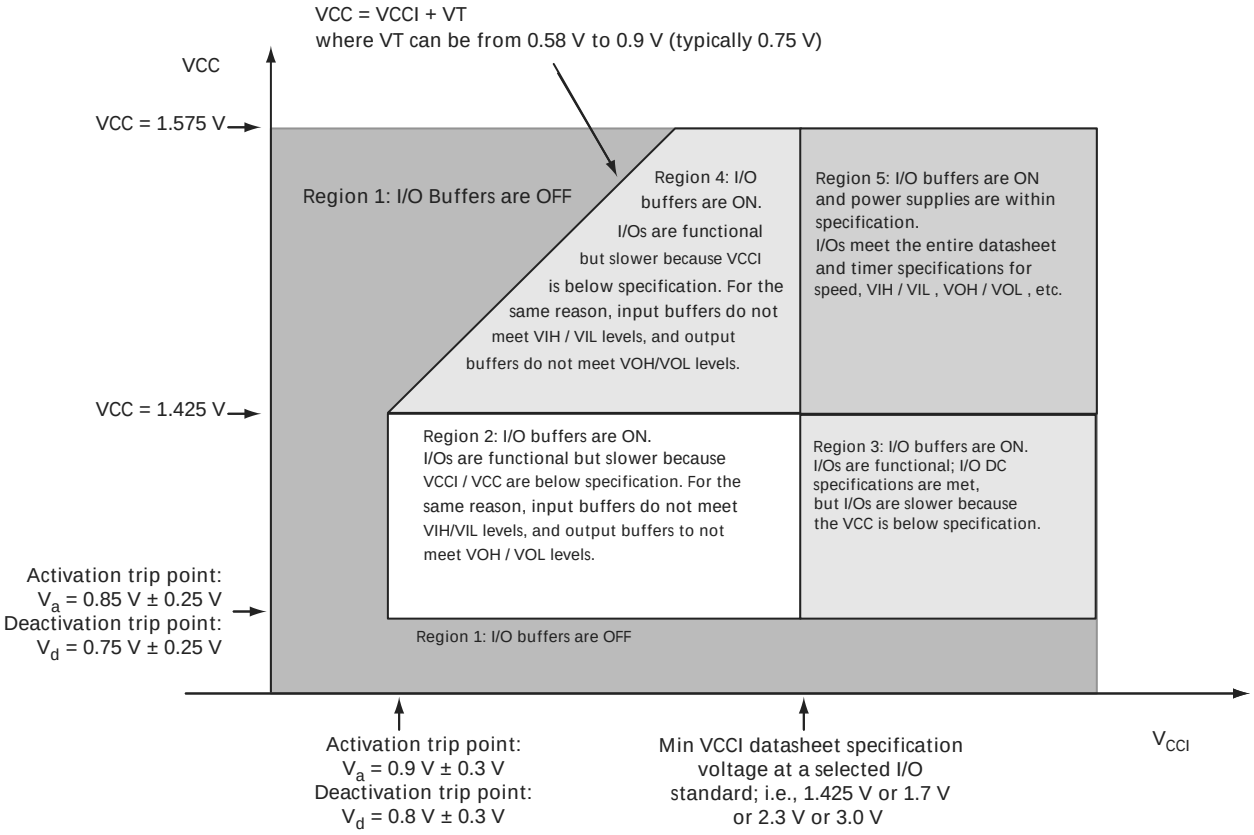


Figure 2-1 • **V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

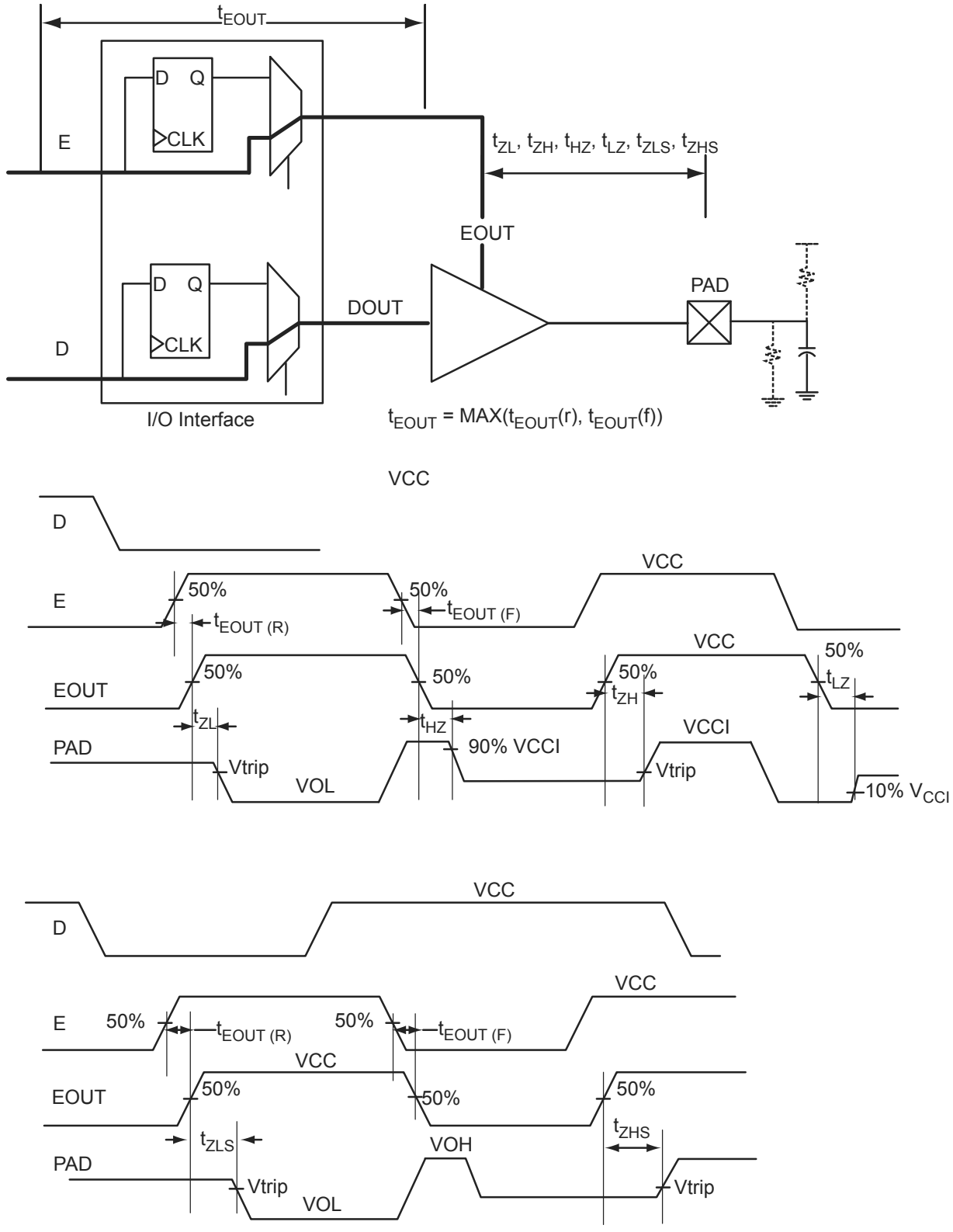


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Detailed I/O DC Characteristics

Table 2-27 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-28 • **I/O Output Buffer Maximum Resistances [1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS [4]	1 mA	315	315
1.2 V LVCMOS Wide Range [4]	100 µA	315	315

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models posted at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)}$ *= (VOLspec) / IOLspec*
3. $R_{(PULL\text{-}UP\text{-}MAX)}$ *= (VCCImax – VOHspec) /* I_{OHspec}
4. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*

Applies to 1.2 V DC Core Voltage

Table 2-38 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
4 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
6 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns
8 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-39 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
4 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
6 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
8 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

I/O Register Specifications

Fully Registered I/O Buffers with Asynchronous Preset

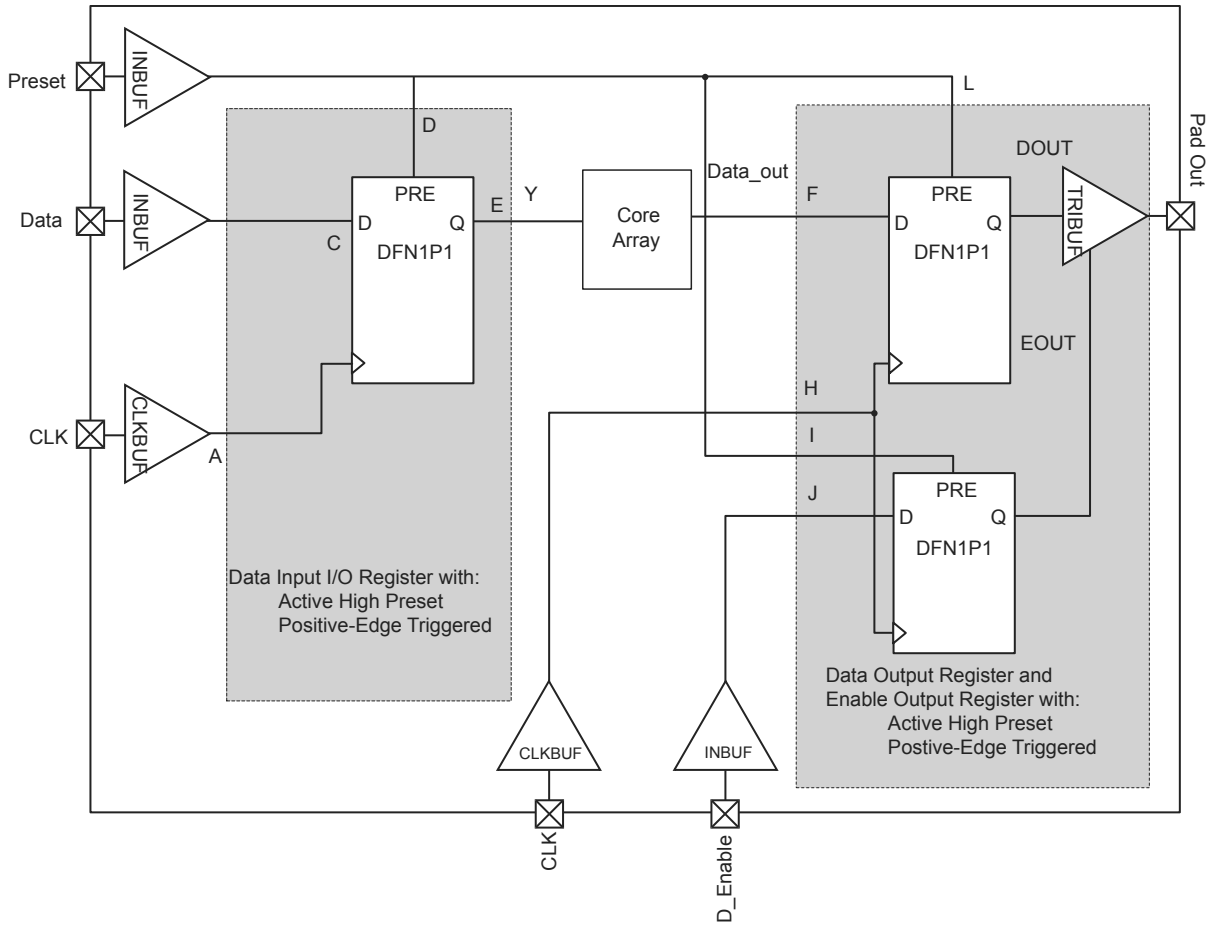


Figure 2-12 • **Timing Model of Registered I/O Buffers with Asynchronous Preset**

Fully Registered I/O Buffers with Asynchronous Clear

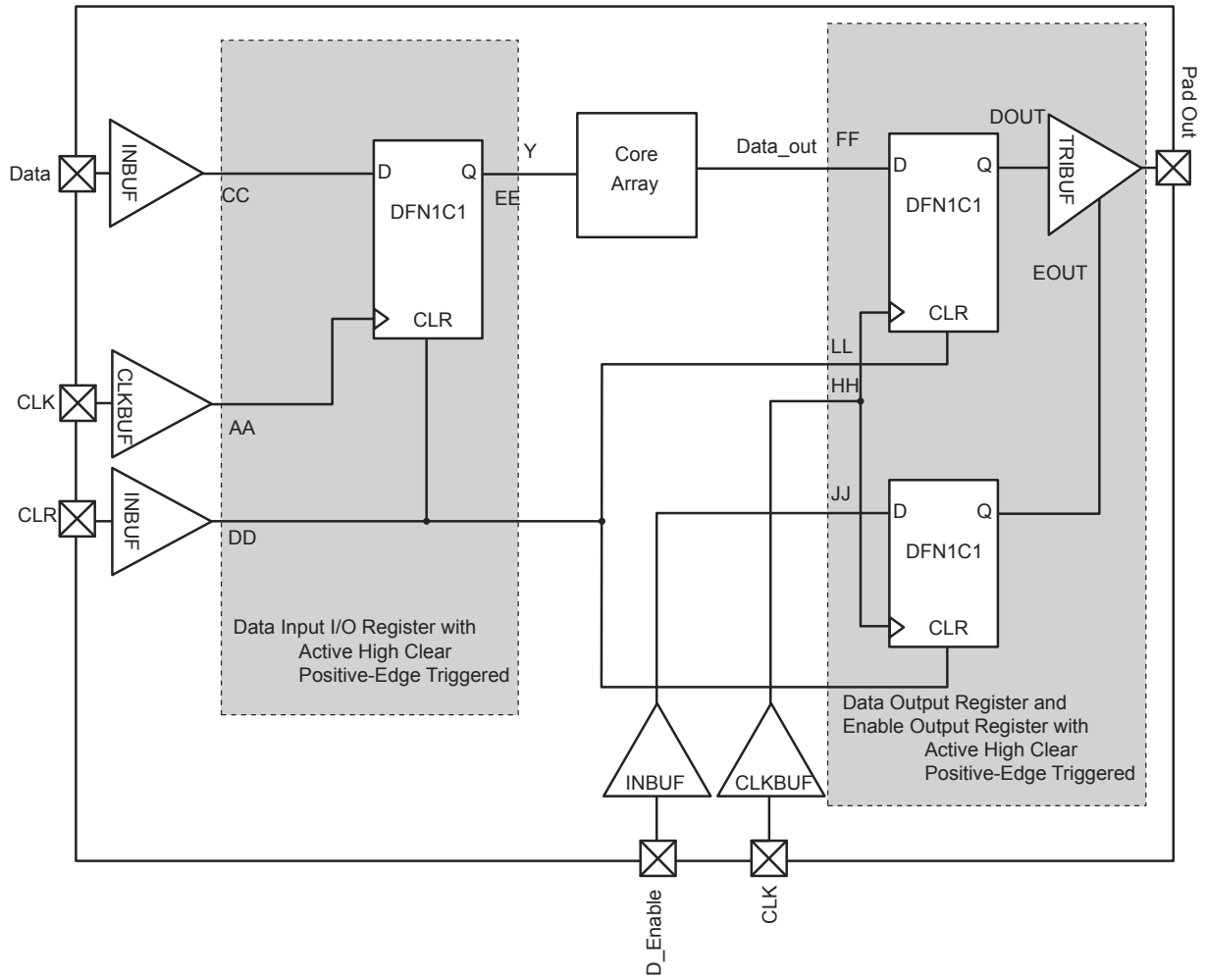


Figure 2-13 • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

Global Resource Characteristics

AGLN125 Clock Tree Topology

Clock delays are device-specific. Figure 2-25 is an example of a global tree used for clock routing. The global tree presented in Figure 2-25 is driven by a CCC located on the west side of the AGLN125 device. It is used to drive all D-flip-flops in the device.

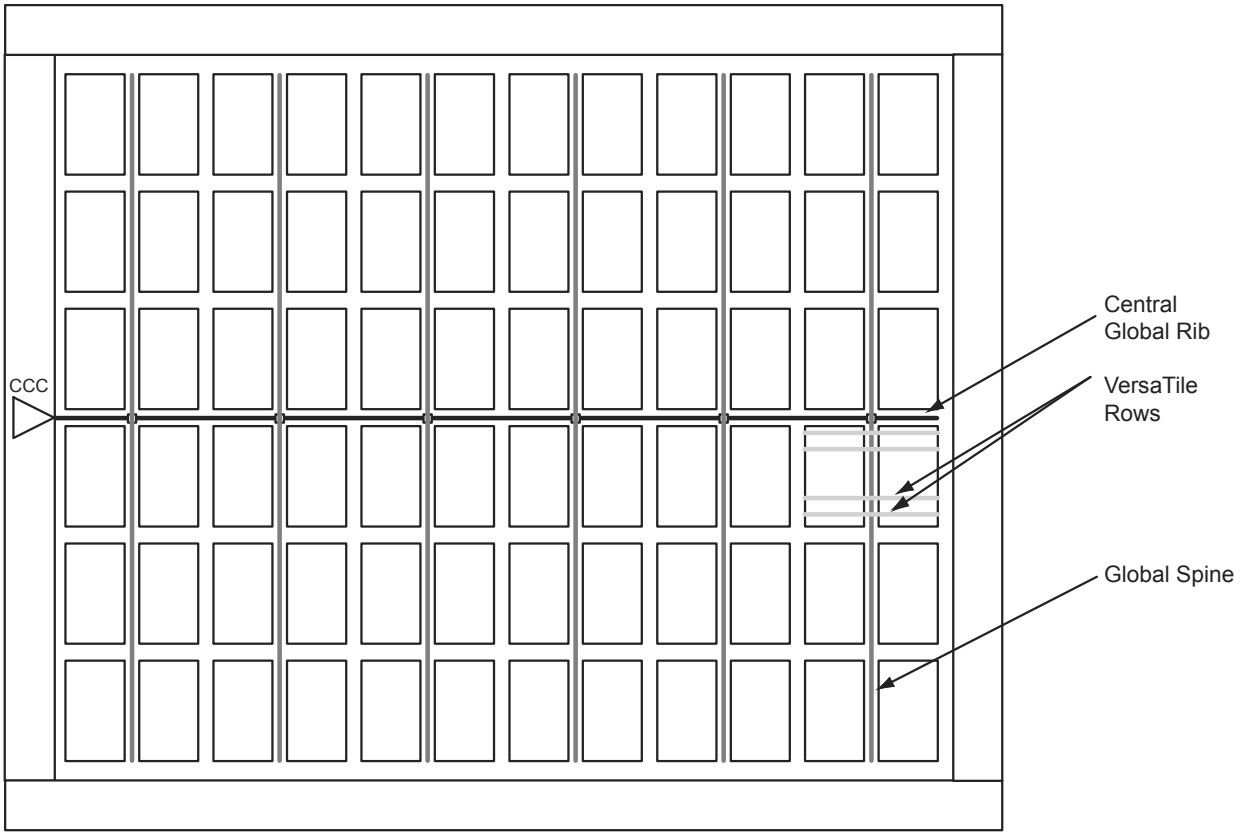


Figure 2-25 • **Example of Global Tree Use in an AGLN125 Device for Clock Routing**

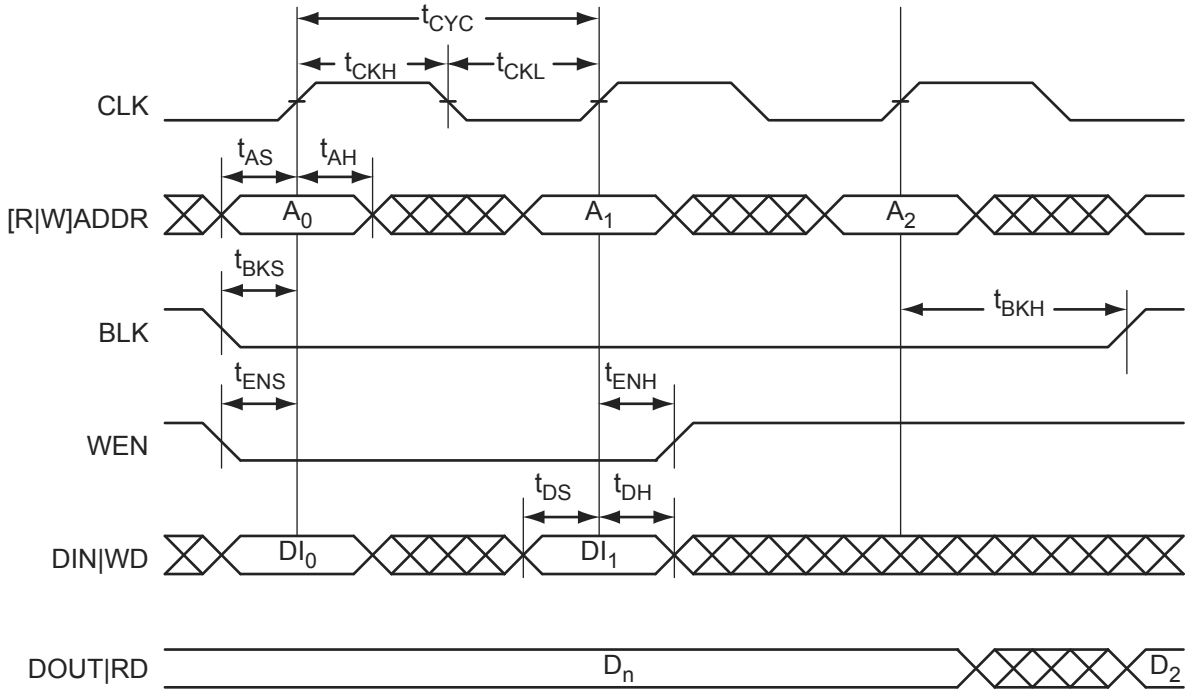


Figure 2-30 • **RAM Write, Output Retained (WMODE = 0). Applicable to Both RAM4K9 and RAM512x18.**

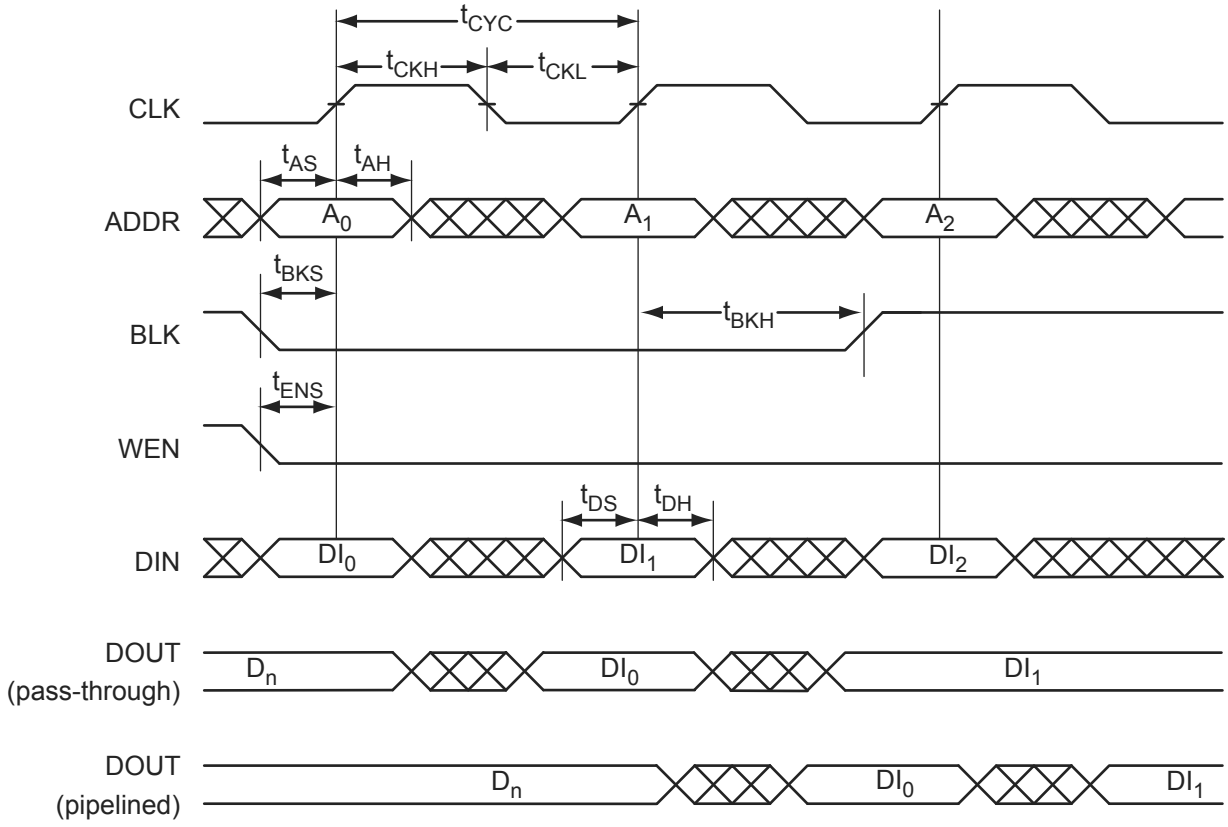


Figure 2-31 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-102 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.68	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{BKS}	BLK setup time	1.37	ns
t_{BKH}	BLK hold time	0.13	ns
t_{DS}	Input data (DIN) setup time	0.59	ns
t_{DH}	Input data (DIN) hold time	0.30	ns
t_{CKQ1}	Clock HIGH to new data valid on DOUT (output retained, WMODE = 0)	2.94	ns
	Clock HIGH to new data valid on DOUT (flow-through, WMODE = 1)	2.55	ns
t_{CKQ2}	Clock HIGH to new data valid on DOUT (pipelined)	1.51	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.23	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.41	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.72	ns
	RESET Low to data out Low on DOUT (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	ns
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-103* • RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.61	ns
t_{ENH}	REN, WEN hold time	0.07	ns
t_{DS}	Input data (WD) setup time	0.59	ns
t_{DH}	Input data (WD) hold time	0.30	ns
t_{CKQ1}	Clock HIGH to new data valid on RD (output retained)	3.51	ns
t_{CKQ2}	Clock HIGH to new data valid on RD (pipelined)	1.43	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	1.72	ns
	RESET Low to data out Low on RD (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	0.51
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-110 • JTAG 1532
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-111 • JTAG 1532
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

CS81	
Pin Number	**AGLN020 Function**
A1	IO64RSB2
A2	IO54RSB2
A3	IO57RSB2
A4	IO36RSB1
A5	IO32RSB1
A6	IO24RSB1
A7	IO20RSB1
A8	IO04RSB0
A9	IO08RSB0
B1	IO59RSB2
B2	IO55RSB2
B3	IO62RSB2
B4	IO34RSB1
B5	IO28RSB1
B6	IO22RSB1
B7	IO18RSB1
B8	IO00RSB0
B9	IO03RSB0
C1	IO51RSB2
C2	IO50RSB2
C3	NC
C4	NC
C5	NC
C6	NC
C7	NC
C8	IO10RSB0
C9	IO07RSB0
D1	IO49RSB2
D2	IO44RSB2
D3	NC
D4	VCC
D5	VCCIB2
D6	GND
D7	NC
D8	IO13RSB0
D9	IO12RSB0

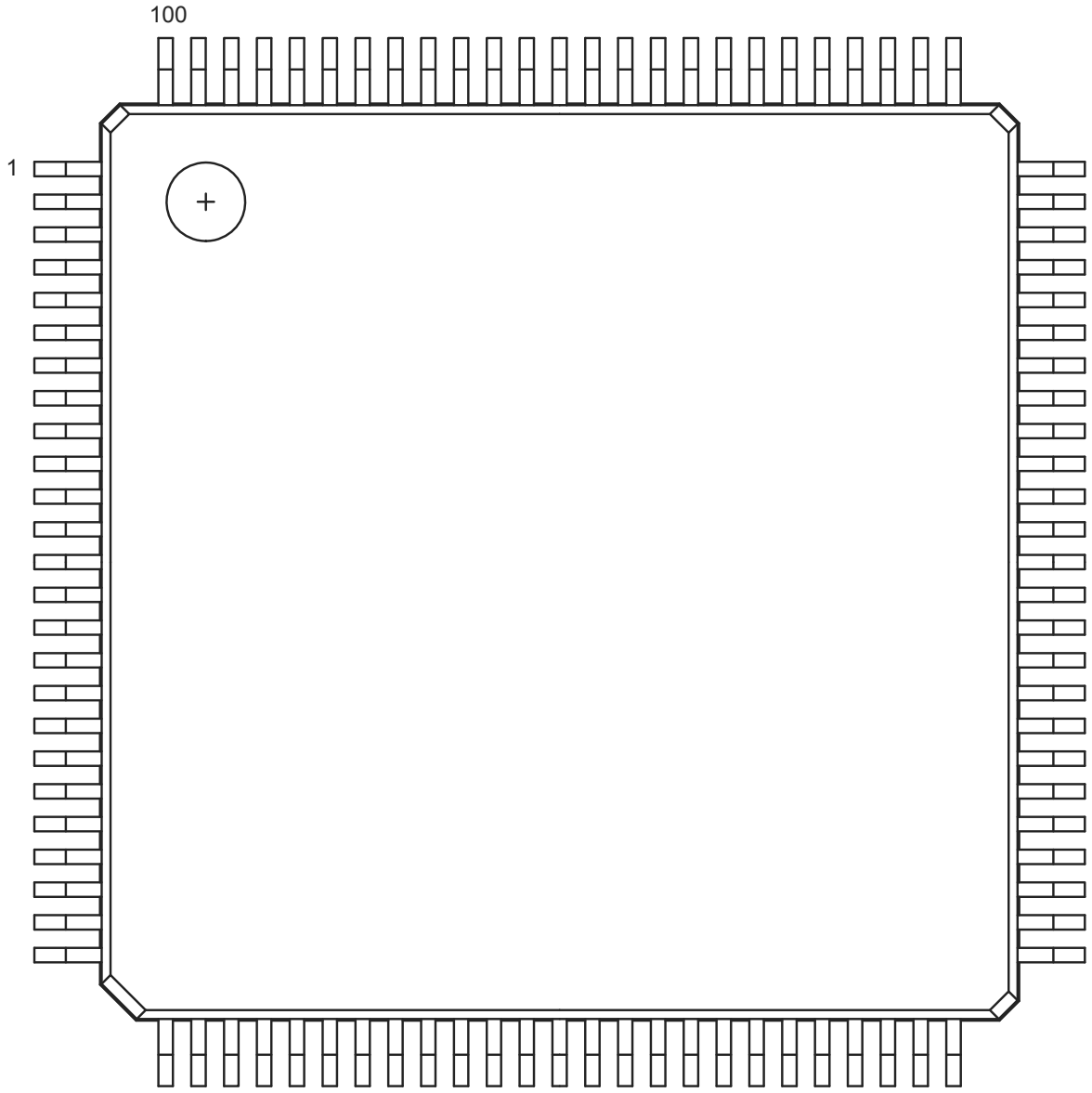
CS81	
Pin Number	**AGLN020 Function**
E1	GEC0/IO48RSB2
E2	GEA0/IO47RSB2
E3	NC
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	NC
E8	GDA0/IO15RSB0
E9	GDC0/IO14RSB0
F1	IO46RSB2
F2	IO45RSB2
F3	NC
F4	GND
F5	VCCIB1
F6	NC
F7	NC
F8	IO16RSB0
F9	IO17RSB0
G1	IO43RSB2
G2	IO42RSB2
G3	IO41RSB2
G4	IO31RSB1
G5	NC
G6	IO21RSB1
G7	NC
G8	VJTAG
G9	TRST
H1	IO40RSB2
H2	FF/IO39RSB1
H3	IO35RSB1
H4	IO29RSB1
H5	IO26RSB1
H6	IO25RSB1
H7	IO19RSB1
H8	TDI
H9	TDO

CS81	
Pin Number	**AGLN020 Function**
J1	IO38RSB1
J2	IO37RSB1
J3	IO33RSB1
J4	IO30RSB1
J5	IO27RSB1
J6	IO23RSB1
J7	TCK
J8	TMS
J9	VPUMP

QN68	
Pin Number	**AGLN015 Function**
1	IO60RSB2
2	IO54RSB2
3	IO52RSB2
4	IO50RSB2
5	IO49RSB2
6	GEC0/IO48RSB2
7	GEA0/IO47RSB2
8	VCC
9	GND
10	VCCIB2
11	IO46RSB2
12	IO45RSB2
13	IO44RSB2
14	IO43RSB2
15	IO42RSB2
16	IO41RSB2
17	IO40RSB2
18	FF/IO39RSB1
19	IO37RSB1
20	IO35RSB1
21	IO33RSB1
22	IO31RSB1
23	IO30RSB1
24	VCC
25	GND
26	VCCIB1
27	IO27RSB1
28	IO25RSB1
29	IO23RSB1
30	IO21RSB1
31	IO19RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP

QN68	
Pin Number	**AGLN015 Function**
36	TDO
37	TRST
38	VJTAG
39	IO17RSB0
40	IO16RSB0
41	GDA0/IO15RSB0
42	GDC0/IO14RSB0
43	IO13RSB0
44	VCCIB0
45	GND
46	VCC
47	IO12RSB0
48	IO11RSB0
49	IO09RSB0
50	IO05RSB0
51	IO00RSB0
52	IO07RSB0
53	IO03RSB0
54	IO18RSB1
55	IO20RSB1
56	IO22RSB1
57	IO24RSB1
58	IO28RSB1
59	NC
60	GND
61	NC
62	IO32RSB1
63	IO34RSB1
64	IO36RSB1
65	IO61RSB2
66	IO58RSB2
67	IO56RSB2
68	IO63RSB2

VQ100



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ100	
Pin Number	**AGLN060Z Function**
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1

VQ100	
Pin Number	**AGLN060Z Function**
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45*	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC

VQ100	
Pin Number	**AGLN060Z Function**
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

*Note: *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin 45 in AGLN060Z-VQ100.*