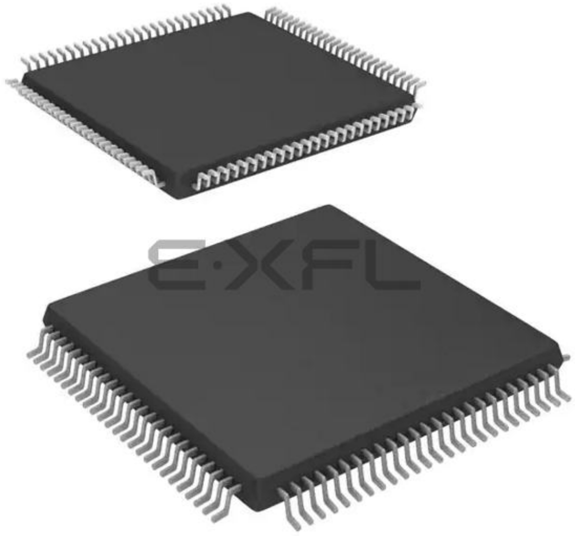
# Microchip Technology - AGLN060V5-VQG100 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 1536 |
| Total RAM Bits | 18432 |
| Number of I/O | 71 |
| Number of Gates | 60000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -20°C ~ 85°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agln060v5-vqg100 |

# IGLOO nano Products Available in the Z Feature Grade

| IGLOO nano-Z Devices | AGLN030Z* | AGLN060Z* | AGLN125Z* | AGLN250Z* |
|---|---|---|---|---|
| **Packages** | QN48 | – | – | – |
| | QN68 | – | – | – |
| | UC81 | – | – | – |
| | CS81 | CS81 | CS81 | CS81 |
| | VQ100 | VQ100 | VQ100 | VQ100 |

*Note: *Not recommended for new designs.*

# Temperature Grade Offerings

| | AGLN010 | AGLN015* | AGLN020 | | AGLN060 | AGLN125 | AGLN250 |
|---|---|---|---|---|---|---|---|
| **Package** | | | | AGLN030Z* | AGLN060Z* | AGLN125Z* | AGLN250Z* |
| UC36 | C, I | – | – | – | – | – | – |
| QN48 | C, I | – | – | C, I | – | – | – |
| QN68 | – | C, I | C, I | C, I | – | – | – |
| UC81 | – | – | C, I | C, I | – | – | – |
| CS81 | – | – | C, I | C, I | C, I | C, I | C, I |
| VQ100 | – | – | – | C, I | C, I | C, I | C, I |

*Note: * Not recommended for new designs.*

*C = Enhanced Commercial temperature range: –20°C to +85°C junction temperature*
*I = Industrial temperature range: –40°C to +100°C junction temperature*

Contact your local Microsemi representative for device availability: http://www.microsemi.com/soc/contact/default.aspx.

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## IGLOO nano Device Overview

## IGLOO nano DC and Switching Characteristics

## Pin Descriptions

## Package Pin Assignments

## Datasheet Information

## Flash Advantages

### Low Power

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

### Security

Nonvolatile, flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO nano devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO nano device provides the best available security for programmable logic designs.

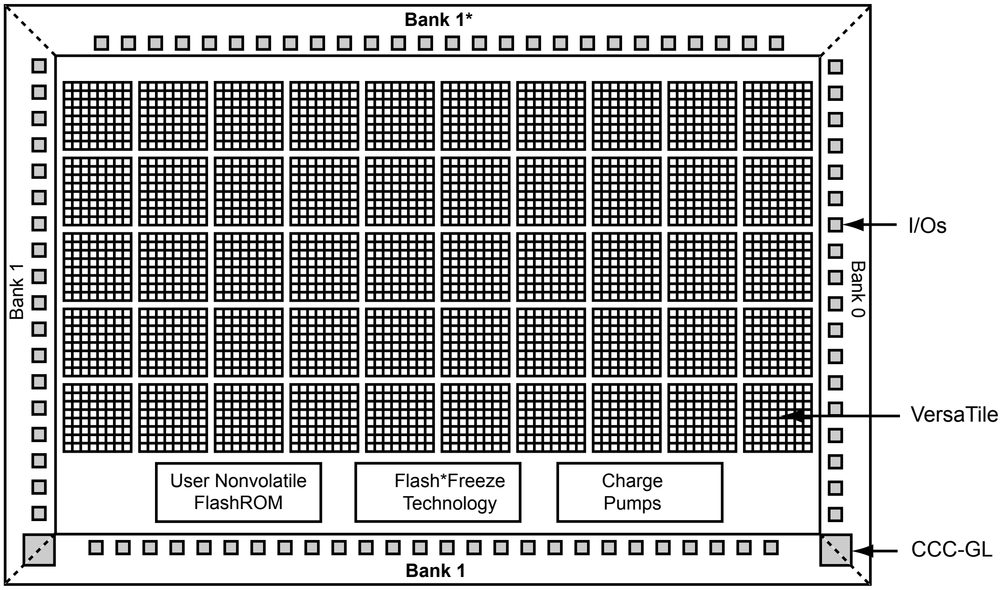
### Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### Instant On

Microsemi flash-based IGLOO nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano flash FPGAs enable the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.



*Note: *Bank 0 for the AGLN030 device*

***Figure 1-1 •*** **IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030)**

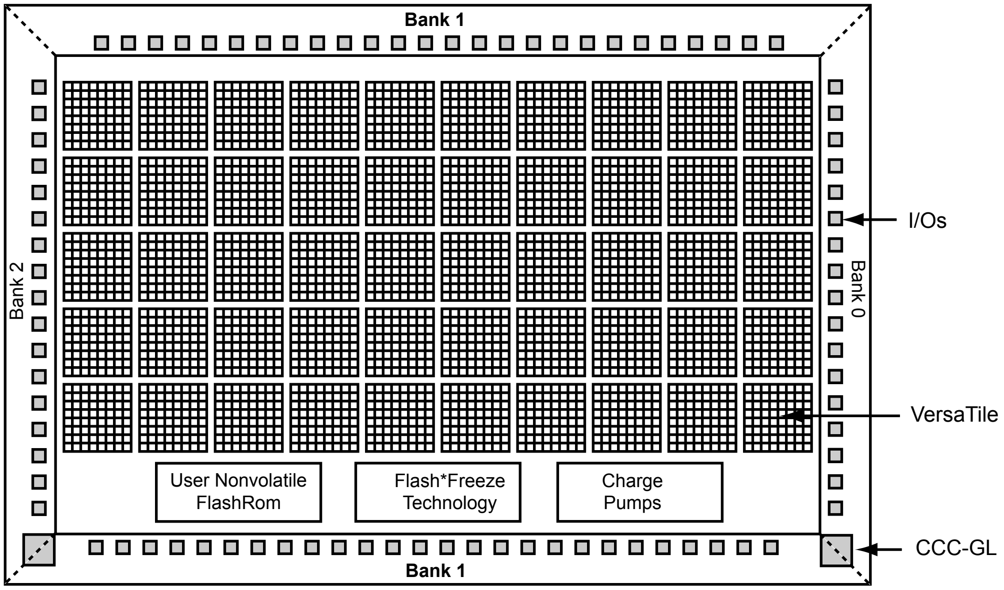


***Figure 1-2 •*** **IGLOO Device Architecture Overview with Three I/O Banks and No RAM (AGLN015 and AGLN020)**

The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz up to 250 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / $f_{OUT\_CCC}$ (for PLL only)

### *Global Clocking*

IGLOO nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

## *I/Os with Advanced I/O Standards*

IGLOO nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.2 V, 1.2 V wide range, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V).

The I/Os are organized into banks with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the AGLN060, AGLN125, and AGLN250 devices.

IGLOO nano devices support LVTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

# Wide Range I/O Support

IGLOO nano devices support JEDEC-defined wide range I/O operation. IGLOO nano devices support both the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

**Table 2-2 • Recommended Operating Conditions** [1]

| Symbol | Parameter | | Extended Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | | –20 to + 85[2] | –40 to +100[2] | °C |
| VCC | 1.5 V DC core supply voltage[3] | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.2 V–1.5 V wide range core voltage[4,5] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP [6] | Programming voltage | Programming mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL[7] | Analog power supply (PLL) | 1.5 V DC core supply voltage[3] | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | | 1.2 V–1.5 V wide range core supply voltage[4] | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VCCI and VMV [8,9] | 1.2 V DC supply voltage [4] | | 1.14 to 1.26 | 1.14 to 1.26 | V |
| | 1.2 V DC wide range supply voltage [4] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | 3.3 V DC wide range supply voltage [10] | | 2.7 to 3.6 | 2.7 to 3.6 | V |

*Notes:*

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.*
3. *For IGLOO® nano V5 devices*
4. *For IGLOO nano V2 devices only, operating at VCCI ≥ VCC*
5. *IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.*
6. *$V_{PUMP}$ can be left floating during operation (not programming mode).*
7. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.*
8. *VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.*
9. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

**Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature**[1]

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) [2] | Maximum Operating Junction Temperature $T_J$ (°C) [2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

*Notes:*

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

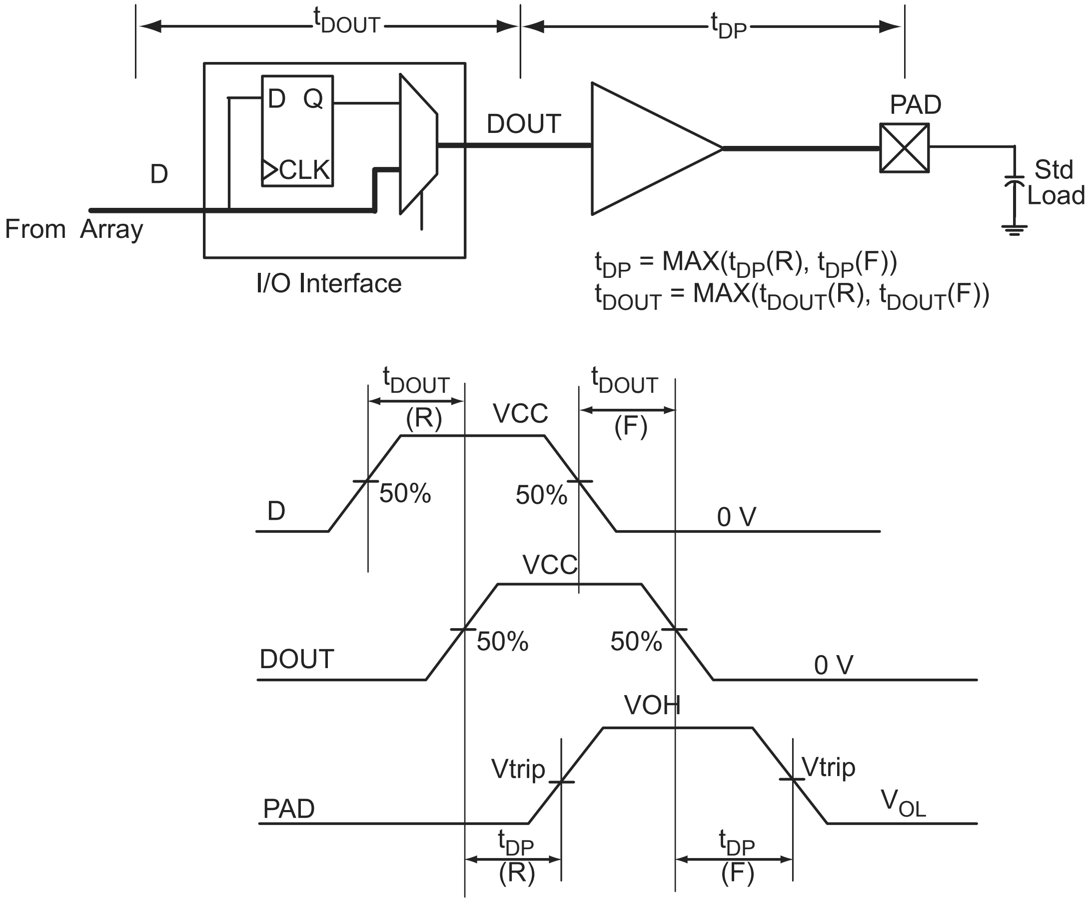


***Figure 2-5 •*** **Output Buffer Model and Delays (example)**

### *Applies to IGLOO nano at 1.2 V Core Operating Conditions*

***Table 2-26 •*** **Summary of I/O Timing Characteristics—Software Default Settings**
**STD Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V,**
**Worst-Case VCCI = 3.0 V**

| I/O Standard | Drive Strength (mA) | Equiv. Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY)}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 8 mA | 8 mA | High | 5 pF | 1.55 | 2.31 | 0.26 | 0.97 | 1.36 | 1.10 | 2.34 | 1.90 | 2.43 | 3.14 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 8 mA | High | 5 pF | 1.55 | 3.25 | 0.26 | 1.31 | 1.91 | 1.10 | 3.25 | 2.61 | 3.38 | 4.27 | ns |
| 2.5 V LVCMOS | 8 mA | 8 mA | High | 5 pF | 1.55 | 2.30 | 0.26 | 1.21 | 1.39 | 1.10 | 2.33 | 2.04 | 2.41 | 2.99 | ns |
| 1.8 V LVCMOS | 4 mA | 4 mA | High | 5 pF | 1.55 | 2.49 | 0.26 | 1.13 | 1.59 | 1.10 | 2.53 | 2.34 | 2.42 | 2.81 | ns |
| 1.5 V LVCMOS | 2 mA | 2 mA | High | 5 pF | 1.55 | 2.78 | 0.26 | 1.27 | 1.77 | 1.10 | 2.82 | 2.62 | 2.44 | 2.74 | ns |
| 1.2 V LVCMOS | 1 mA | 1 mA | High | 5 pF | 1.55 | 3.50 | 0.26 | 1.56 | 2.27 | 1.10 | 3.37 | 3.10 | 2.55 | 2.66 | ns |
| 1.2 V LVCMOS Wide Range[3] | 100 µA | 1 mA | High | 5 pF | 1.55 | 3.50 | 0.26 | 1.56 | 2.27 | 1.10 | 3.37 | 3.10 | 2.55 | 2.66 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V side range as specified in the JESD8-12 specification.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

***Table 2-51*** **• Minimum and Maximum DC Input and Output Levels**

| **1.8 V LVCMOS** | **VIL** | | **VIH** | | **VOL** | **VOH** | **IOL** | **IOH** | **IOSL** | **IOSH** | **IIL [1]** | **$I_I$H [2]** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min. V** | **Max. V** | **Min. V** | **Max. V** | **Max. V** | **Min. V** | **mA** | **mA** | **Max. mA[3]** | **Max. mA[3]** | **μA[4]** | **μA[4]** |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 2 | 2 | 9 | 11 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 4 | 4 | 17 | 22 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

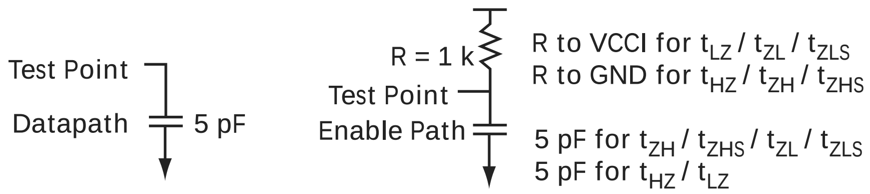


***Figure 2-9*** **• AC Loading**

***Table 2-52*** **• 1.8 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| **Input LOW (V)** | **Input HIGH (V)** | **Measuring Point* (V)** | **$C_{LOAD}$ (pF)** |
|---|---|---|---|
| 0 | 1.8 | 0.9 | 5 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

## 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

***Table 2-63 •*** **Minimum and Maximum DC Input and Output Levels**

| 1.2 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL [1] | IIH [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min. V** | **Max. V** | **Min. V** | **Max. V** | **Max. V** | **Min. V** | **mA** | **mA** | **Max. mA[3]** | **Max. mA[3]** | **μA[4]** | **μA[4]** |
| 1 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 1 | 1 | 10 | 13 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

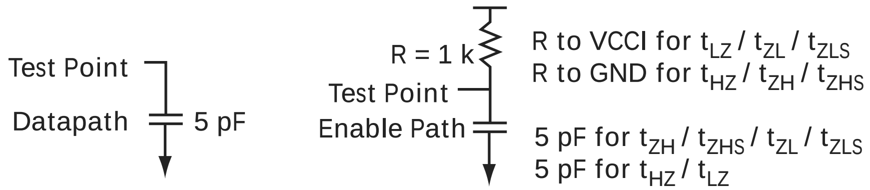


***Figure 2-11 •*** **AC Loading**

***Table 2-64 •*** **1.2 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.2 | 0.6 | 5 |

Note: _*Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points._

### Timing Characteristics

#### Applies to 1.2 V DC Core Voltage

***Table 2-65 •*** **1.2 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | STD | 1.55 | 8.30 | 0.26 | 1.56 | 2.27 | 1.10 | 7.97 | 7.54 | 2.56 | 2.55 | ns |

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-66 •*** **1.2 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | STD | 1.55 | 3.50 | 0.26 | 1.56 | 2.27 | 1.10 | 3.37 | 3.10 | 2.55 | 2.66 | ns |

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Fully Registered I/O Buffers with Asynchronous Clear

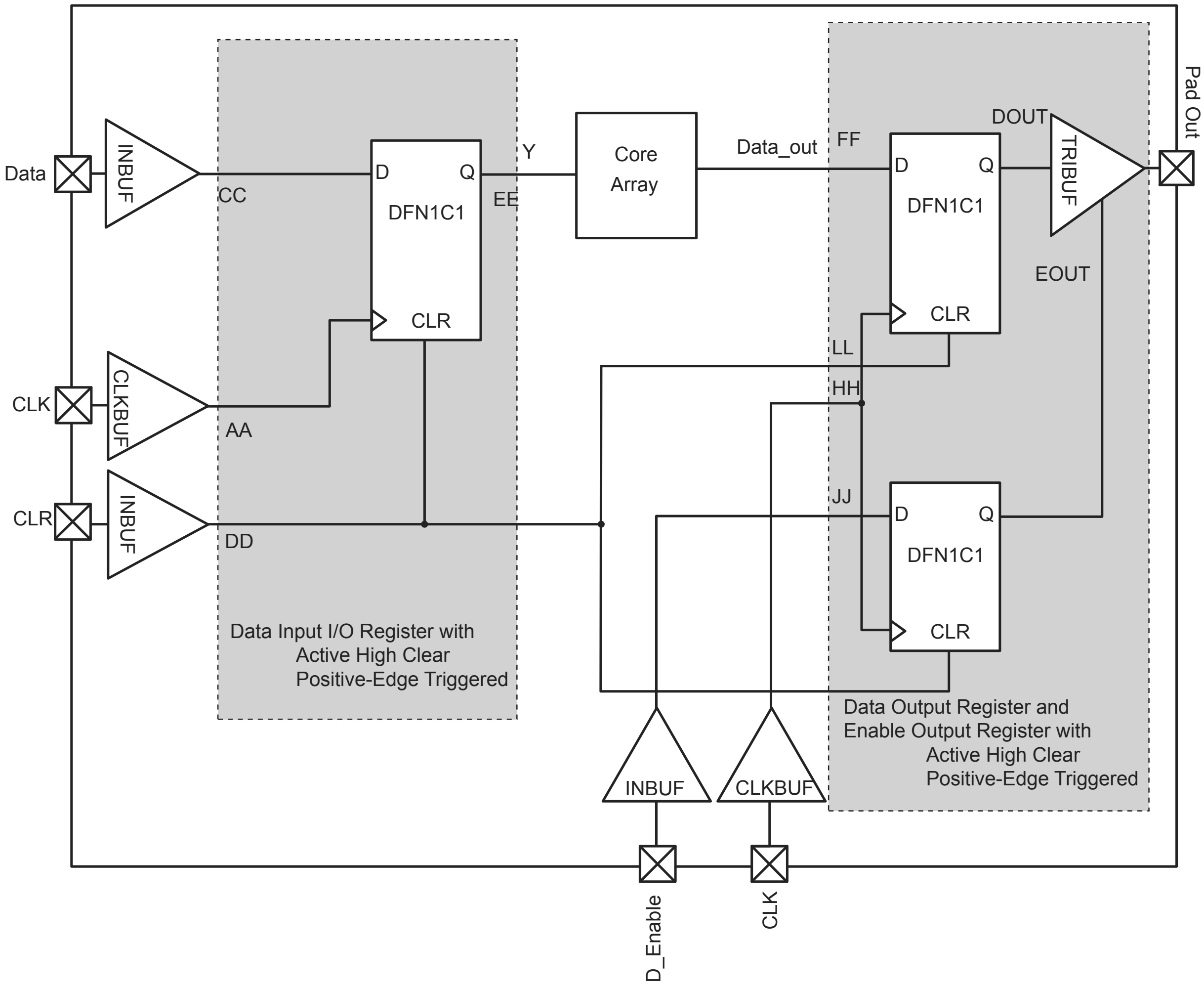


***Figure 2-13* • Timing Model of the Registered I/O Buffers with Asynchronous Clear**

## Input Register

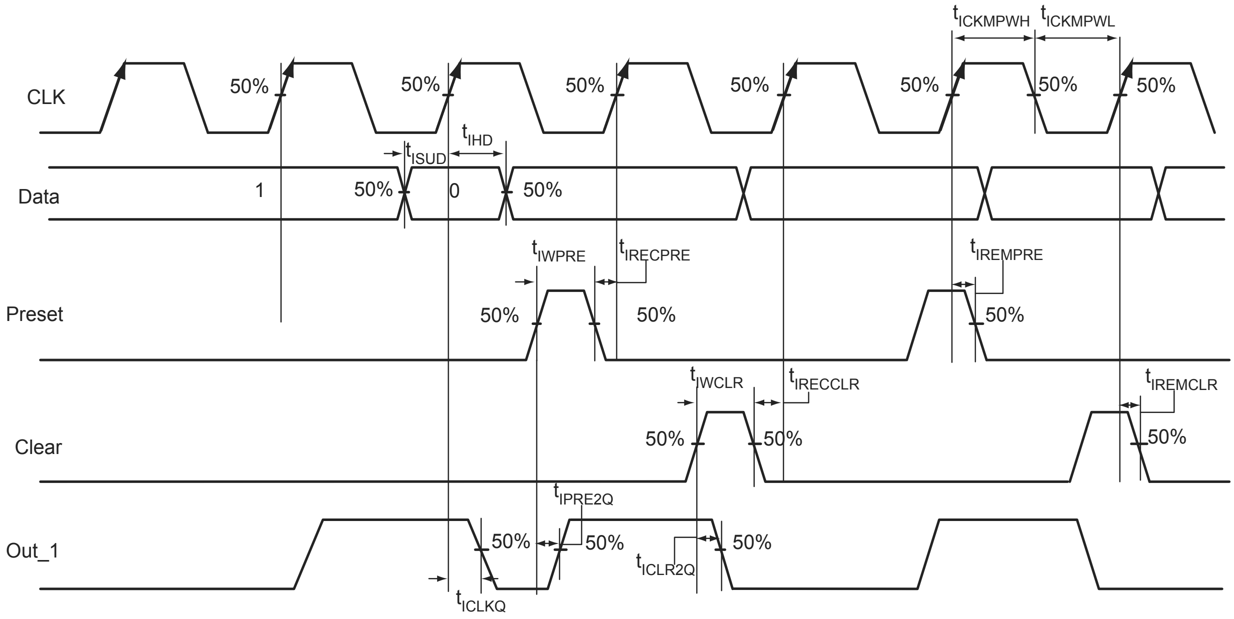


***Figure 2-14 •*** **Input Register Timing Diagram**

### *Timing Characteristics*

#### *1.5 V DC Core Voltage*

***Table 2-72 •*** **Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.42 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.47 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width HIGH for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width LOW for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

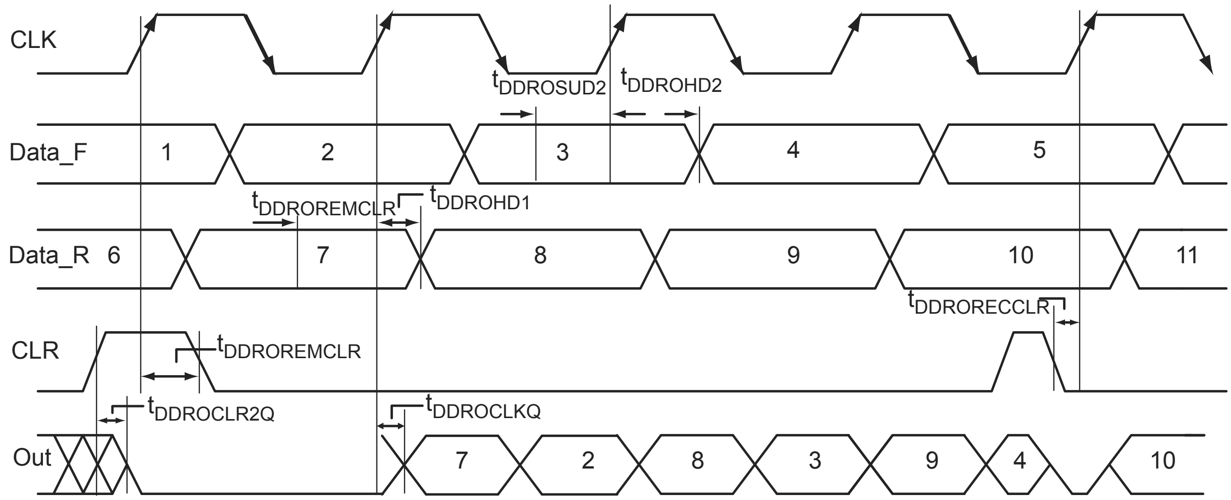


*Figure 2-20 •* **Output DDR Timing Diagram**

### *Timing Characteristics*

#### *1.5 V DC Core Voltage*

*Table 2-82 •* **Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.07 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.67 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.38 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.23 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 250.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-83 • Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.60 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 1.09 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 1.16 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.99 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.24 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 160.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-98 • AGLN125 Global Resource
Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.08 | 2.54 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.15 | 2.77 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.62 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-99 • AGLN250 Global Resource
Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

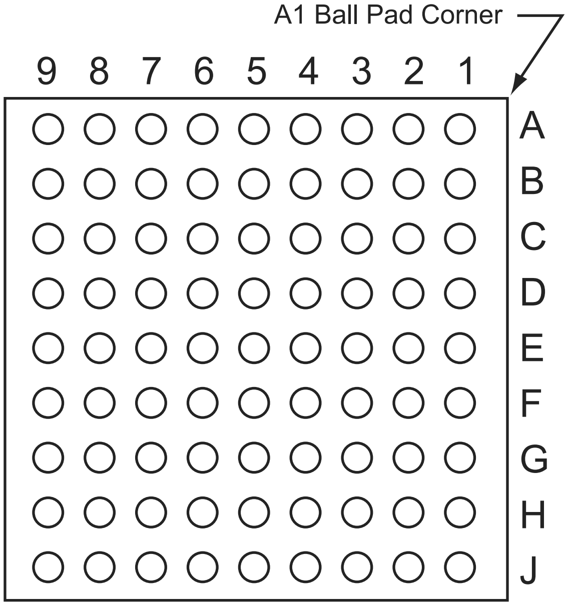
| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.11 | 2.57 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.19 | 2.81 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.62 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

| UC36 | |
|---|---|
| Pin Number | AGLN010 Function |
| A1 | IO21RSB1 |
| A2 | IO18RSB1 |
| A3 | IO13RSB1 |
| A4 | GDC0/IO00RSB0 |
| A5 | IO06RSB0 |
| A6 | GDA0/IO04RSB0 |
| B1 | GEC0/IO37RSB1 |
| B2 | IO20RSB1 |
| B3 | IO15RSB1 |
| B4 | IO09RSB0 |
| B5 | IO08RSB0 |
| B6 | IO07RSB0 |
| C1 | IO22RSB1 |
| C2 | GEA0/IO34RSB1 |
| C3 | GND |
| C4 | GND |
| C5 | VCCIB0 |
| C6 | IO02RSB0 |
| D1 | IO33RSB1 |
| D2 | VCCIB1 |
| D3 | VCC |
| D4 | VCC |
| D5 | IO10RSB0 |
| D6 | IO11RSB0 |
| E1 | IO32RSB1 |
| E2 | FF/IO31RSB1 |
| E3 | TCK |
| E4 | VPUMP |
| E5 | TRST |
| E6 | VJTAG |
| F1 | IO29RSB1 |
| F2 | IO25RSB1 |
| F3 | IO23RSB1 |
| F4 | TDI |
| F5 | TMS |
| F6 | TDO |

# UC81



*Note: This is the bottom view of the package.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| CS81 | |
|---|---|
| Pin Number | AGLN125 Function |
| A1 | GAA0/IO00RSB0 |
| A2 | GAA1/IO01RSB0 |
| A3 | GAC0/IO04RSB0 |
| A4 | IO13RSB0 |
| A5 | IO22RSB0 |
| A6 | IO32RSB0 |
| A7 | GBB0/IO37RSB0 |
| A8 | GBA1/IO40RSB0 |
| A9 | GBA2/IO41RSB0 |
| B1 | GAA2/IO132RSB1 |
| B2 | GAB0/IO02RSB0 |
| B3 | GAC1/IO05RSB0 |
| B4 | IO11RSB0 |
| B5 | IO25RSB0 |
| B6 | GBC0/IO35RSB0 |
| B7 | GBB1/IO38RSB0 |
| B8 | IO42RSB0 |
| B9 | GBB2/IO43RSB0 |
| C1 | GAB2/IO130RSB1 |
| C2 | IO131RSB1 |
| C3 | GND |
| C4 | IO15RSB0 |
| C5 | IO28RSB0 |
| C6 | GND |
| C7 | GBA0/IO39RSB0 |
| C8 | GBC2/IO45RSB0 |
| C9 | IO47RSB0 |
| D1 | GAC2/IO128RSB1 |
| D2 | IO129RSB1 |
| D3 | GFA2/IO117RSB1 |
| D4 | VCC |
| D5 | VCCIB0 |
| D6 | GND |
| D7 | GCC2/IO59RSB0 |
| D8 | GCC1/IO51RSB0 |
| D9 | GCC0/IO52RSB0 |
| E1 | GFB0/IO120RSB1 |
| E2 | GFB1/IO121RSB1 |
| E3 | GFA1/IO118RSB1 |
| E4 | VCCIB1 |
| E5 | VCC |
| E6 | VCCIB0 |
| E7 | GCA0/IO56RSB0 |
| E8 | GCA1/IO55RSB0 |
| E9 | GCB2/IO58RSB0 |
| F1* | VCCPLF |
| F2* | VCOMPLF |
| F3 | GND |
| F4 | GND |
| F5 | VCCIB1 |
| F6 | GND |
| F7 | GDA1/IO65RSB0 |
| F8 | GDC1/IO61RSB0 |
| F9 | GDC0/IO62RSB0 |
| G1 | GEA0/IO104RSB1 |
| G2 | GEC0/IO108RSB1 |
| G3 | GEB1/IO107RSB1 |
| G4 | IO96RSB1 |
| G5 | IO92RSB1 |
| G6 | IO72RSB1 |
| G7 | GDB2/IO68RSB1 |
| G8 | VJTAG |
| G9 | TRST |
| H1 | GEA1/IO105RSB1 |
| H2 | FF/GEB2/IO102RSB1 |
| H3 | IO99RSB1 |
| H4 | IO94RSB1 |
| H5 | IO91RSB1 |
| H6 | IO81RSB1 |
| H7 | GDA2/IO67RSB1 |
| H8 | TDI |
| H9 | TDO |
| J1 | GEA2/IO103RSB1 |
| J2 | GEC2/IO101RSB1 |
| J3 | IO97RSB1 |
| J4 | IO93RSB1 |
| J5 | IO90RSB1 |
| J6 | IO78RSB1 |
| J7 | TCK |
| J8 | TMS |
| J9 | VPUMP |

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN125-CS81.*

| QN48 | |
|---|---|
| Pin Number | AGLN010 Function |
| 1 | GEC0/IO37RSB1 |
| 2 | IO36RSB1 |
| 3 | GEA0/IO34RSB1 |
| 4 | IO22RSB1 |
| 5 | GND |
| 6 | VCCIB1 |
| 7 | IO24RSB1 |
| 8 | IO33RSB1 |
| 9 | IO26RSB1 |
| 10 | IO32RSB1 |
| 11 | IO27RSB1 |
| 12 | IO29RSB1 |
| 13 | IO30RSB1 |
| 14 | FF/IO31RSB1 |
| 15 | IO28RSB1 |
| 16 | IO25RSB1 |
| 17 | IO23RSB1 |
| 18 | VCC |
| 19 | VCCIB1 |
| 20 | IO17RSB1 |
| 21 | IO14RSB1 |
| 22 | TCK |
| 23 | TDI |
| 24 | TMS |
| 25 | VPUMP |
| 26 | TDO |
| 27 | TRST |
| 28 | VJTAG |
| 29 | IO11RSB0 |
| 30 | IO10RSB0 |
| 31 | IO09RSB0 |
| 32 | IO08RSB0 |
| 33 | VCCIB0 |
| 34 | GND |
| 35 | VCC |
| 36 | IO07RSB0 |
| 37 | IO06RSB0 |
| 38 | GDA0/IO05RSB0 |
| 39 | IO03RSB0 |
| 40 | GDC0/IO01RSB0 |
| 41 | IO12RSB1 |
| 42 | IO13RSB1 |
| 43 | IO15RSB1 |
| 44 | IO16RSB1 |
| 45 | IO18RSB1 |
| 46 | IO19RSB1 |
| 47 | IO20RSB1 |
| 48 | IO21RSB1 |

| QN48 | |
|---|---|
| **Pin Number** | **AGLN030Z Function** |
| 1 | IO82RSB1 |
| 2 | GEC0/IO73RSB1 |
| 3 | GEA0/IO72RSB1 |
| 4 | GEB0/IO71RSB1 |
| 5 | GND |
| 6 | VCCIB1 |
| 7 | IO68RSB1 |
| 8 | IO67RSB1 |
| 9 | IO66RSB1 |
| 10 | IO65RSB1 |
| 11 | IO64RSB1 |
| 12 | IO62RSB1 |
| 13 | IO61RSB1 |
| 14 | FF/IO60RSB1 |
| 15 | IO57RSB1 |
| 16 | IO55RSB1 |
| 17 | IO53RSB1 |
| 18 | VCC |
| 19 | VCCIB1 |
| 20 | IO46RSB1 |
| 21 | IO42RSB1 |
| 22 | TCK |
| 23 | TDI |
| 24 | TMS |
| 25 | VPUMP |
| 26 | TDO |
| 27 | TRST |
| 28 | VJTAG |
| 29 | IO38RSB0 |
| 30 | GDB0/IO34RSB0 |
| 31 | GDA0/IO33RSB0 |
| 32 | GDC0/IO32RSB0 |
| 33 | VCCIB0 |
| 34 | GND |
| 35 | VCC |
| 36 | IO25RSB0 |
| 37 | IO24RSB0 |
| 38 | IO22RSB0 |
| 39 | IO20RSB0 |
| 40 | IO18RSB0 |
| 41 | IO16RSB0 |
| 42 | IO14RSB0 |
| 43 | IO10RSB0 |
| 44 | IO08RSB0 |
| 45 | IO06RSB0 |
| 46 | IO04RSB0 |
| 47 | IO02RSB0 |
| 48 | IO00RSB0 |