Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	71
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-20°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln060v5-zvq100

Device Marking

Microsemi normally topside marks the full ordering part number on each device. There are some exceptions to this, such as some of the Z feature grade nano devices, the V2 designator for IGLOO devices, and packages where space is physically limited. Packages that have limited characters available are UC36, UC81, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

Figure 1 shows an example of device marking based on the AGLN250V2-CSG81. The actual mark will vary by the device/package combination ordered.
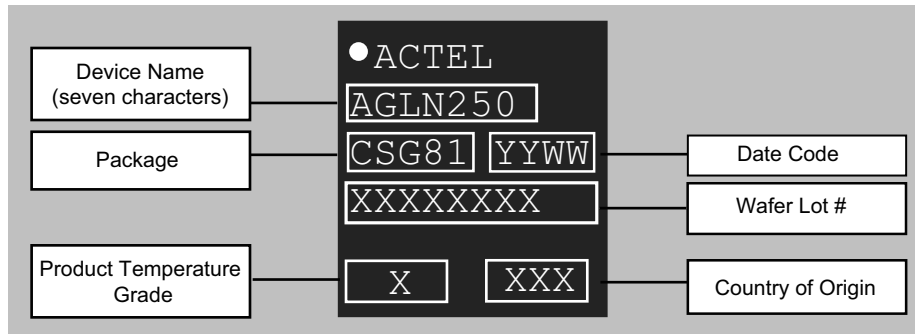
Figure 1 •   **Example of Device Marking for Small Form Factor Packages**

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO nano devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic.

Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO nano device architecture mitigates the need for ASIC migration at higher user volumes. This makes IGLOO nano devices cost-effective ASIC replacement solutions, especially for applications in the consumer, networking/communications, computing, and avionics markets.

With a variety of devices under $1, IGLOO nano FPGAs enable cost-effective implementation of programmable logic and quick time to market.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO nano flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO nano FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO nano device offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO nano FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO nano architecture provides granularity comparable to standard-cell ASICs. The IGLOO nano device consists of five distinct and programmable architectural features (Figure 1-3 on page 1-5 to Figure 1-4 on page 1-5):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO nano core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

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† *The AGLN030 and smaller devices do not support PLL or SRAM.*

2 – IGLOO nano DC and Switching Characteristics

General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash*Freeze bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, and hot-swap I/O capability. Refer to "IGLOO nano Ordering Information" on page IV for more information.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI[1]	I/O input voltage	–0.3 V to 3.6 V	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.46 \text{ W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	200 ft./ min.	500 ft./ min.	Units
Chip Scale Package (CSP)	36	TBD	TBD	TBD	TBD	C/W
	81	TBD	TBD	TBD	TBD	C/W
Quad Flat No Lead (QFN)	48	TBD	TBD	TBD	TBD	C/W
	68	TBD	TBD	TBD	TBD	C/W
	100	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**
For IGLOO nano V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C)						
	−40°C	−20°C	0°C	25°C	70°C	85°C	100°C
1.425	0.947	0.956	0.965	0.978	1.000	1.009	1.013
1.5	0.875	0.883	0.892	0.904	0.925	0.932	0.937
1.575	0.821	0.829	0.837	0.848	0.868	0.875	0.879

Table 2-17 • **Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	2.829	2.875	1.728	0	0	0
PAC2	Clock contribution of a Global Spine	1.731	1.265	1.268	2.562	2.562	1.685
PAC3	Clock contribution of a VersaTile row	0.957	0.963	0.967	0.862	0.862	0.858
PAC4	Clock contribution of a VersaTile used as a sequential module	0.098	0.098	0.098	0.094	0.094	0.091
PAC5	First contribution of a VersaTile used as a sequential module	0.045					
PAC6	Second contribution of a VersaTile used as a sequential module	0.186					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11					
PAC8	Average contribution of a routing net	0.45					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9					
PAC11	Average contribution of a RAM block during a read operation	25.00			N/A		
PAC12	Average contribution of a RAM block during a write operation	30.00			N/A		
PAC13	Dynamic contribution for PLL	2.10			N/A		

Table 2-18 • **Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

Parameter	Definition	Device-Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8					
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7					
PDC4 [1]	Static PLL contribution	0.90			N/A		
PDC5	Bank quiescent power (VCCI-dependent)[2]	See Table 2-12 on page 2-8					

Notes:

1. *Minimum contribution of the PLL when running at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = (PDC1 \text{ or } PDC2 \text{ or } PDC3) + N_{BANKS} * PDC5$

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—P_{S-CELL}

$P_{S-CELL} = N_{S-CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 8 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
–20°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL / LVCMOS (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Applies to 1.2 V DC Core Voltage

Table 2-43 • **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
100 µA	2 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 µA	4 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 µA	6 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns
100 µA	8 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-44 • **3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
100 µA	2 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 µA	4 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 µA	6 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
100 µA	8 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
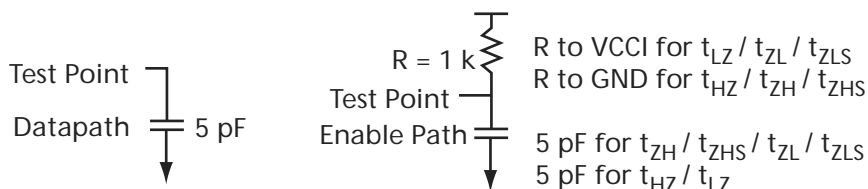3. *Software default selection highlighted in gray.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5 V applications.

Table 2-45 • **Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[3]	Max., mA[3]	μA[4]	μA[4]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Test Point

Datapath — 5 pF

R = 1 k

Test Point

Enable Path

R to VCCI for t_{LZ} / t_{ZL} / t_{ZLS}
R to GND for t_{HZ} / t_{ZH} / t_{ZHS}

5 pF for t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}
5 pF for t_{HZ} / t_{LZ}

Figure 2-8 • **AC Loading**

Table 2-46 • **2.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-59 • **1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.39	0.19	1.19	1.62	0.66	5.48	5.39	2.02	2.06	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-60 • **1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.39	0.19	1.19	1.62	0.66	2.44	2.24	2.02	2.15	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Applies to 1.2 V DC Core Voltage

Table 2-61 • **1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	5.87	0.26	1.27	1.77	1.10	5.92	5.87	2.45	2.65	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-62 • **1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

| Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.78	0.26	1.27	1.77	1.10	2.82	2.62	2.44	2.74	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

DDR Module Specifications

Note: DDR is not supported for AGLN010, AGLN015, and AGLN020 devices.

Input DDR Module
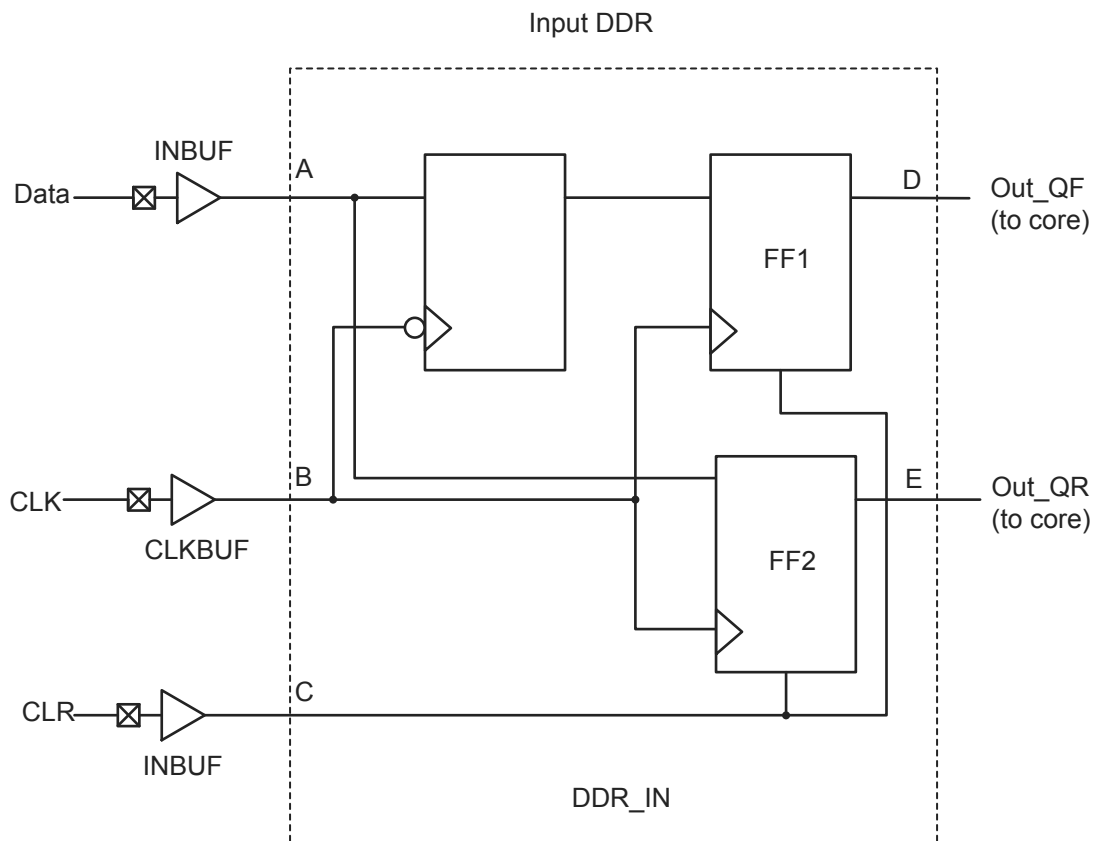
Figure 2-17 • **Input DDR Timing Model**

Table 2-78 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

1.2 V DC Core Voltage

Table 2-83 • **Output DDR Propagation Delays**
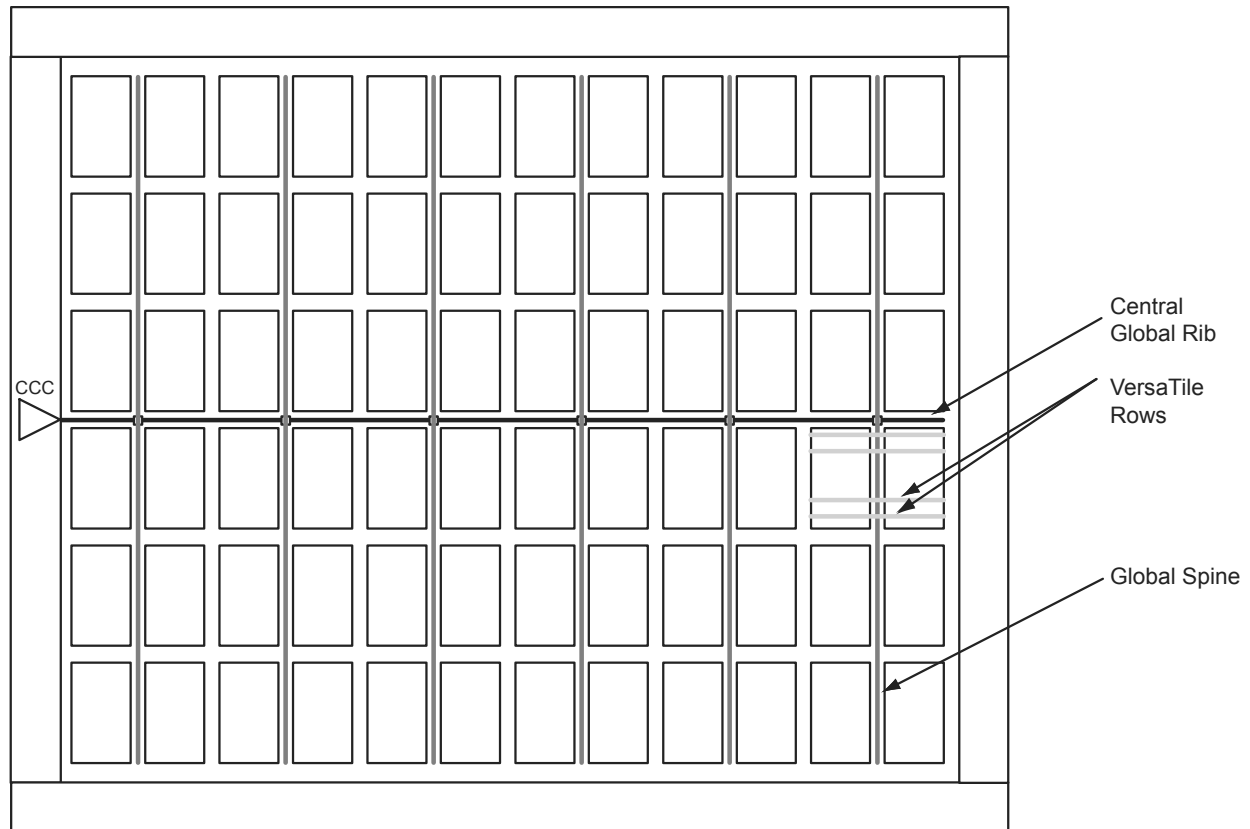**Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V**

Parameter	Description	Std.	Units
t_DDROCLKQ	Clock-to-Out of DDR for Output DDR	1.60	ns
t_DDROSUD1	Data_F Data Setup for Output DDR	1.09	ns
t_DDROSUD2	Data_R Data Setup for Output DDR	1.16	ns
t_DDROHD1	Data_F Data Hold for Output DDR	0.00	ns
t_DDROHD2	Data_R Data Hold for Output DDR	0.00	ns
t_DDROCLR2Q	Asynchronous Clear-to-Out for Output DDR	1.99	ns
t_DDROREMCLR	Asynchronous Clear Removal Time for Output DDR	0.00	ns
t_DDRORECCLR	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
t_DDROWCLR1	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
t_DDROCKMPWH	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
t_DDROCKMPWL	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_DDOMAX	Maximum Frequency for the Output DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Global Resource Characteristics

AGLN125 Clock Tree Topology

Clock delays are device-specific. Figure 2-25 is an example of a global tree used for clock routing. The global tree presented in Figure 2-25 is driven by a CCC located on the west side of the AGLN125 device. It is used to drive all D-flip-flops in the device.

Figure 2-25 • **Example of Global Tree Use in an AGLN125 Device for Clock Routing**

1.2 V DC Core Voltage

Table 2-94 • **AGLN010 Global Resource**
Commercial-Case Conditions: T$_J$ = 70°C, VCC = 1.14 V

| Parameter	Description	Std. Min.[1]	Std. Max.[2]	Units
t$_{RCKL}$	Input Low Delay for Global Clock	1.71	2.09	ns
t$_{RCKH}$	Input High Delay for Global Clock	1.78	2.31	ns
t$_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
t$_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t$_{RCKSW}$	Maximum Skew for Global Clock		0.53	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*

2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*

3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-95 • **AGLN015 Global Resource**
**Commercial-Case Conditions: T$_J$ = 70°C, VCC = 1.14 V**

Parameter	Description	Std. Min.[1]	Std. Max.[2]	Units
t$_{RCKL}$	Input Low Delay for Global Clock	1.81	2.26	ns
t$_{RCKH}$	Input High Delay for Global Clock	1.90	2.51	ns
t$_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
t$_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t$_{RCKSW}$	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*

2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*

3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*
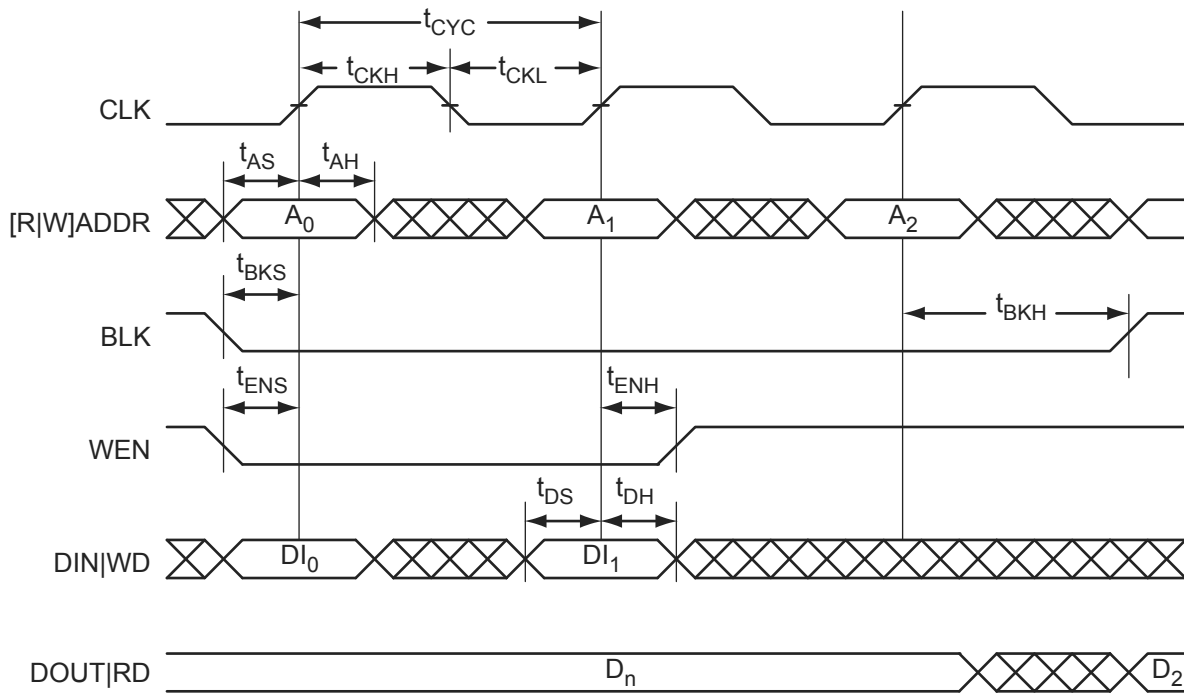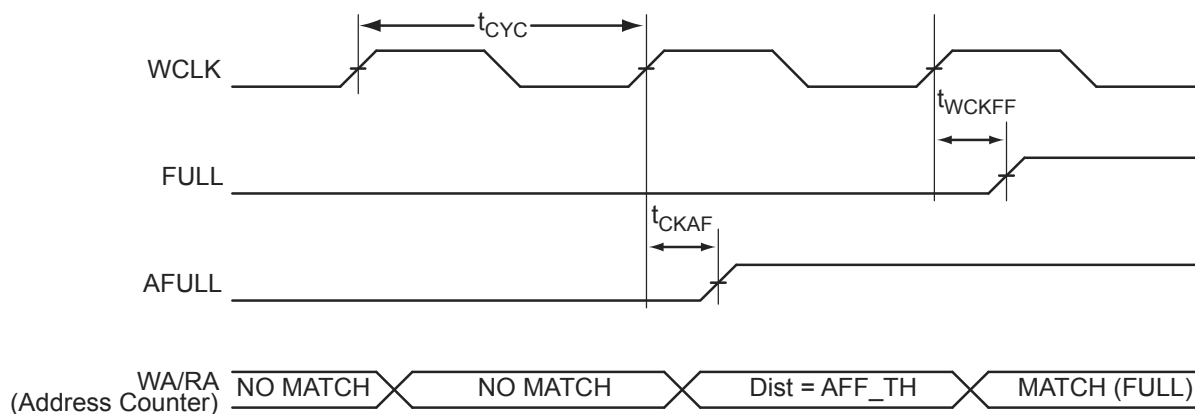
Figure 2-30 • **RAM Write, Output Retained (WMODE = 0). Applicable to Both RAM4K9 and RAM512x18.**
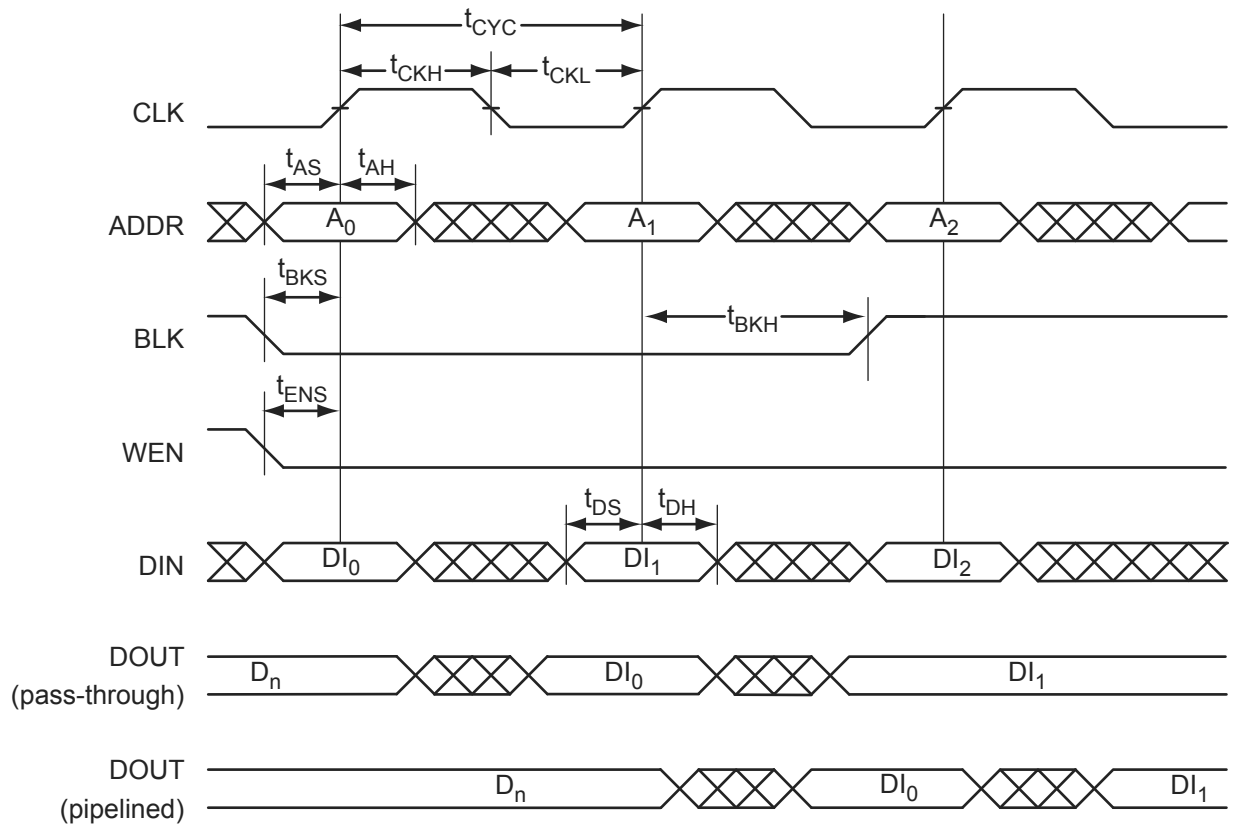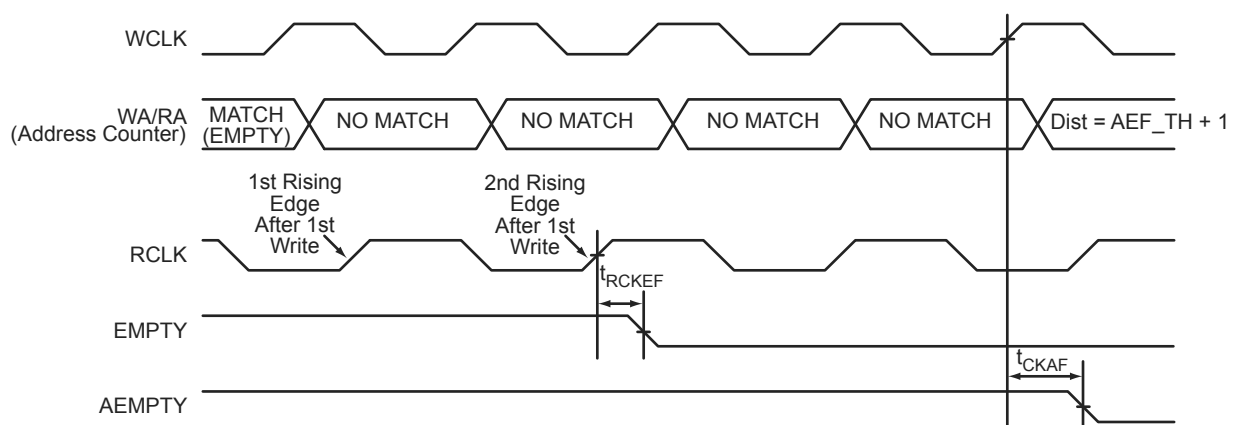

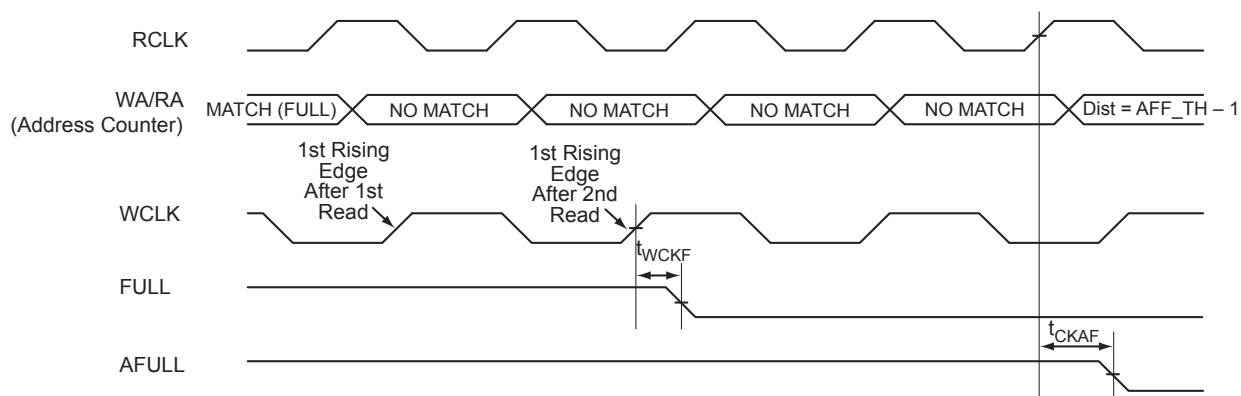*Figure 2-31* • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

Figure 2-38 • **FIFO FULL Flag and AFULL Flag Assertion**

Figure 2-39 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

Figure 2-40 • **FIFO FULL Flag and AFULL Flag Deassertion**

Microsemi

3 – Pin Descriptions

Supply Pins

GND   **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ   **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC   **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO nano V5 devices, and 1.2 V or 1.5 V for IGLOO nano V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx   **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx   **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F   **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V.

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter in the *IGLOO nano FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on IGLOO nano devices.

VCOMPLA/B/C/D/E/F   **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO nano devices.

VJTAG   **JTAG Supply Voltage**

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG

CS81			CS81			CS81	
Pin Number	AGLN250Z Function		Pin Number	AGLN250Z Function		Pin Number	AGLN250Z Function
A1	GAA0/IO00RSB0		E1	GFB0/IO59RSB3		J1	GEA2/IO50RSB2
A2	GAA1/IO01RSB0		E2	GFB1/IO60RSB3		J2	GEC2/IO48RSB2
A3	GAC0/IO04RSB0		E3	GFA1/IO58RSB3		J3	IO46RSB2
A4	IO07RSB0		E4	VCCIB3		J4	IO43RSB2
A5	IO09RSB0		E5	VCC		J5	IO40RSB2
A6	IO12RSB0		E6	VCCIB1		J6	IO38RSB2
A7	GBB0/IO16RSB0		E7	GCA0/IO28RSB1		J7	TCK
A8	GBA1/IO19RSB0		E8	GCA1/IO27RSB1		J8	TMS
A9	GBA2/IO20RSB1		E9	GCB2/IO29RSB1		J9	VPUMP
B1	GAA2/IO67RSB3		F1*	VCCPLF			
B2	GAB0/IO02RSB0		F2*	VCOMPLF			
B3	GAC1/IO05RSB0		F3	GND			
B4	IO06RSB0		F4	GND			
B5	IO10RSB0		F5	VCCIB2			
B6	GBC0/IO14RSB0		F6	GND			
B7	GBB1/IO17RSB0		F7	GDA1/IO33RSB1			
B8	IO21RSB1		F8	GDC1/IO31RSB1			
B9	GBB2/IO22RSB1		F9	GDC0/IO32RSB1			
C1	GAB2/IO65RSB3		G1	GEA0/IO51RSB3			
C2	IO66RSB3		G2	GEC1/IO54RSB3			
C3	GND		G3	GEC0/IO53RSB3			
C4	IO08RSB0		G4	IO45RSB2			
C5	IO11RSB0		G5	IO42RSB2			
C6	GND		G6	IO37RSB2			
C7	GBA0/IO18RSB0		G7	GDB2/IO35RSB2			
C8	GBC2/IO23RSB1		G8	VJTAG			
C9	IO24RSB1		G9	TRST			
D1	GAC2/IO63RSB3		H1	GEA1/IO52RSB3			
D2	IO64RSB3		H2	FF/GEB2/IO49RSB2			
D3	GFA2/IO56RSB3		H3	IO47RSB2			
D4	VCC		H4	IO44RSB2			
D5	VCCIB0		H5	IO41RSB2			
D6	GND		H6	IO39RSB2			
D7	IO30RSB1		H7	GDA2/IO34RSB2			
D8	GCC1/IO25RSB1		H8	TDI			
D9	GCC0/IO26RSB1		H9	TDO			

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250Z-CS81.*

VQ100	
Pin Number	AGLN250 Function
1	GND
2	GAA2/IO67RSB3
3	IO66RSB3
4	GAB2/IO65RSB3
5	IO64RSB3
6	GAC2/IO63RSB3
7	IO62RSB3
8	IO61RSB3
9	GND
10	GFB1/IO60RSB3
11	GFB0/IO59RSB3
12	VCOMPLF
13	GFA0/IO57RSB3
14	VCCPLF
15	GFA1/IO58RSB3
16	GFA2/IO56RSB3
17	VCC
18	VCCIB3
19	GFC2/IO55RSB3
20	GEC1/IO54RSB3
21	GEC0/IO53RSB3
22	GEA1/IO52RSB3
23	GEA0/IO51RSB3
24	VMV3
25	GNDQ
26	GEA2/IO50RSB2
27	FF/GEB2/IO49RSB2
28	GEC2/IO48RSB2
29	IO47RSB2
30	IO46RSB2
31	IO45RSB2
32	IO44RSB2
33	IO43RSB2
34	IO42RSB2
35	IO41RSB2
36	IO40RSB2

VQ100	
Pin Number	AGLN250 Function
37	VCC
38	GND
39	VCCIB2
40	IO39RSB2
41	IO38RSB2
42	IO37RSB2
43	GDC2/IO36RSB2
44	GDB2/IO35RSB2
45	GDA2/IO34RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO33RSB1
58	GDC0/IO32RSB1
59	GDC1/IO31RSB1
60	IO30RSB1
61	GCB2/IO29RSB1
62	GCA1/IO27RSB1
63	GCA0/IO28RSB1
64	GCC0/IO26RSB1
65	GCC1/IO25RSB1
66	VCCIB1
67	GND
68	VCC
69	IO24RSB1
70	GBC2/IO23RSB1
71	GBB2/IO22RSB1
72	IO21RSB1

VQ100	
Pin Number	AGLN250 Function
73	GBA2/IO20RSB1
74	VMV1
75	GNDQ
76	GBA1/IO19RSB0
77	GBA0/IO18RSB0
78	GBB1/IO17RSB0
79	GBB0/IO16RSB0
80	GBC1/IO15RSB0
81	GBC0/IO14RSB0
82	IO13RSB0
83	IO12RSB0
84	IO11RSB0
85	IO10RSB0
86	IO09RSB0
87	VCCIB0
88	GND
89	VCC
90	IO08RSB0
91	IO07RSB0
92	IO06RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

Revision / Version	Changes	Page
Revision 1 (cont'd) Packaging Advance v0.2	The "QN48" pin diagram was revised.	4-16
	Note 2 for the "QN48", "QN68", and "100-Pin QFN" pin diagrams was changed to "The die attach paddle of the package is tied to ground (GND)."	4-16, 4-19
	The "VQ100" pin diagram was revised to move the pin IDs to the upper left corner instead of the upper right corner.	4-23
Revision 0 (Oct 2008) Product Brief Advance v0.2	The following tables and sections were updated to add the UC81 and CS81 packages for AGL030: "IGLOO nano Devices" "I/Os Per Package" "IGLOO nano Products Available in the Z Feature Grade" "Temperature Grade Offerings"	N/A
	The "I/Os Per Package" table was updated to add the following information to table note 4: "For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only."	II
	The "IGLOO nano Products Available in the Z Feature Grade" section was updated to remove QN100 for AGLN250.	VI
	The device architecture figures, Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125) through Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250), were revised. Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030) is new.	1-4 through 1-5
	The "PLL and CCC" section was revised to include information about CCC-GLs in AGLN020 and smaller devices.	1-7
	The "I/Os with Advanced I/O Standards" section was revised to add information about IGLOO nano devices supporting double-data-rate applications.	1-8