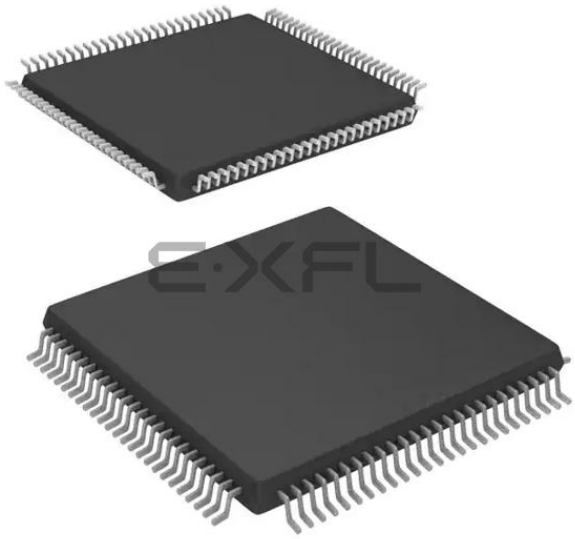


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

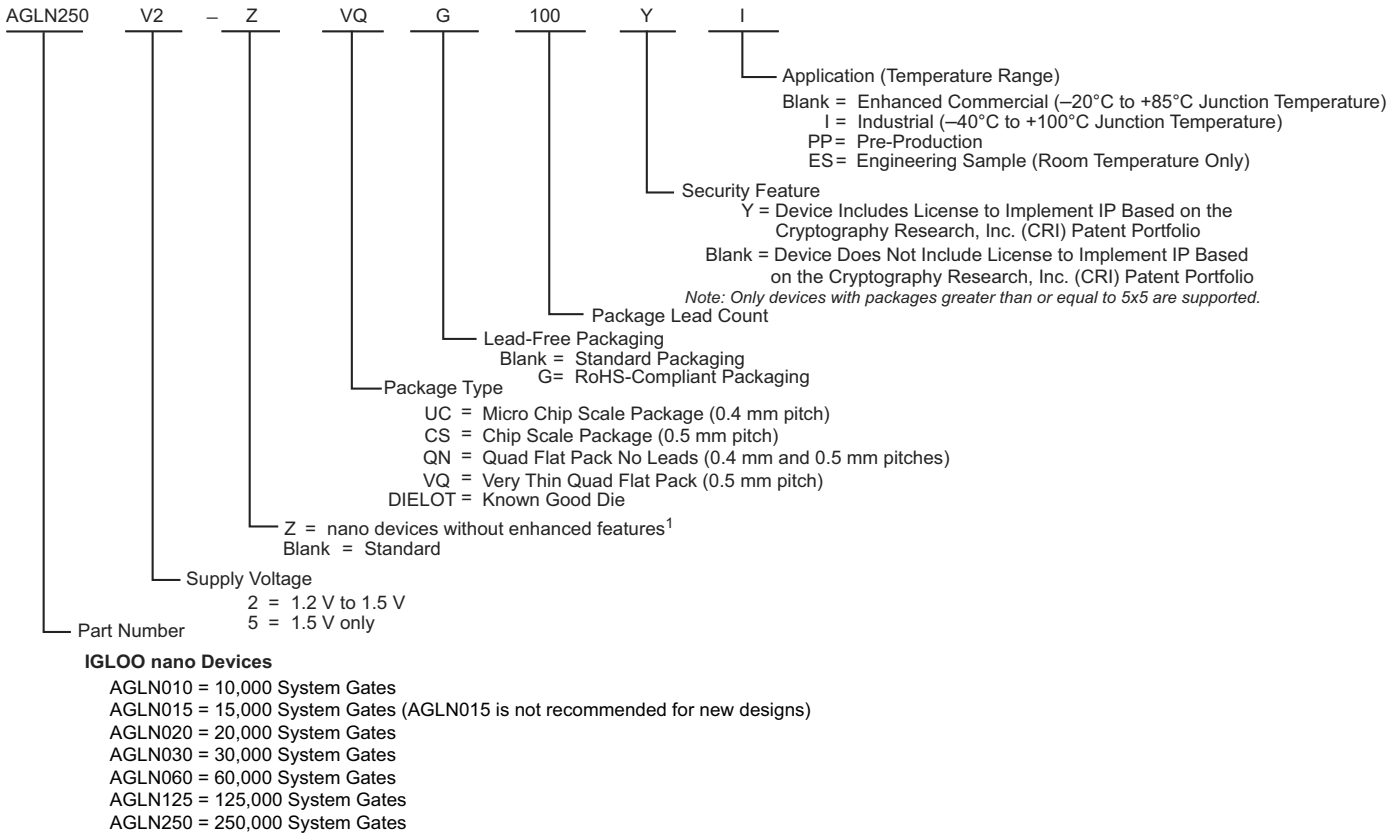
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3072
Total RAM Bits	36864
Number of I/O	71
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln125v5-vq100i

IGLOO nano Ordering Information



IGLOO nano Devices

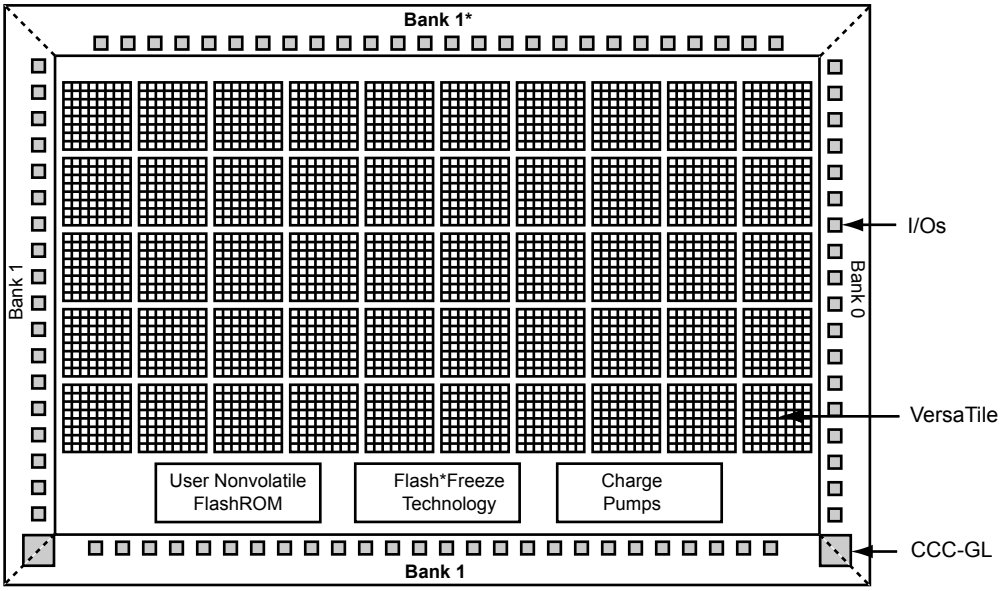
AGLN010 = 10,000 System Gates
AGLN015 = 15,000 System Gates (AGLN015 is not recommended for new designs)
AGLN020 = 20,000 System Gates
AGLN030 = 30,000 System Gates
AGLN060 = 60,000 System Gates
AGLN125 = 125,000 System Gates
AGLN250 = 250,000 System Gates

Notes:

1. *Z-feature grade devices AGLN060Z, AGLN125Z, and AGLN250Z do not support the enhanced nano features of Schmitt Trigger input, bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, hot-swap I/O capability and 1.2 V programming. The AGLN030 Z feature grade does not support Schmitt trigger input, bus hold and 1.2 V programming. For the VQ100, CS81, UC81, QN68, and QN48 packages, the Z feature grade and the N part number are not marked on the device. Z feature grade devices are not recommended for new designs.*
2. *AGLN030 is available in the Z feature grade only.*
3. *Marking Information: IGLOO nano V2 devices do not have a V2 marking, but IGLOO nano V5 devices are marked with a V5 designator.*

Devices Not Recommended For New Designs

AGLN015, AGLN030Z, AGLN060Z, AGLN125Z, and AGLN250Z are not recommended for new designs. For more information on obsoleted devices/packages, refer to the *PDN1503 - IGLOO nano Z and ProASIC3 nano Z Families*.



*Note: *Bank 0 for the AGLN030 device*

Figure 1-1 • **IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030)**

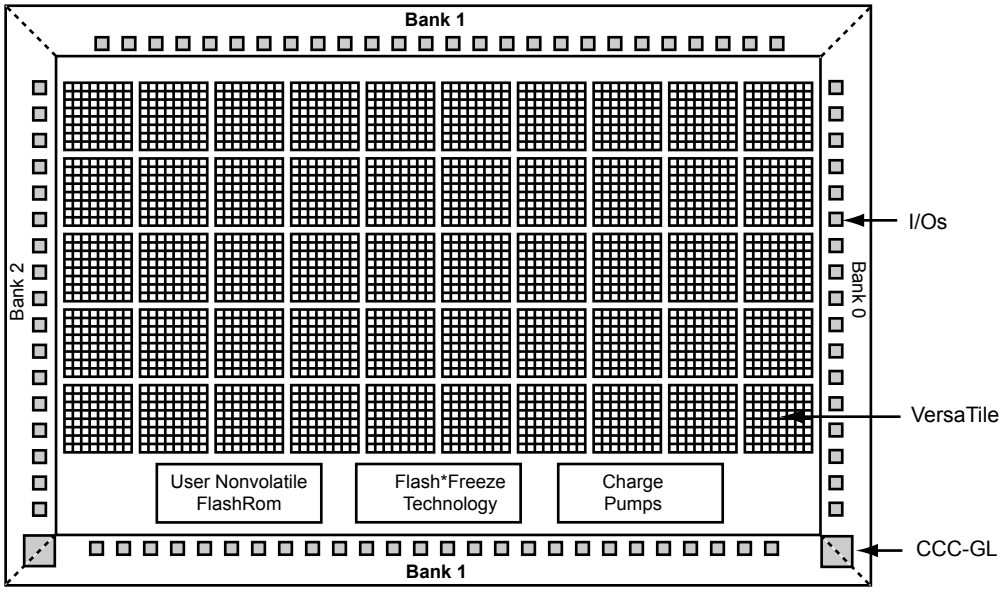


Figure 1-2 • **IGLOO Device Architecture Overview with Three I/O Banks and No RAM (AGLN015 and AGLN020)**

Table 2-2 • **Recommended Operating Conditions [1]**

Symbol	Parameter		Extended Commercial	Industrial	Units
T_J	Junction temperature		–20 to + 85[2]	–40 to +100[2]	°C
VCC	1.5 V DC core supply voltage[3]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage[4,5]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP [6]	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL[7]	Analog power supply (PLL)	1.5 V DC core supply voltage[3]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core supply voltage[4]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [8,9]	1.2 V DC supply voltage [4]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage [4]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V DC wide range supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero Online Help.*
3. *For IGLOO® nano V5 devices*
4. *For IGLOO nano V2 devices only, operating at VCCI ≥ VCC*
5. *IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5 V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2 V (with FlashPro4 only) or 1.5 V. If you are using FlashPro3 and want to do in-system programming using 1.2 V, please contact the factory.*
6. *V_{PUMP} can be left floating during operation (not programming mode).*
7. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.*
8. *VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.*
9. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Table 2-3 • **Flash Programming Limits – Retention, Storage, and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Power Consumption of Various Internal Resources

Table 2-15 • **Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	4.421	4.493	2.700	0	0	0
PAC2	Clock contribution of a Global Spine	2.704	1.976	1.982	4.002	4.002	2.633
PAC3	Clock contribution of a VersaTile row	1.496	1.504	1.511	1.346	1.346	1.340
PAC4	Clock contribution of a VersaTile used as a sequential module	0.152	0.153	0.153	0.148	0.148	0.143
PAC5	First contribution of a VersaTile used as a sequential module	0.057					
PAC6	Second contribution of a VersaTile used as a sequential module	0.207					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.17					
PAC8	Average contribution of a routing net	0.7					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9.					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14.					
PAC11	Average contribution of a RAM block during a read operation	25.00			N/A		
PAC12	Average contribution of a RAM block during a write operation	30.00			N/A		
PAC13	Dynamic contribution for PLL	2.70			N/A		

Table 2-16 • **Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device -Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8					
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7					
PDC4 [1]	Static PLL contribution	1.84			N/A		
PDC5	Bank quiescent power (VCCI-dependent)[2]	See Table 2-12 on page 2-8					

Notes:

1. *Minimum contribution of the PLL when running at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.*

Applies to IGLOO nano at 1.2 V Core Operating Conditions

Table 2-26 • **Summary of I/O Timing Characteristics—Software Default Settings**
STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY})	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
3.3 V LVCMOS Wide Range[2]	100 µA	8 mA	High	5 pF	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
2.5 V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
1.8 V LVCMOS	4 mA	4 mA	High	5 pF	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns
1.5 V LVCMOS	2 mA	2 mA	High	5 pF	1.55	2.78	0.26	1.27	1.77	1.10	2.82	2.62	2.44	2.74	ns
1.2 V LVCMOS	1 mA	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns
1.2 V LVCMOS Wide Range[3]	100 µA	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V side range as specified in the JESD8-12 specification.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 8 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
–20°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL / LVCMOS (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

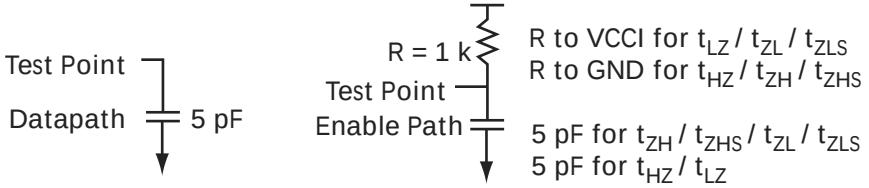


Figure 2-9 • AC Loading

Table 2-52 • 1.8 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-57 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

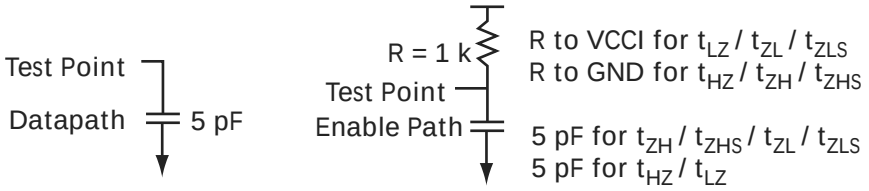


Figure 2-10 • AC Loading

Table 2-58 • 1.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

DDR Module Specifications

Note: DDR is not supported for AGLN010, AGLN015, and AGLN020 devices.

Input DDR Module

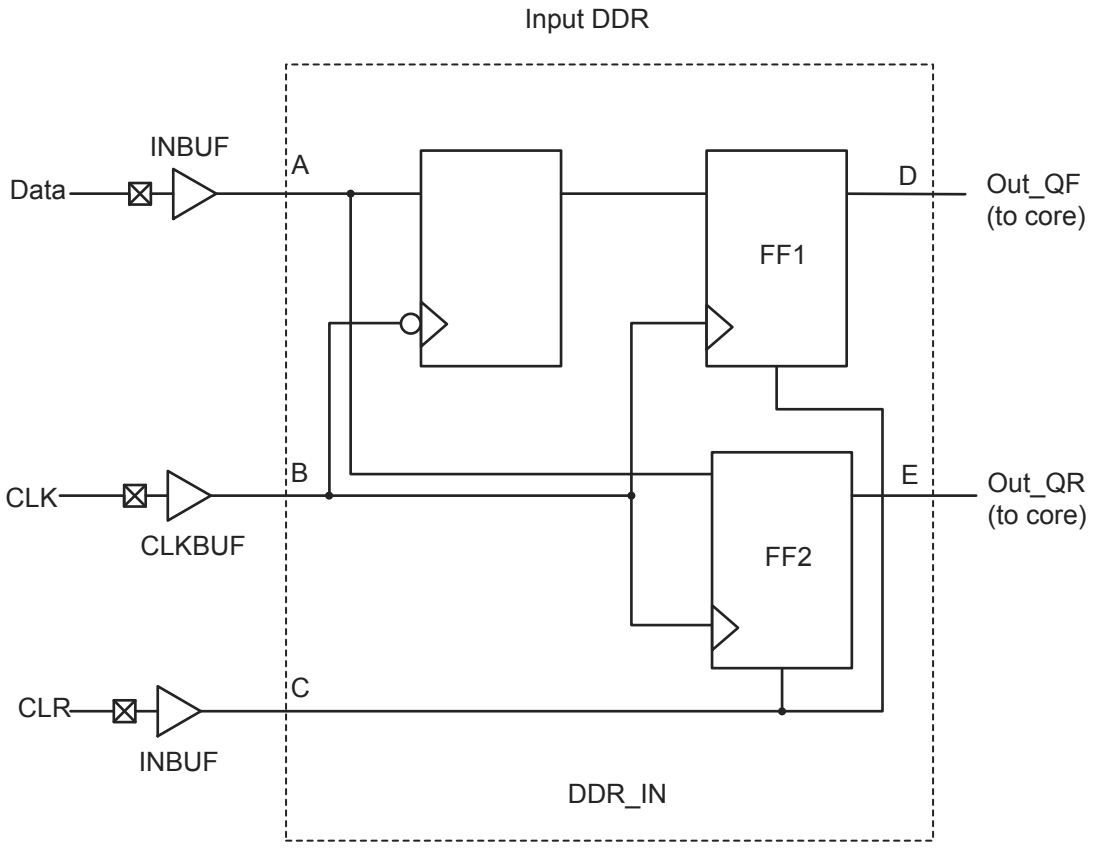


Figure 2-17 • **Input DDR Timing Model**

Table 2-78 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

VersaTile Specifications as a Sequential Module

The IGLOO nano library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for Software v10.1*.

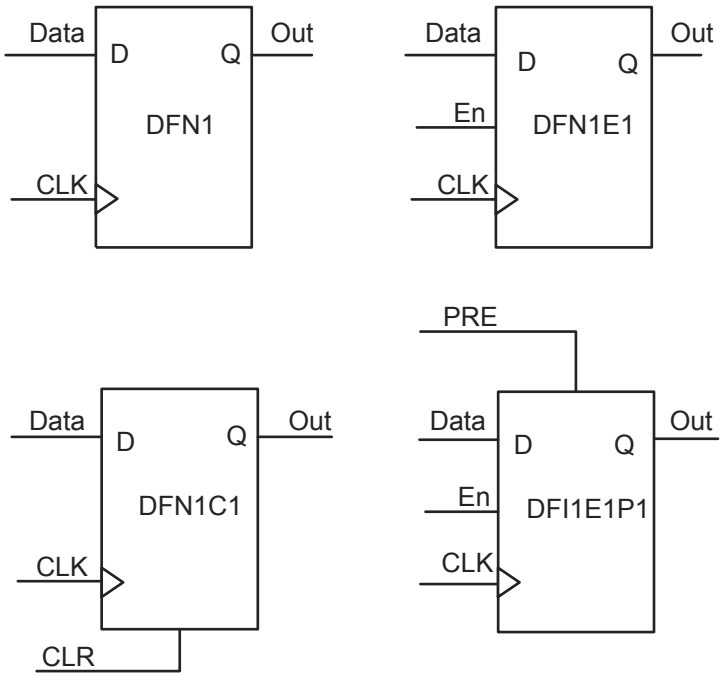
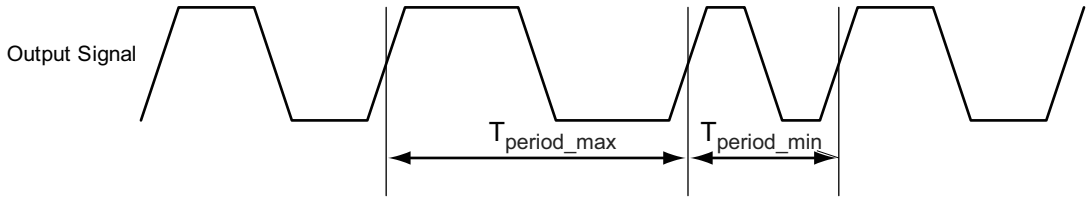


Figure 2-23 • **Sample of Sequential Cells**



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-26 • **Peak-to-Peak Jitter Definition**

***Table 2-105* • RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.13	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{DS}	Input data (WD) setup time	1.10	ns
t_{DH}	Input data (WD) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	6.56	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	2.67	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.87	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.04	ns
t_{RSTBQ}	RESET LOW to data out LOW on RD (flow through)	3.21	ns
	RESET LOW to data out LOW on RD (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

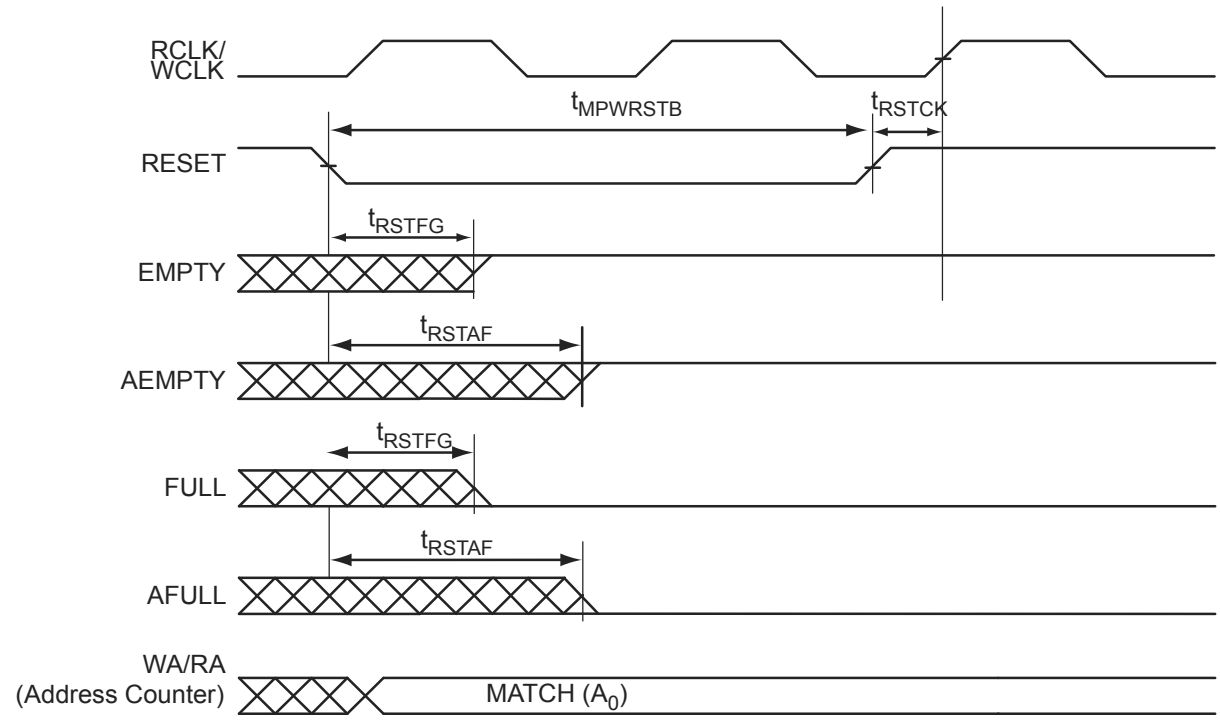


Figure 2-36 • **FIFO Reset**

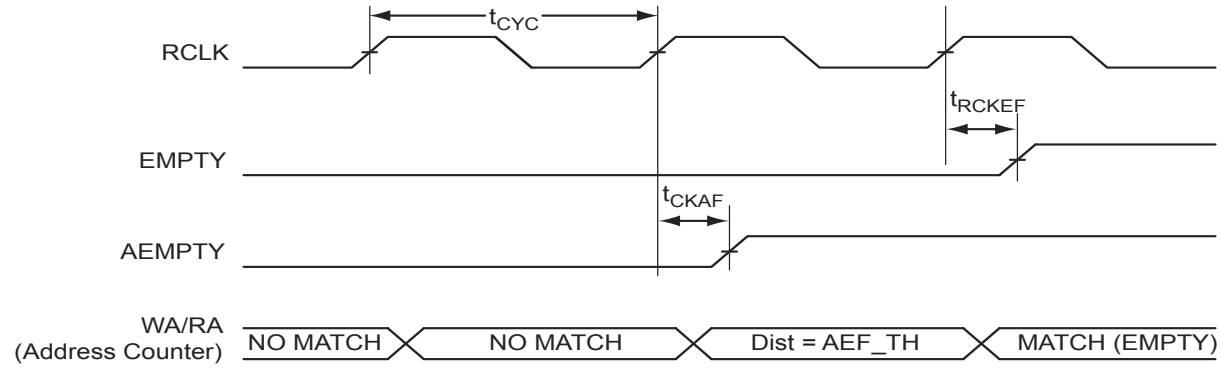


Figure 2-37 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-106 • FIFO

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	ns
t_{ENH}	REN, WEN Hold Time	0.13	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.63	ns
t_{DH}	Input Data (WD) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET Low to Data Out LOW on RD (flow-through)	1.68	ns
	RESET Low to Data Out LOW on RD (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET Removal	0.51	ns
$t_{RECRSTB}$	RESET Recovery	2.68	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

CS81	
Pin Number	**AGLN060 Function**
A1	GAA0/IO02RSB0
A2	GAA1/IO03RSB0
A3	GAC0/IO06RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO18RSB0
A7	GBB0/IO21RSB0
A8	GBA1/IO24RSB0
A9	GBA2/IO25RSB0
B1	GAA2/IO95RSB1
B2	GAB0/IO04RSB0
B3	GAC1/IO07RSB0
B4	IO08RSB0
B5	IO15RSB0
B6	GBC0/IO19RSB0
B7	GBB1/IO22RSB0
B8	IO26RSB0
B9	GBB2/IO27RSB0
C1	GAB2/IO93RSB1
C2	IO94RSB1
C3	GND
C4	IO10RSB0
C5	IO17RSB0
C6	GND
C7	GBA0/IO23RSB0
C8	GBC2/IO29RSB0
C9	IO31RSB0
D1	GAC2/IO91RSB1
D2	IO92RSB1
D3	GFA2/IO80RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO43RSB0

CS81	
Pin Number	**AGLN060 Function**
D8	GCC1/IO35RSB0
D9	GCC0/IO36RSB0
E1	GFB0/IO83RSB1
E2	GFB1/IO84RSB1
E3	GFA1/IO81RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GCA1/IO39RSB0
E8	GCA0/IO40RSB0
E9	GCB2/IO42RSB0
F1[1]	VCCPLF
F2[1]	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO49RSB0
F8	GDC1/IO45RSB0
F9	GDC0/IO46RSB0
G1	GEA0/IO69RSB1
G2	GEC1/IO74RSB1
G3	GEB1/IO72RSB1
G4	IO63RSB1
G5	IO60RSB1
G6	IO54RSB1
G7	GDB2/IO52RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO70RSB1
H2	FF/GEB2/IO67RSB1
H3	IO65RSB1
H4	IO62RSB1
H5	IO59RSB1

CS81	
Pin Number	**AGLN060 Function**
H6	IO56RSB1
H7[2]	GDA2/IO51RSB1
H8	TDI
H9	TDO
J1	GEA2/IO68RSB1
J2	GEC2/IO66RSB1
J3	IO64RSB1
J4	IO61RSB1
J5	IO58RSB1
J6	IO55RSB1
J7	TCK
J8	TMS
J9	VPUMP

Notes:

1. *Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN060-CS81.*
2. *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin H7 in AGLN060-CS81.*

CS81	
Pin Number	**AGLN250 Function**
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO12RSB0
A7	GBB0/IO16RSB0
A8	GBA1/IO19RSB0
A9	GBA2/IO20RSB1
B1	GAA2/IO67RSB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO06RSB0
B5	IO10RSB0
B6	GBC0/IO14RSB0
B7	GBB1/IO17RSB0
B8	IO21RSB1
B9	GBB2/IO22RSB1
C1	GAB2/IO65RSB3
C2	IO66RSB3
C3	GND
C4	IO08RSB0
C5	IO11RSB0
C6	GND
C7	GBA0/IO18RSB0
C8	GBC2/IO23RSB1
C9	IO24RSB1
D1	GAC2/IO63RSB3
D2	IO64RSB3
D3	GFA2/IO56RSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO30RSB1
D8	GCC1/IO25RSB1
D9	GCC0/IO26RSB1

CS81	
Pin Number	**AGLN250 Function**
E1	GFB0/IO59RSB3
E2	GFB1/IO60RSB3
E3	GFA1/IO58RSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1
E7	GCA0/IO28RSB1
E8	GCA1/IO27RSB1
E9	GCB2/IO29RSB1
F1	VCCPLF
F2	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO33RSB1
F8	GDC1/IO31RSB1
F9	GDC0/IO32RSB1
G1	GEA0/IO51RSB3
G2	GEC1/IO54RSB3
G3	GEC0/IO53RSB3
G4	IO45RSB2
G5	IO42RSB2
G6	IO37RSB2
G7	GDB2/IO35RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO52RSB3
H2	FF/GEB2/IO49RSB2
H3	IO47RSB2
H4	IO44RSB2
H5	IO41RSB2
H6	IO39RSB2
H7	GDA2/IO34RSB2
H8	TDI
H9	TDO

CS81	
Pin Number	**AGLN250 Function**
J1	GEA2/IO50RSB2
J2	GEC2/IO48RSB2
J3	IO46RSB2
J4	IO43RSB2
J5	IO40RSB2
J6	IO38RSB2
J7	TCK
J8	TMS
J9	VPUMP

*Note: * Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250-CS81.*

VQ100	
Pin Number	**AGLN060Z Function**
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1

VQ100	
Pin Number	**AGLN060Z Function**
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45*	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC

VQ100	
Pin Number	**AGLN060Z Function**
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

*Note: *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin 45 in AGLN060Z-VQ100.*

VQ100	
Pin Number	AGLN125Z Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1

VQ100	
Pin Number	AGLN125Z Function
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0

VQ100	
Pin Number	AGLN125Z Function
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

Revision / Version	Changes	Page
Revision 9 (Mar2010) Product Brief Advance v0.9 Packaging Advance v0.8	All product tables and pin tables were updated to show clearly that AGLN030 is available only in the Z feature grade at this time. The nano-Z feature grade devices are designated with a Z at the end of the part number.	N/A
Revision 8 (Jan 2009)	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance".	I
Product Brief Advance v0.8	The note for AGLN030 in the "IGLOO nano Devices" table and "I/Os Per Package" table was revised to remove the statement regarding package compatibility with lower density nano devices.	II, II
	The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing.	1-8
Packaging Advance v0.7	The "UC81", "CS81", "QN48", and "QN68" pin tables for AGLN030 are new.	4-5, 4-8, 4-17, 4-21
	The "CS81"pin table for AGLN060 is new.	4-9
	The "CS81" and "VQ100" pin tables for AGLN060Z are new.	4-10, 4-25
	The "CS81" and "VQ100" pin tables for AGLN125Z are new.	4-12, 4-27
	The "CS81" and "VQ100" pin tables for AGLN250Z is new.	4-14, 4-29
Revision 7 (Apr 2009) Product Brief Advance v0.7 DC and Switching Characteristics Advance v0.3	The –F speed grade is no longer offered for IGLOO nano devices and was removed from the datasheet.	N/A
Revision 6 (Mar 2009) Packaging Advance v0.6	The "VQ100" pin table for AGLN030 is new.	4-23
Revision 5 (Feb 2009) Packaging Advance v0.5	The "100-Pin QFN" section was removed.	N/A
Revision 4 (Feb 2009)	The QN100 package was removed for all devices.	N/A
Product Brief Advance v0.6	"IGLOO nano Devices" table was updated to change the maximum user I/Os for AGLN030 from 81 to 77.	II
	The "Device Marking" section is new.	V
Revision 3 (Feb 2009) Product Brief Advance v0.5	The following table note was removed from "IGLOO nano Devices" table: "Six chip (main) and three quadrant global networks are available for AGLN060 and above."	II
	The CS81 package was added for AGLN250 in the "IGLOO nano Products Available in the Z Feature Grade" table.	VI
Packaging Advance v0.4	The "UC81" and "CS81" pin tables for AGLN020 are new.	4-4, 4-7
	The "CS81" pin table for AGLN250 is new.	4-13

Revision / Version	Changes	Page
Revision 2 (Dec 2008) Product Brief Advance v0.4	The second table note in "IGLOO nano Devices" table was revised to state, "AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. AGLN030 and smaller devices do not support this feature."	II
	The I/Os per package for CS81 were revised to 60 for AGLN060, AGLN125, and AGLN250 in the "I/Os Per Package"table.	II
Packaging Advance v0.3	The "UC36" pin table is new.	4-2
Revision 1 (Nov 2008) Product Brief Advance v0.3	The "Advanced I/Os" section was updated to include wide power supply voltage support for 1.14 V to 1.575 V.	I
	The AGLN030 device was added to product tables and replaces AGL030 entries that were formerly in the tables.	VI
	The "I/Os Per Package"table was updated for the CS81 package to change the number of I/Os for AGLN060, AGLN125, and AGLN250 from 66 to 64.	II
	The "Wide Range I/O Support" section is new.	1-8
	The table notes and references were revised in Table 2-2 • Recommended Operating Conditions [1]. VMV was included with VCCI and a table note was added stating, "VMV pins must be connected to the corresponding VCCI pins. See *Pin Descriptions* for further information." Please review carefully.	2-2
	VJTAG was added to the list in the table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Flash*Freeze Mode*. Values were added for AGLN010, AGLN015, and AGLN030 for 1.5 V.	2-7
	VCCI was removed from the list in the table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode*.	2-8
	Values for I_{CCA} current were updated for AGLN010, AGLN015, and AGLN030 in Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode[1].	2-8
	Values for PAC1 and PAC2 were added to Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices and Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices.	2-10, 2-11
	Table notes regarding wide range support were added to Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels.	2-19
	1.2 V LVCMOS wide range values were added to Table 2-22 • Summary of Maximum and Minimum DC Input Levels and Table 2-23 • Summary of AC Measuring Points.	2-19, 2-20
	The following table note was added to Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings and Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings: "All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification."	2-21
	3.3 V LVCMOS Wide Range and 1.2 V Wide Range were added to Table 2-28 • I/O Output Buffer Maximum Resistances [1] andTable 2-30 • I/O Short Currents IOSH/IOSL.	2-23, 2-24