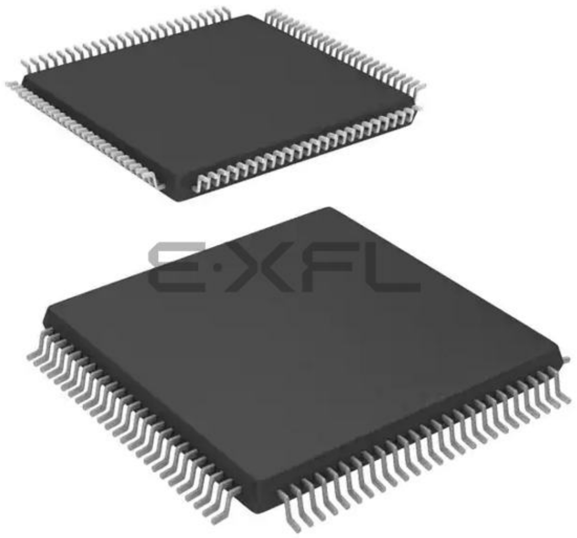
# Microchip Technology - AGLN125V5-ZVQG100I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 3072 |
| Total RAM Bits | 36864 |
| Number of I/O | 71 |
| Number of Gates | 125000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agln125v5-zvqg100i |

| IGLOO nano Devices | AGLN010 | AGLN015[1] | AGLN020 | | AGLN060 | AGLN125 | AGLN250 |
|---|---|---|---|---|---|---|---|
| IGLOO nano-Z Devices[1] | | | | AGLN030Z[1] | AGLN060Z[1] | AGLN125Z[1] | AGLN250Z[1] |
| Package Pins | | | | | | | |
| UC/CS | UC36 | | UC81, CS81 | UC81, CS81 | CS81 | CS81 | CS81 |
| QFN | QN48 | QN68 | QN68 | QN48, QN68 | | | |
| VQFP | | | | VQ100 | VQ100 | VQ100 | VQ100 |

*Notes:*

1. *Not recommended for new designs. Few devices/packages are obsoleted. For more information on obsoleted devices/packages, refer to the PDN 1503 - IGLOO nano Z and ProASIC3 nano Z Families.*
2. *AGLN030 and smaller devices do not support this feature.*
3. *AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs.*
4. *For higher densities and support of additional features, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOOe Low-Power Flash FPGAs Datasheet .*

# I/Os Per Package

| IGLOO nano Devices | AGLN010 | AGLN015[1] | AGLN020 | | AGLN060 | AGLN125 | AGLN250 |
|---|---|---|---|---|---|---|---|
| **IGLOO nano-Z Devices[1]** | | | | **AGLN030Z[1]** | **AGLN060Z[1]** | **AGLN125Z[1]** | **AGLN250Z[1]** |
| Known Good Die | 34 | – | 52 | 83 | 71 | 71 | 68 |
| UC36 | 23 | – | – | – | – | – | – |
| QN48 | 34 | – | – | 34 | – | – | – |
| QN68 | – | 49 | 49 | 49 | – | – | – |
| UC81 | – | – | 52 | 66 | – | – | – |
| CS81 | – | – | 52 | 66 | 60 | 60 | 60 |
| VQ100 | – | – | – | 77 | 71 | 71 | 68 |

*Notes:*

1. *Not recommended for new designs.*
2. *When considering migrating your design to a lower- or higher-density device, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOO FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.*
3. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
4. *"G" indicates RoHS-compliant packages. Refer to "IGLOO nano Ordering Information" on page IV for the location of the "G" in the part number. For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.*

***Table 1* • IGLOO nano FPGAs Package Sizes Dimensions**

| Packages | UC36 | UC81 | CS81 | QN48 | QN68 | VQ100 |
|---|---|---|---|---|---|---|
| Length × Width (mm\mm) | 3 x 3 | 4 x 4 | 5 x 5 | 6 x 6 | 8 x 8 | 14 x 14 |
| Nominal Area (mm$^2$) | 9 | 16 | 25 | 36 | 64 | 196 |
| Pitch (mm) | 0.4 | 0.4 | 0.5 | 0.4 | 0.4 | 0.5 |
| Height (mm) | 0.80 | 0.80 | 0.80 | 0.90 | 0.90 | 1.20 |

# IGLOO nano Device Status

| IGLOO nano Devices | Status | IGLOO nano-Z Devices | Status |
|---|---|---|---|
| AGLN010 | Production | | |
| AGLN015 | Not recommended for new designs. | | |
| AGLN020 | Production | | |
| | | AGLN030Z | Not recommended for new designs. |
| AGLN060 | Production | AGLN060Z | Not recommended for new designs. |
| AGLN125 | Production | AGLN125Z | Not recommended for new designs. |
| AGLN250 | Production | AGLN250Z | Not recommended for new designs. |

## Flash Advantages

### Low Power

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

### Security

Nonvolatile, flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO nano devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO nano device provides the best available security for programmable logic designs.

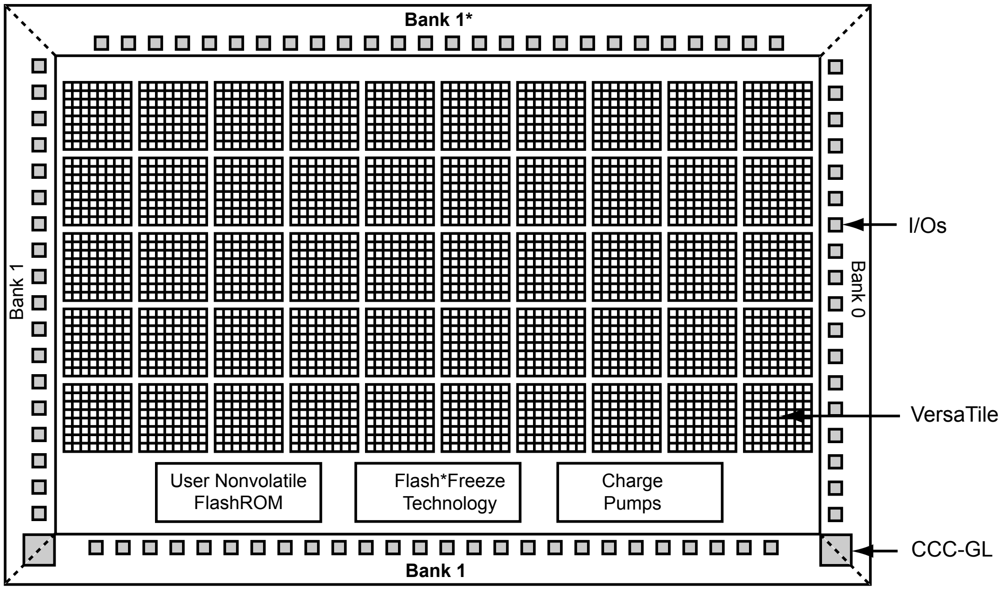
### Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### Instant On

Microsemi flash-based IGLOO nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano flash FPGAs enable the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.



*Note:* **Bank 0 for the AGLN030 device*

***Figure 1-1 •*** **IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030)**

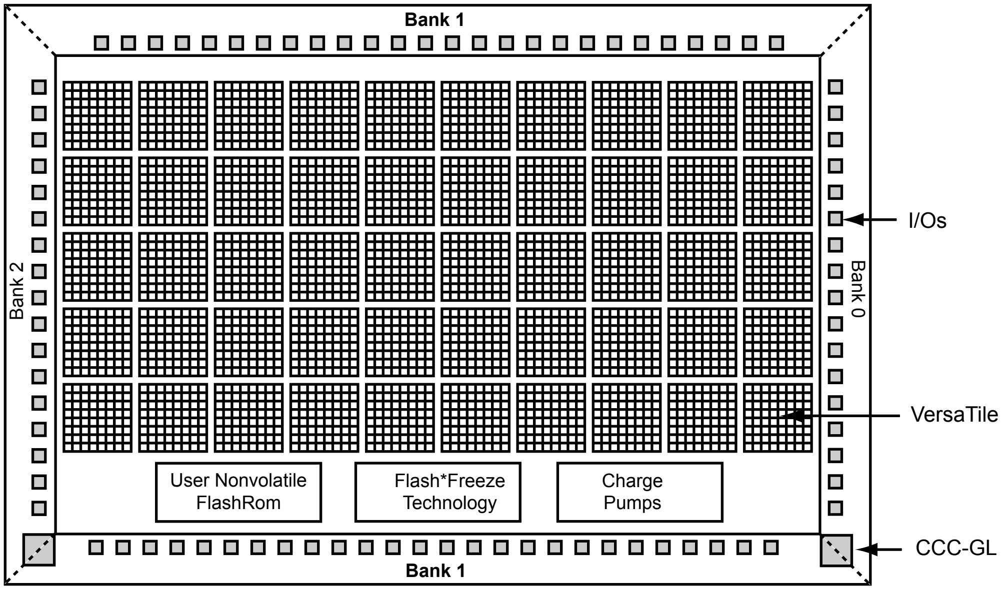


***Figure 1-2 •*** **IGLOO Device Architecture Overview with Three I/O Banks and No RAM (AGLN015 and AGLN020)**

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

# User I/O Characteristics

## Timing Model

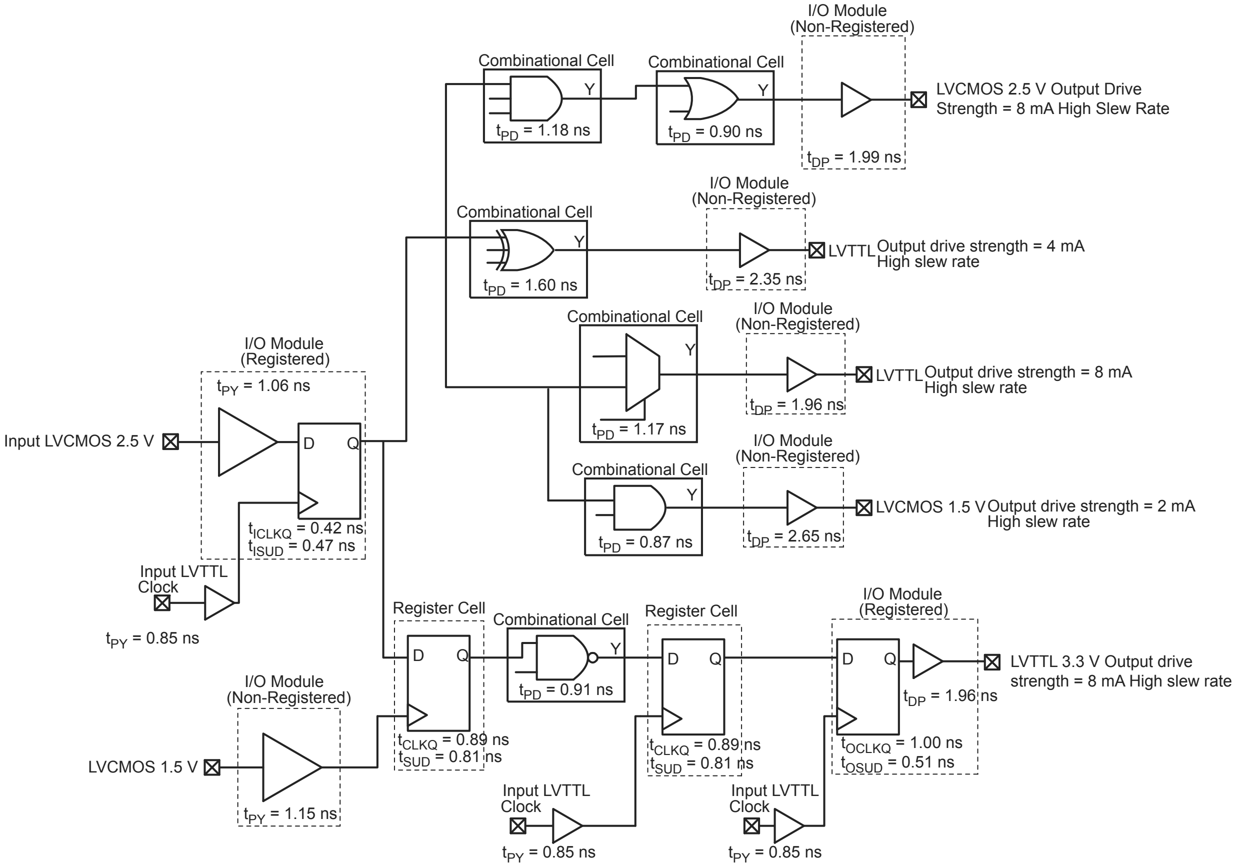


***Figure 2-3 •*** **Timing Model**
**Operating Conditions: STD Speed, Commercial Temperature Range ($T_J$ = 70°C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices**

***Table 2-29 •*** **I/O Weak Pull-Up/Pull-Down Resistances**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCI | $R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω) | | $R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω) | |
|---|---|---|---|---|
| | **Min.** | **Max.** | **Min.** | **Max.** |
| 3.3 V | 10 K | 45 K | 10 K | 45 K |
| 3.3 V (wide range I/Os) | 10 K | 45 K | 10 K | 45 K |
| 2.5 V | 11 K | 55 K | 12 K | 74 K |
| 1.8 V | 18 K | 70 K | 17 K | 110 K |
| 1.5 V | 19 K | 90 K | 19 K | 140 K |
| 1.2 V | 25 K | 110 K | 25 K | 150 K |
| 1.2 V (wide range I/Os) | 19 K | 110 K | 19 K | 150 K |

*Notes:*

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

***Table 2-30 •*** **I/O Short Currents IOSH/IOSL**

| | Drive Strength | IOSL (mA)* | IOSH (mA)* |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as equivalent software default drive | |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| 1.2 V LVCMOS | 1 mA | 10 | 13 |
| 1.2 V LVCMOS Wide Range | 100 µA | 10 | 13 |

*Note:* *$T_J$ = 100°C

### *Timing Characteristics*

#### *Applies to 1.5 V DC Core Voltage*

***Table 2-47 •*** **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 4.13 | 0.19 | 1.10 | 1.24 | 0.66 | 4.01 | 4.13 | 1.73 | 1.74 | ns |
| 4 mA | STD | 0.97 | 4.13 | 0.19 | 1.10 | 1.24 | 0.66 | 4.01 | 4.13 | 1.73 | 1.74 | ns |
| 8 mA | STD | 0.97 | 3.39 | 0.19 | 1.10 | 1.24 | 0.66 | 3.31 | 3.39 | 1.98 | 2.19 | ns |
| 8 mA | STD | 0.97 | 3.39 | 0.19 | 1.10 | 1.24 | 0.66 | 3.31 | 3.39 | 1.98 | 2.19 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-48 •*** **2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.19 | 0.19 | 1.10 | 1.24 | 0.66 | 2.23 | 2.11 | 1.72 | 1.80 | ns |
| 4 mA | STD | 0.97 | 2.19 | 0.19 | 1.10 | 1.24 | 0.66 | 2.23 | 2.11 | 1.72 | 1.80 | ns |
| 6 mA | STD | 0.97 | 1.81 | 0.19 | 1.10 | 1.24 | 0.66 | 1.85 | 1.63 | 1.97 | 2.26 | ns |
| 8 mA | STD | 0.97 | 1.81 | 0.19 | 1.10 | 1.24 | 0.66 | 1.85 | 1.63 | 1.97 | 2.26 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Applies to 1.2 V DC Core Voltage***

**Table 2-49 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 4.61 | 0.26 | 1.21 | 1.39 | 1.10 | 4.55 | 4.61 | 2.15 | 2.43 | ns |
| 4 mA | STD | 1.55 | 4.61 | 0.26 | 1.21 | 1.39 | 1.10 | 4.55 | 4.61 | 2.15 | 2.43 | ns |
| 6 mA | STD | 1.55 | 3.86 | 0.26 | 1.21 | 1.39 | 1.10 | 3.82 | 3.86 | 2.41 | 2.89 | ns |
| 8 mA | STD | 1.55 | 3.86 | 0.26 | 1.21 | 1.39 | 1.10 | 3.82 | 3.86 | 2.41 | 2.89 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-50 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 2.68 | 0.26 | 1.21 | 1.39 | 1.10 | 2.72 | 2.54 | 2.15 | 2.51 | ns |
| 4 mA | STD | 1.55 | 2.68 | 0.26 | 1.21 | 1.39 | 1.10 | 2.72 | 2.54 | 2.15 | 2.51 | ns |
| 6 mA | STD | 1.55 | 2.30 | 0.26 | 1.21 | 1.39 | 1.10 | 2.33 | 2.04 | 2.41 | 2.99 | ns |
| 8 mA | STD | 1.55 | 2.30 | 0.26 | 1.21 | 1.39 | 1.10 | 2.33 | 2.04 | 2.41 | 2.99 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

***Table 2-63 •*** **Minimum and Maximum DC Input and Output Levels**

| 1.2 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL [1] | IIH [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min. V** | **Max. V** | **Min. V** | **Max. V** | **Max. V** | **Min. V** | **mA** | **mA** | **Max. mA[3]** | **Max. mA[3]** | **μA[4]** | **μA[4]** |
| 1 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 1 | 1 | 10 | 13 | 10 | 10 |

*Notes:*

1. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
2. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

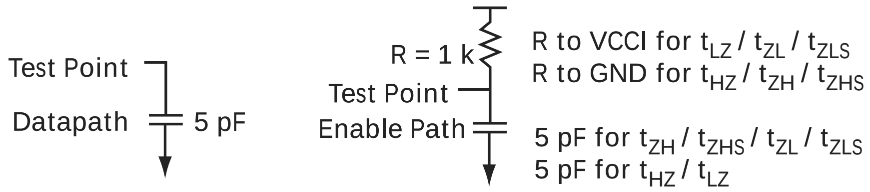


***Figure 2-11 •*** **AC Loading**

***Table 2-64 •*** **1.2 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads**

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.2 | 0.6 | 5 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.

### Timing Characteristics

#### Applies to 1.2 V DC Core Voltage

***Table 2-65 •*** **1.2 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | STD | 1.55 | 8.30 | 0.26 | 1.56 | 2.27 | 1.10 | 7.97 | 7.54 | 2.56 | 2.55 | ns |

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-66 •*** **1.2 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | STD | 1.55 | 3.50 | 0.26 | 1.56 | 2.27 | 1.10 | 3.37 | 3.10 | 2.55 | 2.66 | ns |

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-77 • Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 1.10 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 1.15 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Enable Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## DDR Module Specifications

Note: DDR is not supported for AGLN010, AGLN015, and AGLN020 devices.

### *Input DDR Module*

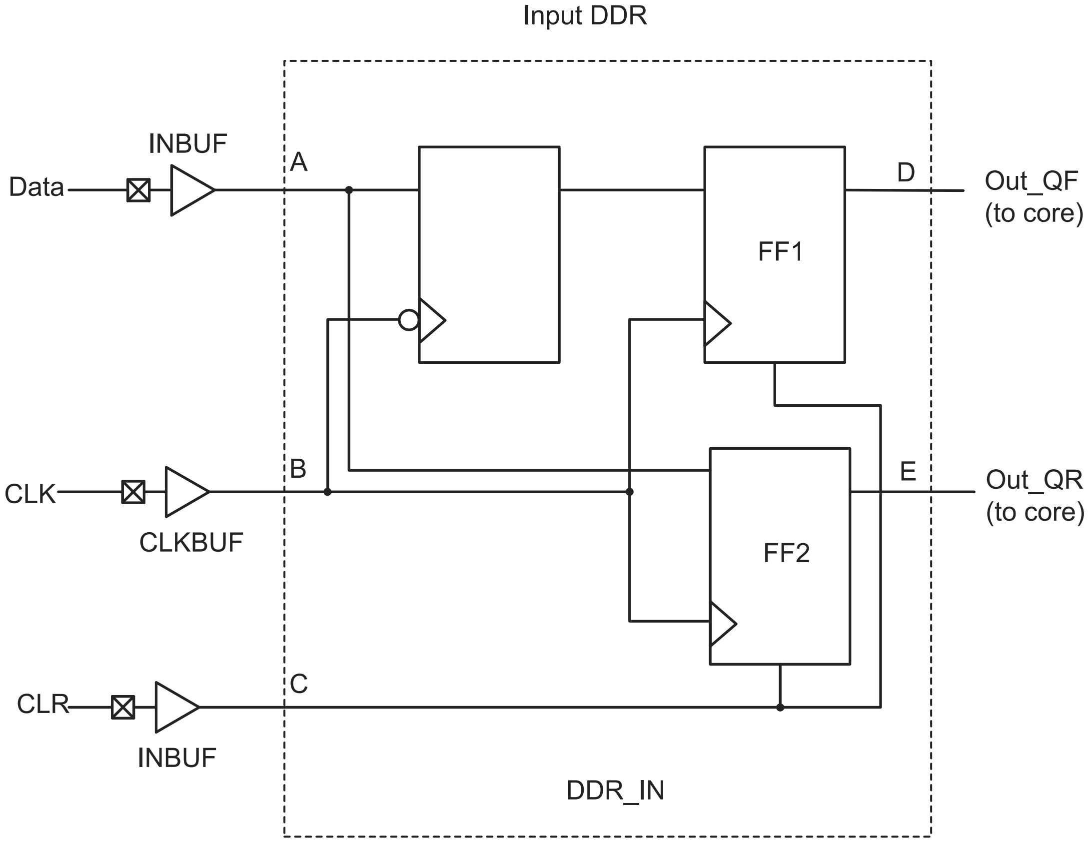


***Figure 2-17 •*** **Input DDR Timing Model**

***Table 2-78 •*** **Parameter Definitions**

| **Parameter Name** | **Parameter Definition** | **Measuring Nodes (from, to)** |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

## Output DDR Module

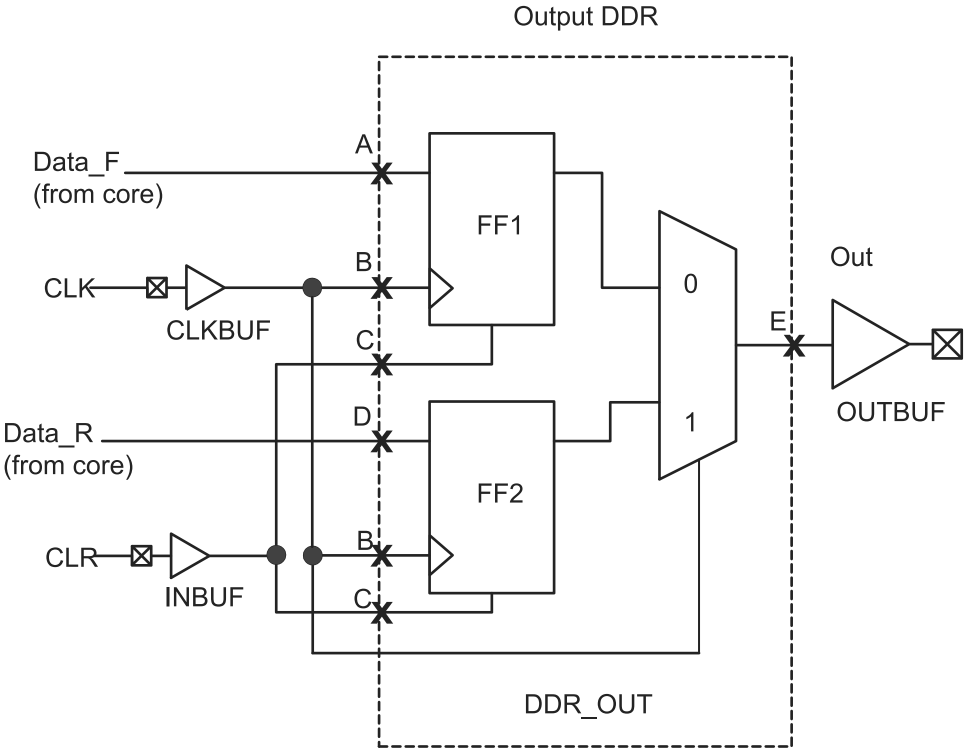


***Figure 2-19* • Output DDR Timing Model**

***Table 2-81* • Parameter Definitions**

| **Parameter Name** | **Parameter Definition** | **Measuring Nodes (from, to)** |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

### *1.2 V DC Core Voltage*

***Table 2-83 •*** **Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.60 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 1.09 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 1.16 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.99 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.24 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 160.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

### 1.2 V DC Core Voltage

*Table 2-87 •* **Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 1.61 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 1.17 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 1.29 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.87 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.89 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.24 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width HIGH for the Core Register | 0.95 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width LOW for the Core Register | 0.95 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Timing Waveforms

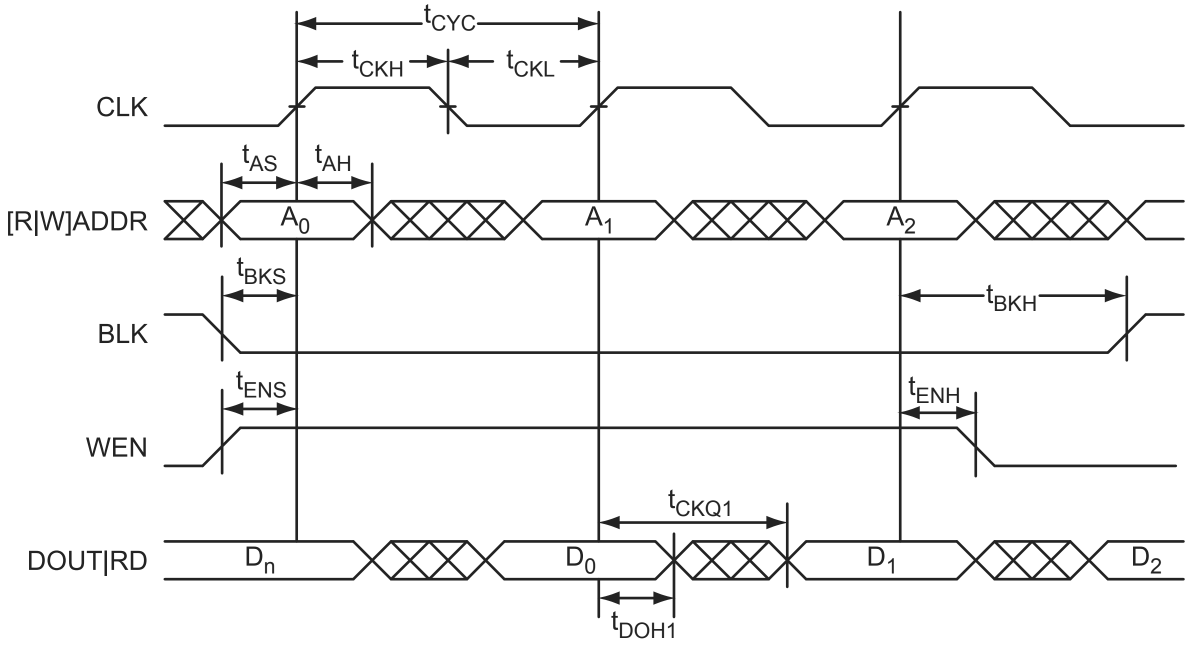


*Figure 2-28* • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

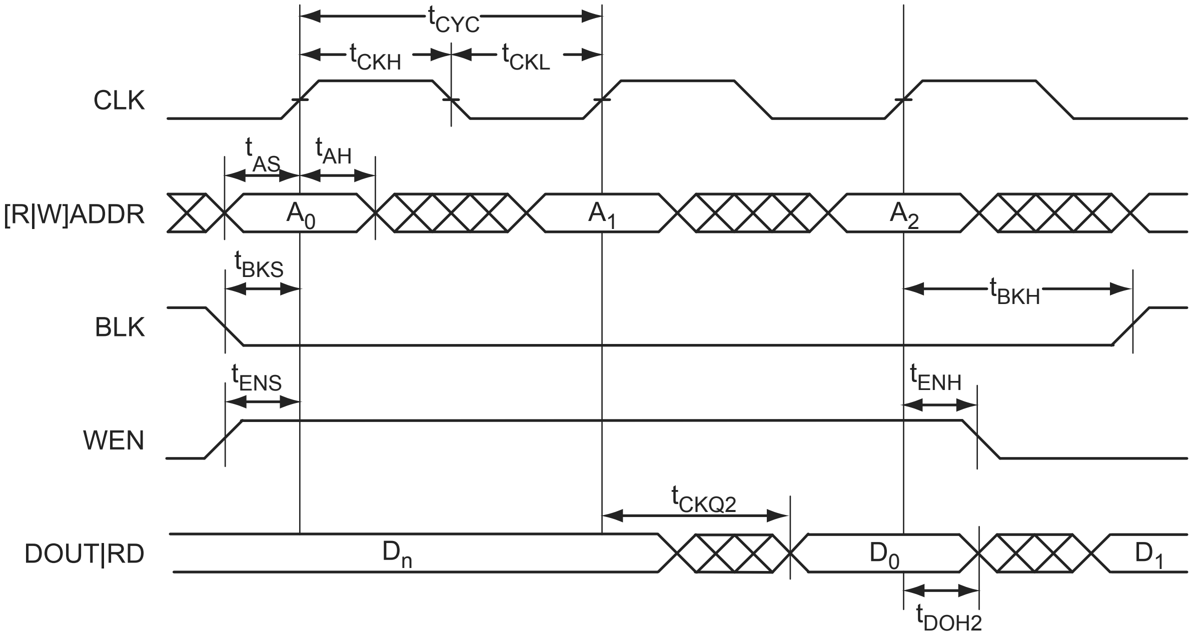


*Figure 2-29* • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

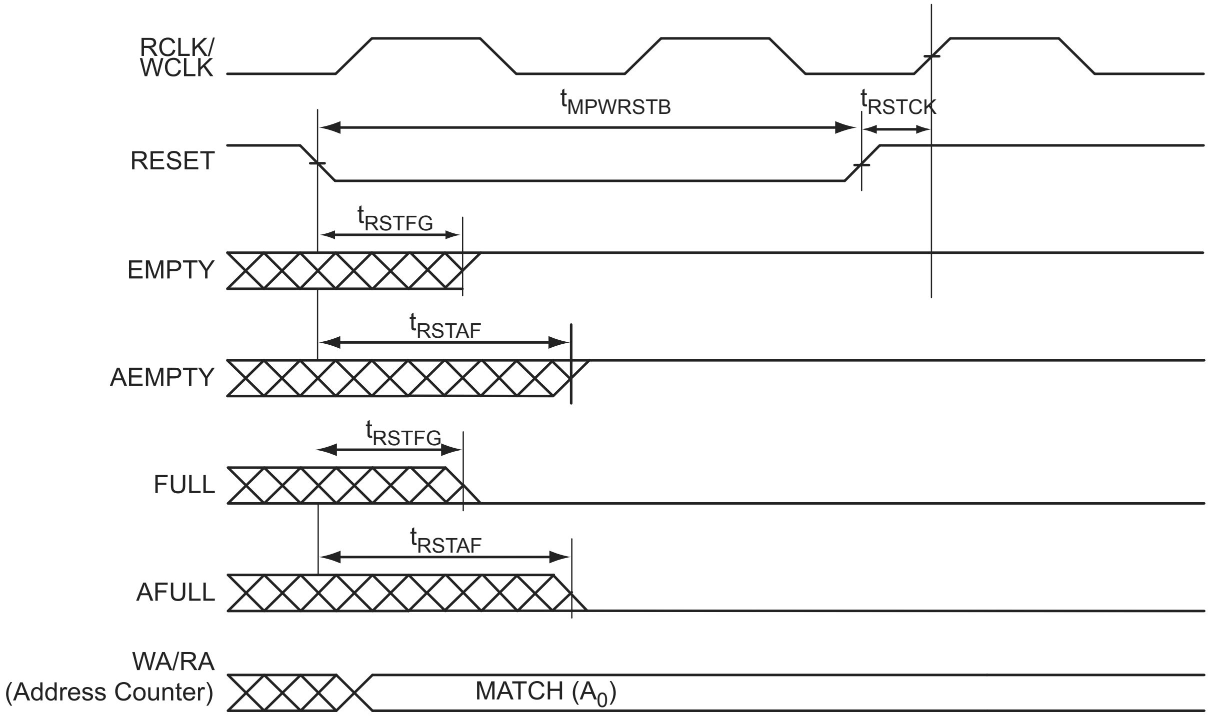


***Figure 2-36* • FIFO Reset**

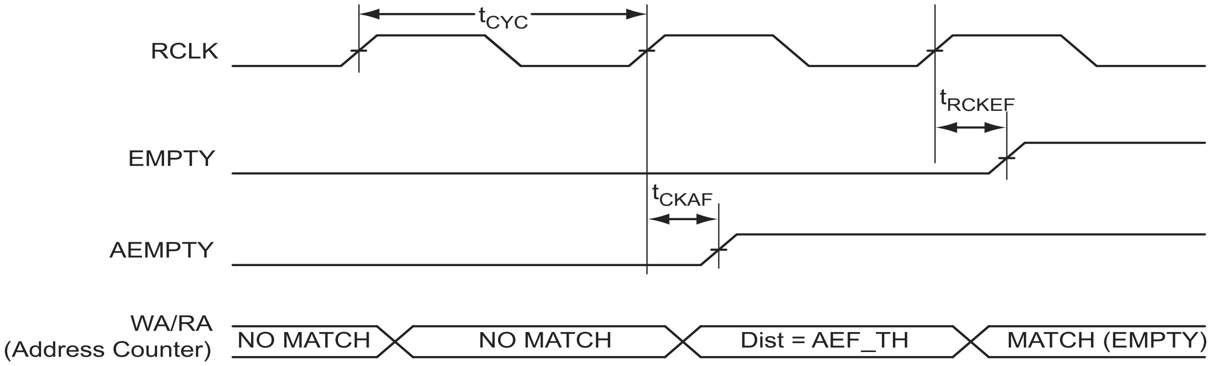


***Figure 2-37* • FIFO EMPTY Flag and AEMPTY Flag Assertion**

interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

### VPUMP Programming Supply Voltage

IGLOO nano devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## User Pins

### I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter in the *IGLOO nano FPGA Fabric User's Guide.* All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in nano Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for an explanation of the naming of global pins.

### FF Flash*Freeze Mode Activation Pin

Flash*Freeze is available on IGLOO nano devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin

| VQ100 | |
|---|---|
| Pin Number | AGLN030Z Function |
| 1 | GND |
| 2 | IO82RSB1 |
| 3 | IO81RSB1 |
| 4 | IO80RSB1 |
| 5 | IO79RSB1 |
| 6 | IO78RSB1 |
| 7 | IO77RSB1 |
| 8 | IO76RSB1 |
| 9 | GND |
| 10 | IO75RSB1 |
| 11 | IO74RSB1 |
| 12 | GEC0/IO73RSB1 |
| 13 | GEA0/IO72RSB1 |
| 14 | GEB0/IO71RSB1 |
| 15 | IO70RSB1 |
| 16 | IO69RSB1 |
| 17 | VCC |
| 18 | VCCIB1 |
| 19 | IO68RSB1 |
| 20 | IO67RSB1 |
| 21 | IO66RSB1 |
| 22 | IO65RSB1 |
| 23 | IO64RSB1 |
| 24 | IO63RSB1 |
| 25 | IO62RSB1 |
| 26 | IO61RSB1 |
| 27 | FF/IO60RSB1 |
| 28 | IO59RSB1 |
| 29 | IO58RSB1 |
| 30 | IO57RSB1 |
| 31 | IO56RSB1 |
| 32 | IO55RSB1 |
| 33 | IO54RSB1 |
| 34 | IO53RSB1 |
| 35 | IO52RSB1 |
| 36 | IO51RSB1 |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB1 |
| 40 | IO49RSB1 |
| 41 | IO47RSB1 |
| 42 | IO46RSB1 |
| 43 | IO45RSB1 |
| 44 | IO44RSB1 |
| 45 | IO43RSB1 |
| 46 | IO42RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | NC |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | IO41RSB0 |
| 58 | IO40RSB0 |
| 59 | IO39RSB0 |
| 60 | IO38RSB0 |
| 61 | IO37RSB0 |
| 62 | IO36RSB0 |
| 63 | GDB0/IO34RSB0 |
| 64 | GDA0/IO33RSB0 |
| 65 | GDC0/IO32RSB0 |
| 66 | VCCIB0 |
| 67 | GND |
| 68 | VCC |
| 69 | IO31RSB0 |
| 70 | IO30RSB0 |
| 71 | IO29RSB0 |
| 72 | IO28RSB0 |
| 73 | IO27RSB0 |
| 74 | IO26RSB0 |
| 75 | IO25RSB0 |
| 76 | IO24RSB0 |
| 77 | IO23RSB0 |
| 78 | IO22RSB0 |
| 79 | IO21RSB0 |
| 80 | IO20RSB0 |
| 81 | IO19RSB0 |
| 82 | IO18RSB0 |
| 83 | IO17RSB0 |
| 84 | IO16RSB0 |
| 85 | IO15RSB0 |
| 86 | IO14RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO12RSB0 |
| 91 | IO10RSB0 |
| 92 | IO08RSB0 |
| 93 | IO07RSB0 |
| 94 | IO06RSB0 |
| 95 | IO05RSB0 |
| 96 | IO04RSB0 |
| 97 | IO03RSB0 |
| 98 | IO02RSB0 |
| 99 | IO01RSB0 |
| 100 | IO00RSB0 |

| Revision / Version | Changes | Page |
|---|---|---|
| **Revision 1 (cont'd)**<br>Packaging Advance v0.2 | The "QN48" pin diagram was revised. | 4-16 |
| | Note 2 for the "QN48", "QN68", and "100-Pin QFN" pin diagrams was changed to "The die attach paddle of the package is tied to ground (GND)." | 4-16, 4-19 |
| | The "VQ100" pin diagram was revised to move the pin IDs to the upper left corner instead of the upper right corner. | 4-23 |
| **Revision 0 (Oct 2008)**<br>Product Brief Advance v0.2 | The following tables and sections were updated to add the UC81 and CS81 packages for AGL030:<br>"IGLOO nano Devices"<br>"I/Os Per Package"<br>"IGLOO nano Products Available in the Z Feature Grade"<br>"Temperature Grade Offerings" | N/A |
| | The "I/Os Per Package" table was updated to add the following information to table note 4: "For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only." | II |
| | The "IGLOO nano Products Available in the Z Feature Grade" section was updated to remove QN100 for AGLN250. | VI |
| | The device architecture figures, Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125) through Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250), were revised. Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030) is new. | 1-4 through 1-5 |
| | The "PLL and CCC" section was revised to include information about CCC-GLs in AGLN020 and smaller devices. | 1-7 |
| | The "I/Os with Advanced I/O Standards" section was revised to add information about IGLOO nano devices supporting double-data-rate applications. | 1-8 |