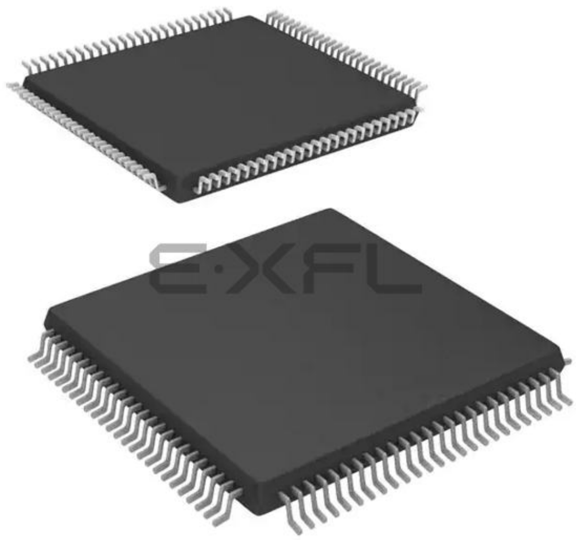

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6144 |
| Total RAM Bits | 36864 |
| Number of I/O | 68 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -20°C ~ 85°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agln250v2-vq100 |

# IGLOO nano Products Available in the Z Feature Grade

| IGLOO nano-Z Devices | AGLN030Z* | AGLN060Z* | AGLN125Z* | AGLN250Z* |
|---|---|---|---|---|
| Packages | QN48 | – | – | – |
| | QN68 | – | – | – |
| | UC81 | – | – | – |
| | CS81 | CS81 | CS81 | CS81 |
| | VQ100 | VQ100 | VQ100 | VQ100 |

*Note: *Not recommended for new designs.*

# Temperature Grade Offerings

| Package | AGLN010 | AGLN015* | AGLN020 | | AGLN060 | AGLN125 | AGLN250 |
|---|---|---|---|---|---|---|---|
| | | | | AGLN030Z* | AGLN060Z* | AGLN125Z* | AGLN250Z* |
| UC36 | C, I | – | – | – | – | – | – |
| QN48 | C, I | – | – | C, I | – | – | – |
| QN68 | – | C, I | C, I | C, I | – | – | – |
| UC81 | – | – | C, I | C, I | – | – | – |
| CS81 | – | – | C, I | C, I | C, I | C, I | C, I |
| VQ100 | – | – | – | C, I | C, I | C, I | C, I |

*Note: * Not recommended for new designs.*

*C = Enhanced Commercial temperature range: –20°C to +85°C junction temperature*
*I = Industrial temperature range: –40°C to +100°C junction temperature*

Contact your local Microsemi representative for device availability: http://www.microsemi.com/soc/contact/default.aspx.

# Table of Contents

# 1 – IGLOO nano Device Overview

## General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO nano devices enables entering and exiting an ultra-low power mode that consumes nanoPower while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO nano device is completely functional in the system. This allows the IGLOO nano device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO nano devices the advantage of being a secure, low power, single-chip solution that is Instant On. The IGLOO nano device is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGLN030 and smaller devices have no PLL or RAM support. IGLOO nano devices have up to 250 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

IGLOO nano devices increase the breadth of the IGLOO product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Features such as smaller footprint packages designed with two-layer PCBs in mind, power consumption measured in nanoPower, Schmitt trigger, and bus hold (hold previous I/O state in Flash*Freeze mode) functionality make these devices ideal for deployment in applications that require high levels of flexibility and low cost.

### Flash*Freeze Technology

The IGLOO nano device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO nano devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO nano V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, HIGH, or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and small-footprint packages make IGLOO nano devices the best fit for portable electronics.

## Flash*Freeze Technology

The IGLOO nano device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode.

Alternatively, I/Os can be set to a specific state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 2 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-5 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

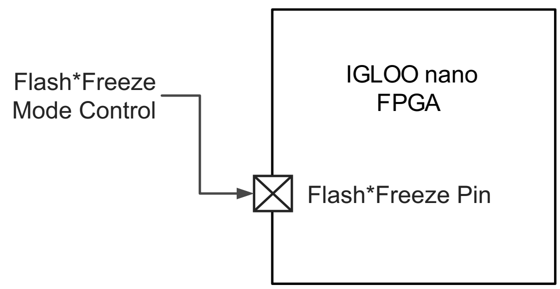



***Figure 1-5 •*** **IGLOO nano Flash*Freeze Mode**

## VersaTiles

The IGLOO nano core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{\text{PLUS}®}$ core tiles. The IGLOO nano VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-6 for VersaTile configurations.

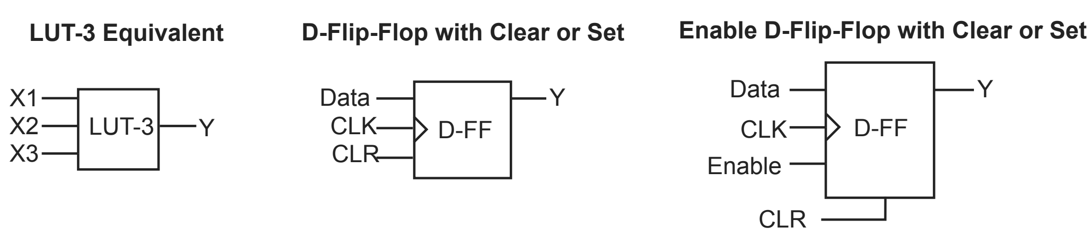



***Figure 1-6 •*** **VersaTile Configurations**

## Power per I/O Pin

**Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to IGLOO nano I/O Banks**

| | VCCI (V) | Dynamic Power PAC9 (µW/MHz) [1] |
|---|---|---|
| **Single-Ended** | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | 16.38 |
| 3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger | 3.3 | 18.89 |
| 3.3 V LVCMOS Wide Range[2] | 3.3 | 16.38 |
| 3.3 V LVCMOS Wide Range – Schmitt Trigger | 3.3 | 18.89 |
| 2.5 V LVCMOS | 2.5 | 4.71 |
| 2.5 V LVCMOS – Schmitt Trigger | 2.5 | 6.13 |
| 1.8 V LVCMOS | 1.8 | 1.64 |
| 1.8 V LVCMOS – Schmitt Trigger | 1.8 | 1.79 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | 0.97 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt Trigger | 1.5 | 0.96 |
| 1.2 V LVCMOS[3] | 1.2 | 0.57 |
| 1.2 V LVCMOS – Schmitt Trigger[3] | 1.2 | 0.52 |
| 1.2 V LVCMOS Wide Range[3] | 1.2 | 0.57 |
| 1.2 V LVCMOS Wide Range – Schmitt Trigger[3] | 1.2 | 0.52 |

*Notes:*

1. *PAC9 is the total dynamic power measured on $V_{CCI}$.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*

**Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to IGLOO nano I/O Banks**

| | $C_{LOAD}$ (pF) | VCCI (V) | Dynamic Power PAC10 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 5 | 3.3 | 107.98 |
| 3.3 V LVCMOS Wide Range[3] | 5 | 3.3 | 107.98 |
| 2.5 V LVCMOS | 5 | 2.5 | 61.24 |
| 1.8 V LVCMOS | 5 | 1.8 | 31.28 |
| 1.5 V LVCMOS (JESD8-11) | 5 | 1.5 | 21.50 |
| 1.2 V LVCMOS[4] | 5 | 1.2 | 15.22 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
4. *Applicable for IGLOO nano V2 devices operating at VCCI ≥ VCC.*

## Overview of I/O Performance

### *Summary of I/O DC Input and Output Levels – Default I/O Software Settings*

***Table 2-21 •*** **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength[2] | Slew Rate | VIL Min. V | VIL Max. V | VIH Min. V | VIH Max. V | VOL Max. V | VOH Min. V | IOL[1] mA | IOH[1] mA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 8 mA | 8 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 |
| 3.3 V LVCMOS Wide Range[3] | 100 µA | 8 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 100 µA | 100 µA |
| 2.5 V LVCMOS | 8 mA | 8 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 |
| 1.8 V LVCMOS | 4 mA | 4 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 4 | 4 |
| 1.5 V LVCMOS | 2 mA | 2 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 |
| 1.2 V LVCMOS[4] | 1 mA | 1 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 1 | 1 |
| 1.2 V LVCMOS Wide Range[4,5] | 100 µA | 1 mA | High | –0.3 | 0.3 * VCCI | 0.7 * VCCI | 3.6 | 0.1 | VCCI – 0.1 | 100 µA | 100 µA |

*Notes:*

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
4. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range, as specified in the JESD8-12 specification.*

***Table 2-22 •*** **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

| DC I/O Standards | Commercial[1] IIL[3] µA | Commercial[1] IIH[4] µA | Industrial[2] IIL[3] µA | Industrial[2] IIH[4] µA |
|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V LVCOMS Wide Range | 10 | 10 | 15 | 15 |
| 2.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS[5] | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS Wide Range[5] | 10 | 10 | 15 | 15 |

*Notes:*

1. *Commercial range (–20°C < $T_A$ < 70°C)*
2. *Industrial range (–40°C < $T_A$ < 85°C)*
3. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions, where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions, where –0.3 V < VIN < VIL.*
5. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*

### 3.3 V LVCMOS Wide Range

**Table 2-40 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range**

| 3.3 V LVCMOS Wide Range[1] | Equivalent Software Default Drive Strength Option[4] | VIL | | VIH | | VOL | VOH | IOL | $I_{OH}$ | IIL [2] | IIH [3] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 100 | 100 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 100 | 100 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 100 | 100 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 100 | 100 | 10 | 10 |

*Notes:*

1. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V Wide Range, as specified in the JEDEC JESD8-B specification.*
2. *$I_{IL}$ is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.*
3. *$I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection is highlighted in gray.*

***Applies to 1.2 V DC Core Voltage***

**Table 2-43 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | STD | 1.55 | 6.01 | 0.26 | 1.31 | 1.91 | 1.10 | 6.01 | 5.66 | 3.02 | 3.49 | ns |
| 100 µA | 4 mA | STD | 1.55 | 6.01 | 0.26 | 1.31 | 1.91 | 1.10 | 6.01 | 5.66 | 3.02 | 3.49 | ns |
| 100 µA | 6 mA | STD | 1.55 | 5.02 | 0.26 | 1.31 | 1.91 | 1.10 | 5.02 | 4.76 | 3.38 | 4.10 | ns |
| 100 µA | 8 mA | STD | 1.55 | 5.02 | 0.26 | 1.31 | 1.91 | 1.10 | 5.02 | 4.76 | 3.38 | 4.10 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-44 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | STD | 1.55 | 3.82 | 0.26 | 1.31 | 1.91 | 1.10 | 3.82 | 3.15 | 3.01 | 3.65 | ns |
| 100 µA | 4 mA | STD | 1.55 | 3.82 | 0.26 | 1.31 | 1.91 | 1.10 | 3.82 | 3.15 | 3.01 | 3.65 | ns |
| 100 µA | 6 mA | STD | 1.55 | 3.25 | 0.26 | 1.31 | 1.91 | 1.10 | 3.25 | 2.61 | 3.38 | 4.27 | ns |
| 100 µA | 8 mA | STD | 1.55 | 3.25 | 0.26 | 1.31 | 1.91 | 1.10 | 3.25 | 2.61 | 3.38 | 4.27 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

# I/O Register Specifications

## *Fully Registered I/O Buffers with Asynchronous Preset*

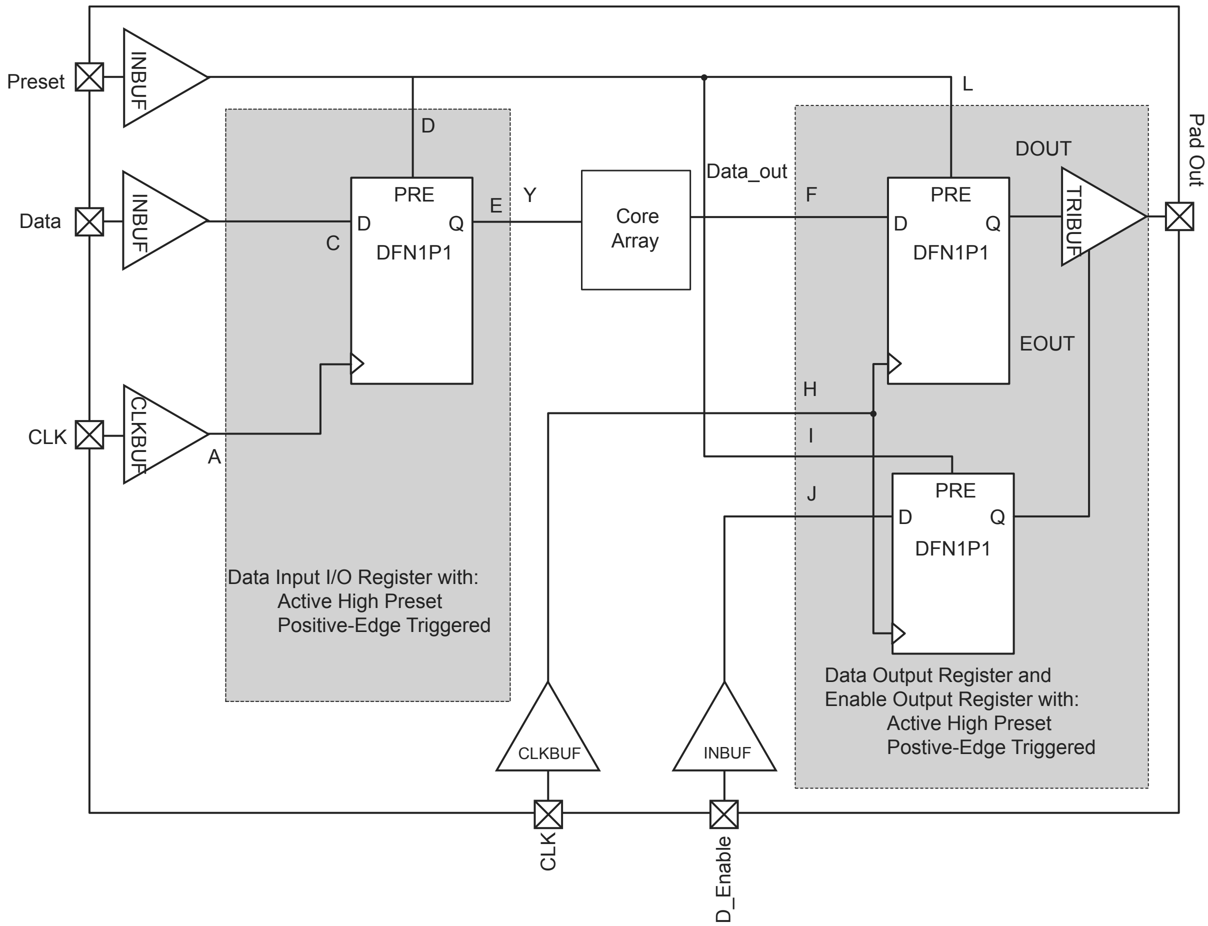



***Figure 2-12 •* Timing Model of Registered I/O Buffers with Asynchronous Preset**

## Input Register

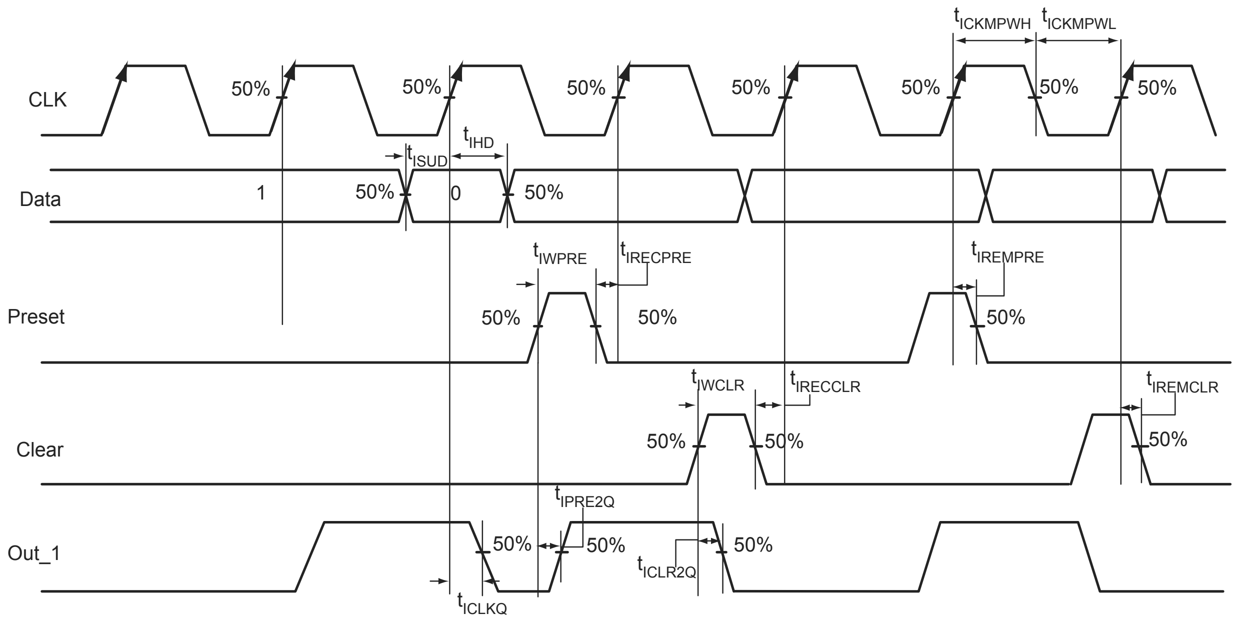



***Figure 2-14 •*** **Input Register Timing Diagram**

### *Timing Characteristics*

#### *1.5 V DC Core Voltage*

***Table 2-72 •*** **Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.42 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.47 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width HIGH for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width LOW for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## DDR Module Specifications

Note: DDR is not supported for AGLN010, AGLN015, and AGLN020 devices.

### *Input DDR Module*

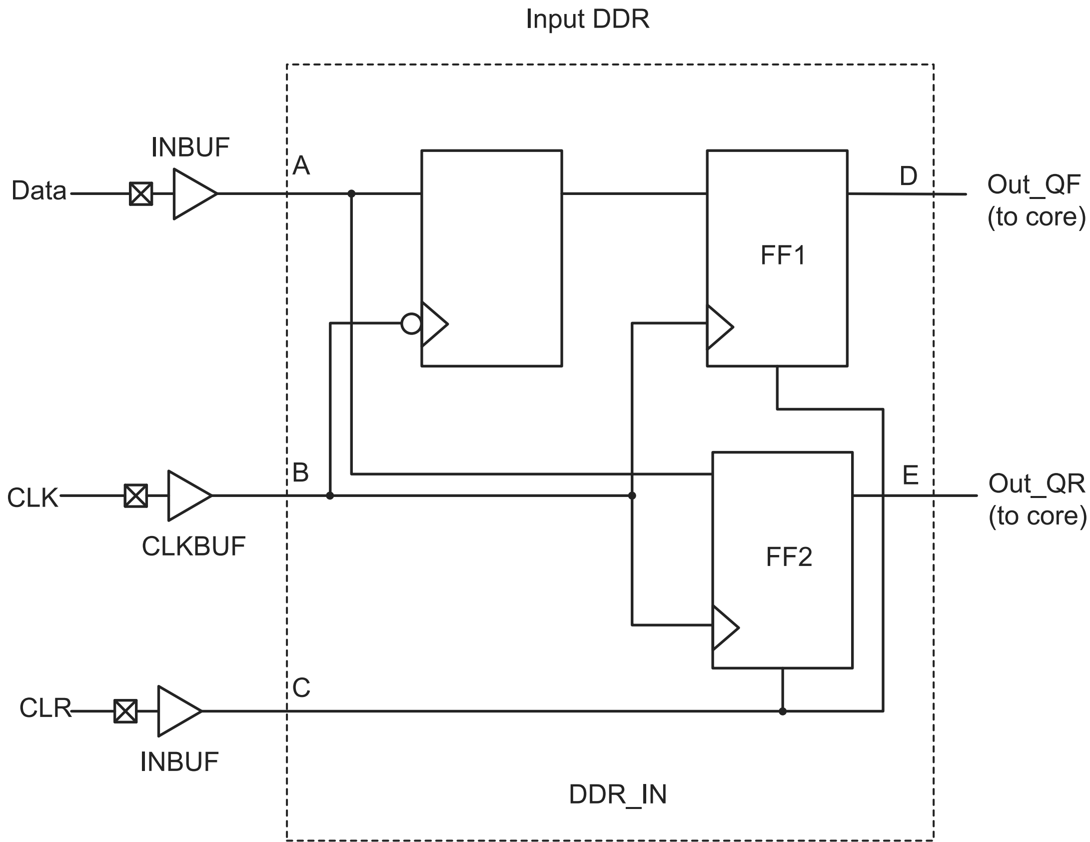



***Figure 2-17 •*** **Input DDR Timing Model**

***Table 2-78 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-84 • Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.76 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.87 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.91 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.90 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.94 | ns |
| XOR2 | Y = A $\oplus$ B | $t_{PD}$ | 1.39 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 1.44 | ns |
| XOR3 | Y = A $\oplus$ B $\oplus$ C | $t_{PD}$ | 1.60 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 1.17 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 1.18 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-85 • Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 1.33 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 1.48 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 1.58 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 1.53 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 1.63 | ns |
| XOR2 | Y = A $\oplus$ B | $t_{PD}$ | 2.34 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 2.59 | ns |
| XOR3 | Y = A $\oplus$ B $\oplus$ C | $t_{PD}$ | 2.74 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 2.03 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 2.11 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

# Global Resource Characteristics

## AGLN125 Clock Tree Topology

Clock delays are device-specific. Figure 2-25 is an example of a global tree used for clock routing. The global tree presented in Figure 2-25 is driven by a CCC located on the west side of the AGLN125 device. It is used to drive all D-flip-flops in the device.

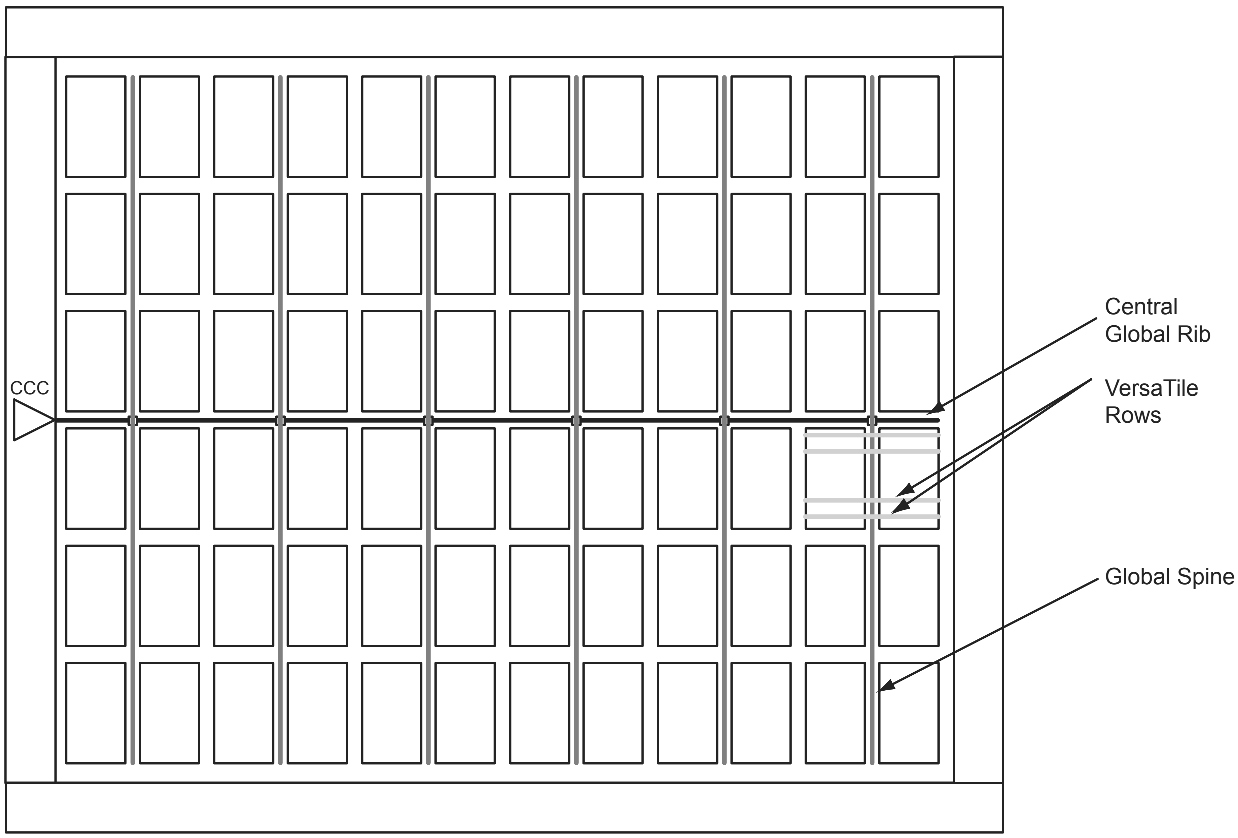



***Figure 2-25*** **• Example of Global Tree Use in an AGLN125 Device for Clock Routing**

**Table 2-92 • AGLN125 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.36 | 1.71 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.39 | 1.82 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.43 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-93 • AGLN250 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.39 | 1.73 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.41 | 1.84 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.43 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

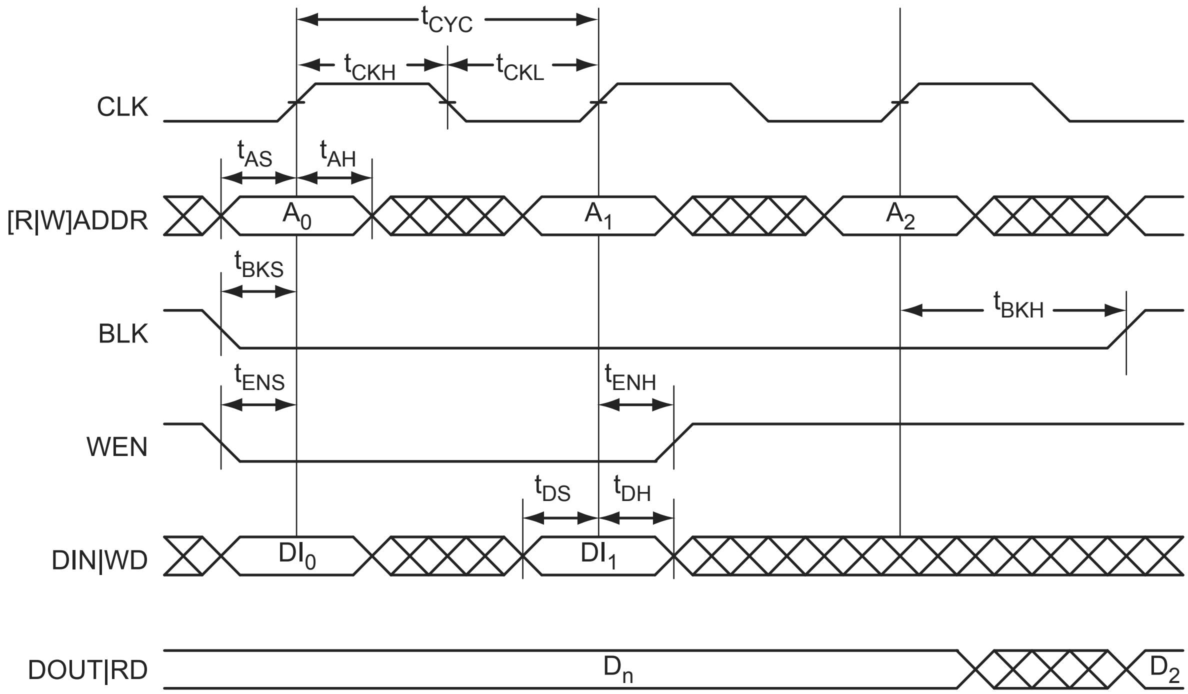



***Figure 2-30*** **• RAM Write, Output Retained (WMODE = 0). Applicable to Both RAM4K9 and RAM512x18.**

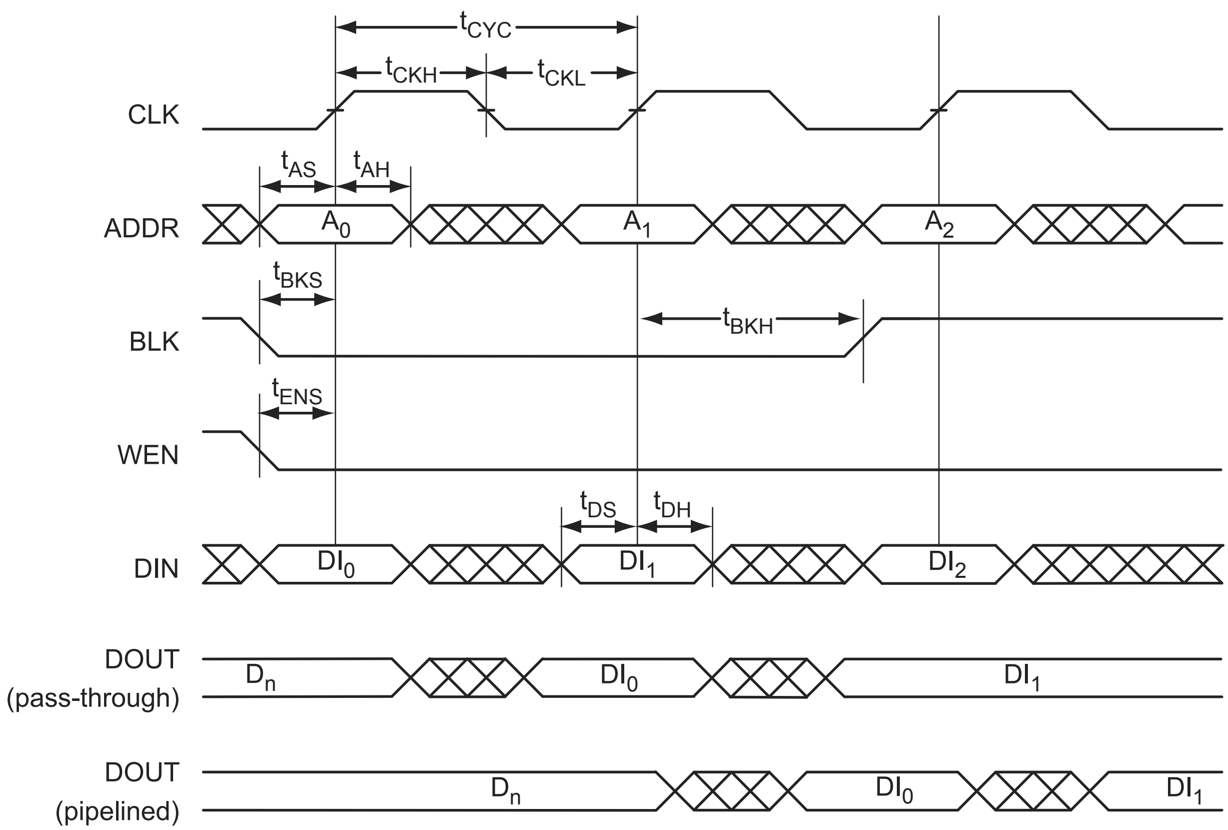



***Figure 2-31*** **• RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO nano devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO nano devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO nano FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

***Table 3-1*** **• Flash*Freeze Pin Locations for IGLOO nano Devices**

| Package | Flash*Freeze Pin |
|---|---|
| CS81/UC81 | H2 |
| QN48 | 14 |
| QN68 | 18 |
| VQ100 | 27 |
| UC36 | E2 |

# JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

### TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

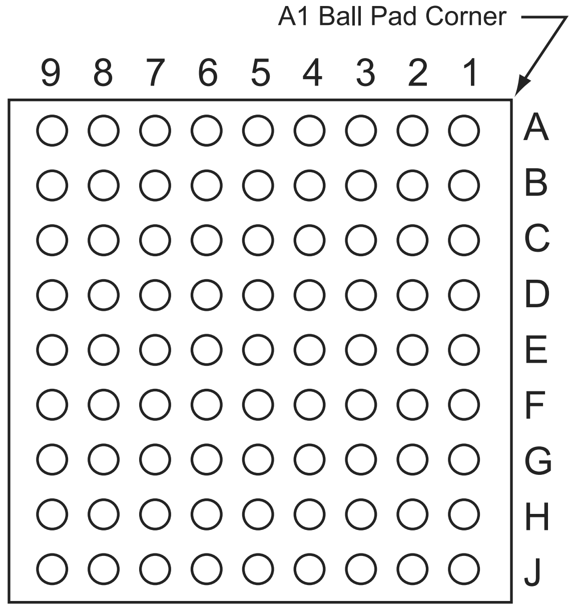
***Table 3-2*** **• Recommended Tie-Off Values for the TCK and TRST Pins**

| VJTAG | Tie-Off Resistance [1,2] |
|---|---|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

*Notes:*

1. *The TCK pin can be pulled-up or pulled-down.*
2. *The TRST pin is pulled-down.*
3. *Equivalent parallel resistance if more than one device is on the JTAG chain*

# UC81




*Note: This is the bottom view of the package.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| QN68 | |
|---|---|
| Pin Number | AGLN020 Function |
| 1 | IO60RSB2 |
| 2 | IO54RSB2 |
| 3 | IO52RSB2 |
| 4 | IO50RSB2 |
| 5 | IO49RSB2 |
| 6 | GEC0/IO48RSB2 |
| 7 | GEA0/IO47RSB2 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCIB2 |
| 11 | IO46RSB2 |
| 12 | IO45RSB2 |
| 13 | IO44RSB2 |
| 14 | IO43RSB2 |
| 15 | IO42RSB2 |
| 16 | IO41RSB2 |
| 17 | IO40RSB2 |
| 18 | FF/IO39RSB1 |
| 19 | IO37RSB1 |
| 20 | IO35RSB1 |
| 21 | IO33RSB1 |
| 22 | IO31RSB1 |
| 23 | IO30RSB1 |
| 24 | VCC |
| 25 | GND |
| 26 | VCCIB1 |
| 27 | IO27RSB1 |
| 28 | IO25RSB1 |
| 29 | IO23RSB1 |
| 30 | IO21RSB1 |
| 31 | IO19RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | VPUMP |

| QN68 | |
|---|---|
| Pin Number | AGLN020 Function |
| 36 | TDO |
| 37 | TRST |
| 38 | VJTAG |
| 39 | IO17RSB0 |
| 40 | IO16RSB0 |
| 41 | GDA0/IO15RSB0 |
| 42 | GDC0/IO14RSB0 |
| 43 | IO13RSB0 |
| 44 | VCCIB0 |
| 45 | GND |
| 46 | VCC |
| 47 | IO12RSB0 |
| 48 | IO11RSB0 |
| 49 | IO09RSB0 |
| 50 | IO05RSB0 |
| 51 | IO00RSB0 |
| 52 | IO07RSB0 |
| 53 | IO03RSB0 |
| 54 | IO18RSB1 |
| 55 | IO20RSB1 |
| 56 | IO22RSB1 |
| 57 | IO24RSB1 |
| 58 | IO28RSB1 |
| 59 | NC |
| 60 | GND |
| 61 | NC |
| 62 | IO32RSB1 |
| 63 | IO34RSB1 |
| 64 | IO36RSB1 |
| 65 | IO61RSB2 |
| 66 | IO58RSB2 |
| 67 | IO56RSB2 |
| 68 | IO63RSB2 |

| VQ100 | |
|---|---|
| Pin Number | AGLN125Z Function |
| 1 | GND |
| 2 | GAA2/IO67RSB1 |
| 3 | IO68RSB1 |
| 4 | GAB2/IO69RSB1 |
| 5 | IO132RSB1 |
| 6 | GAC2/IO131RSB1 |
| 7 | IO130RSB1 |
| 8 | IO129RSB1 |
| 9 | GND |
| 10 | GFB1/IO124RSB1 |
| 11 | GFB0/IO123RSB1 |
| 12 | VCOMPLF |
| 13 | GFA0/IO122RSB1 |
| 14 | VCCPLF |
| 15 | GFA1/IO121RSB1 |
| 16 | GFA2/IO120RSB1 |
| 17 | VCC |
| 18 | VCCIB1 |
| 19 | GEC0/IO111RSB1 |
| 20 | GEB1/IO110RSB1 |
| 21 | GEB0/IO109RSB1 |
| 22 | GEA1/IO108RSB1 |
| 23 | GEA0/IO107RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO106RSB1 |
| 27 | FF/GEB2/IO105RSB1 |
| 28 | GEC2/IO104RSB1 |
| 29 | IO102RSB1 |
| 30 | IO100RSB1 |
| 31 | IO99RSB1 |
| 32 | IO97RSB1 |
| 33 | IO96RSB1 |
| 34 | IO95RSB1 |
| 35 | IO94RSB1 |

| VQ100 | |
|---|---|
| Pin Number | AGLN125Z Function |
| 36 | IO93RSB1 |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB1 |
| 40 | IO87RSB1 |
| 41 | IO84RSB1 |
| 42 | IO81RSB1 |
| 43 | IO75RSB1 |
| 44 | GDC2/IO72RSB1 |
| 45 | GDB2/IO71RSB1 |
| 46 | GDA2/IO70RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO65RSB0 |
| 58 | GDC0/IO62RSB0 |
| 59 | GDC1/IO61RSB0 |
| 60 | GCC2/IO59RSB0 |
| 61 | GCB2/IO58RSB0 |
| 62 | GCA0/IO56RSB0 |
| 63 | GCA1/IO55RSB0 |
| 64 | GCC0/IO52RSB0 |
| 65 | GCC1/IO51RSB0 |
| 66 | VCCIB0 |
| 67 | GND |
| 68 | VCC |
| 69 | IO47RSB0 |
| 70 | GBC2/IO45RSB0 |

| VQ100 | |
|---|---|
| Pin Number | AGLN125Z Function |
| 71 | GBB2/IO43RSB0 |
| 72 | IO42RSB0 |
| 73 | GBA2/IO41RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO40RSB0 |
| 77 | GBA0/IO39RSB0 |
| 78 | GBB1/IO38RSB0 |
| 79 | GBB0/IO37RSB0 |
| 80 | GBC1/IO36RSB0 |
| 81 | GBC0/IO35RSB0 |
| 82 | IO32RSB0 |
| 83 | IO28RSB0 |
| 84 | IO25RSB0 |
| 85 | IO22RSB0 |
| 86 | IO19RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO15RSB0 |
| 91 | IO13RSB0 |
| 92 | IO11RSB0 |
| 93 | IO09RSB0 |
| 94 | IO07RSB0 |
| 95 | GAC1/IO05RSB0 |
| 96 | GAC0/IO04RSB0 |
| 97 | GAB1/IO03RSB0 |
| 98 | GAB0/IO02RSB0 |
| 99 | GAA1/IO01RSB0 |
| 100 | GAA0/IO00RSB0 |

| Revision | Changes | Page |
|---|---|---|
| Revision 10 (continued) | The following tables were updated with current available information. The equivalent software default drive strength option was added.<br>Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels<br>Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings<br>Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings<br>Table 2-28 • I/O Output Buffer Maximum Resistances [1]<br>Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances<br>Table 2-30 • I/O Short Currents IOSH/IOSL<br>Timing tables in the "Single-Ended I/O Characteristics" section, including new tables for 3.3 V and 1.2 V LVCMOS wide range.<br>Table 2-40 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range<br>Table 2-63 • Minimum and Maximum DC Input and Output Levels<br>Table 2-67 • Minimum and Maximum DC Input and Output Levels (new) | 2-19 through 2-40 |
| | The formulas in the notes to Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised (SAR 21348). | 2-24 |
| | The text introducing Table 2-31 • Duration of Short Circuit Event before Failure was revised to state six months at 100° instead of three months at 110° for reliability concerns. The row for 110° was removed from the table. | 2-25 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5-V tolerant input buffer and push-pull output buffer." | 2-32 |
| | The $F_{DDRIMAX}$ and $F_{DDOMAX}$ values were added to tables in the "DDR Module Specifications" section (SAR 23919). A note was added stating that DDR is not supported for AGLN010, AGLN015, and AGLN020. | 2-51 |
| | Tables in the "Global Tree Timing Characteristics" section were updated with new information available. | 2-64 |
| | Table 2-100 • IGLOO nano CCC/PLL Specification and Table 2-101 • IGLOO nano CCC/PLL Specification were revised (SAR 79390). | 2-70, 2-71 |
| | Tables in the SRAM "Timing Characteristics" section and FIFO "Timing Characteristics" section were updated with new information available. | 2-77, 2-85 |
| | Table 3-3 • TRST and TCK Pull-Down Recommendations is new. | 3-4 |
| | A note was added to the "CS81" pin tables for AGLN060, AGLN060Z, AGLN125, AGLN125Z, AGLN250, and AGLN250Z indicating that pins F1 and F2 must be grounded (SAR 25007). | 4-9, through 4-14 |
| | A note was added to the "CS81" and "VQ100" pin tables for AGLN060 and AGLN060Z stating that bus hold is not available for pin H7 or pin 45 (SAR 24079). | 4-9, 4-24 |
| | The AGLN250 function for pin C8 in the "CS81" table was revised (SAR 22134). | 4-13 |