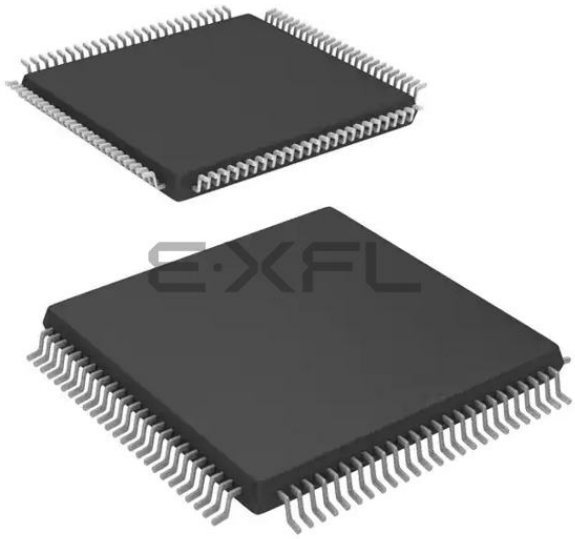

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6144 |
| Total RAM Bits | 36864 |
| Number of I/O | 68 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -20°C ~ 85°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agln250v5-vq100 |

# IGLOO nano Device Status

| IGLOO nano Devices | Status | IGLOO nano-Z Devices | Status |
|---|---|---|---|
| AGLN010 | Production | | |
| AGLN015 | Not recommended for new designs. | | |
| AGLN020 | Production | | |
| | | AGLN030Z | Not recommended for new designs. |
| AGLN060 | Production | AGLN060Z | Not recommended for new designs. |
| AGLN125 | Production | AGLN125Z | Not recommended for new designs. |
| AGLN250 | Production | AGLN250Z | Not recommended for new designs. |

## User Nonvolatile FlashROM

IGLOO nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGLN030 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO nano development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Microsemi Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## SRAM and FIFO

IGLOO nano devices (except the AGLN030 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGLN030 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## PLL and CCC

Higher density IGLOO nano devices using either the two I/O bank or four I/O bank architectures provide designers with very flexible clock conditioning capabilities. AGLN060, AGLN125, and AGLN250 contain six CCCs. One CCC (center west side) has a PLL. The AGLN030 and smaller devices use different CCCs in their architecture (CCC-GL). These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these are located at the four corners and the centers of the east and west sides. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

***Table 2-17 •*** **Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

| Parameter | Definition | Device-Specific Dynamic Power (µW/MHz) | | | | | |
|---|---|---|---|---|---|---|---|
| | | AGLN250 | AGLN125 | AGLN060 | AGLN020 | AGLN015 | AGLN010 |
| PAC1 | Clock contribution of a Global Rib | 2.829 | 2.875 | 1.728 | 0 | 0 | 0 |
| PAC2 | Clock contribution of a Global Spine | 1.731 | 1.265 | 1.268 | 2.562 | 2.562 | 1.685 |
| PAC3 | Clock contribution of a VersaTile row | 0.957 | 0.963 | 0.967 | 0.862 | 0.862 | 0.858 |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.098 | 0.098 | 0.098 | 0.094 | 0.094 | 0.091 |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.045 | | | | | |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.186 | | | | | |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.11 | | | | | |
| PAC8 | Average contribution of a routing net | 0.45 | | | | | |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-13 on page 2-9 | | | | | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-14 on page 2-9 | | | | | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | | | N/A | | |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | | | N/A | | |
| PAC13 | Dynamic contribution for PLL | 2.10 | | | N/A | | |

***Table 2-18 •*** **Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 Devices, 1.2 V Core Supply Voltage**

| Parameter | Definition | Device-Specific Static Power (mW) | | | | | |
|---|---|---|---|---|---|---|---|
| | | AGLN250 | AGLN125 | AGLN060 | AGLN020 | AGLN015 | AGLN010 |
| PDC1 | Array static power in Active mode | See Table 2-12 on page 2-8 | | | | | |
| PDC2 | Array static power in Static (Idle) mode | See Table 2-12 on page 2-8 | | | | | |
| PDC3 | Array static power in Flash*Freeze mode | See Table 2-9 on page 2-7 | | | | | |
| PDC4 [1] | Static PLL contribution | 0.90 | | | N/A | | |
| PDC5 | Bank quiescent power (VCCI-dependent)[2] | See Table 2-12 on page 2-8 | | | | | |

*Notes:*

1. *Minimum contribution of the PLL when running at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.*

## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

### Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

***Table 2-19 •*** **Toggle Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\alpha_1$ | Toggle rate of VersaTile outputs | 10% |
| $\alpha_2$ | I/O buffer toggle rate | 10% |

***Table 2-20 •*** **Enable Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\beta_1$ | I/O output buffer enable rate | 100% |
| $\beta_2$ | RAM enable rate for read operations | 12.5% |
| $\beta_3$ | RAM enable rate for write operations | 12.5% |

## Summary of I/O Timing Characteristics – Default I/O Software Settings

***Table 2-23 •*** **Summary of AC Measuring Points**

| Standard | Measuring Trip Point (Vtrip) |
|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 1.4 V |
| 3.3 V LVCMOS Wide Range | 1.4 V |
| 2.5 V LVCMOS | 1.2 V |
| 1.8 V LVCMOS | 0.90 V |
| 1.5 V LVCMOS | 0.75 V |
| 1.2 V LVCMOS | 0.60 V |
| 1.2 V LVCMOS Wide Range | 0.60 V |

***Table 2-24 •*** **I/O AC Parameter Definitions**

| Parameter | Parameter Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—HIGH to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to HIGH |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—LOW to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to LOW |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW |

### *Applies to IGLOO nano at 1.5 V Core Operating Conditions*

***Table 2-25 •*** **Summary of I/O Timing Characteristics—Software Default Settings**
**STD Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 3.0 V**

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 8 mA | 8 mA | High | 5 pF | 0.97 | 1.79 | 0.19 | 0.86 | 1.16 | 0.66 | 1.83 | 1.45 | 1.98 | 2.38 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 8 mA | High | 5 pF | 0.97 | 2.56 | 0.19 | 1.20 | 1.66 | 0.66 | 2.57 | 2.02 | 2.82 | 3.31 | ns |
| 2.5 V LVCMOS | 8 mA | 8 mA | High | 5 pF | 0.97 | 1.81 | 0.19 | 1.10 | 1.24 | 0.66 | 1.85 | 1.63 | 1.97 | 2.26 | ns |
| 1.8 V LVCMOS | 4 mA | 4 mA | High | 5 pF | 0.97 | 2.08 | 0.19 | 1.03 | 1.44 | 0.66 | 2.12 | 1.95 | 1.99 | 2.19 | ns |
| 1.5 V LVCMOS | 2 mA | 2 mA | High | 5 pF | 0.97 | 2.39 | 0.19 | 1.19 | 1.52 | 0.66 | 2.44 | 2.24 | 2.02 | 2.15 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| | $R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω) | | $R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω) | |
|---|---|---|---|---|
| **VCCI** | **Min.** | **Max.** | **Min.** | **Max.** |
| 3.3 V | 10 K | 45 K | 10 K | 45 K |
| 3.3 V (wide range I/Os) | 10 K | 45 K | 10 K | 45 K |
| 2.5 V | 11 K | 55 K | 12 K | 74 K |
| 1.8 V | 18 K | 70 K | 17 K | 110 K |
| 1.5 V | 19 K | 90 K | 19 K | 140 K |
| 1.2 V | 25 K | 110 K | 25 K | 150 K |
| 1.2 V (wide range I/Os) | 19 K | 110 K | 19 K | 150 K |

*Notes:*

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

**Table 2-30 • I/O Short Currents IOSH/IOSL**

| | **Drive Strength** | **IOSL (mA)*** | **IOSH (mA)*** |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as equivalent software default drive | |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| 1.2 V LVCMOS | 1 mA | 10 | 13 |
| 1.2 V LVCMOS Wide Range | 100 µA | 10 | 13 |

*Note: *$T_J$ = 100°C*

### *Applies to 1.2 V DC Core Voltage*

***Table 2-38 •*** **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 4.09 | 0.26 | 0.97 | 1.36 | 1.10 | 4.16 | 3.91 | 2.19 | 2.64 | ns |
| 4 mA | STD | 1.55 | 4.09 | 0.26 | 0.97 | 1.36 | 1.10 | 4.16 | 3.91 | 2.19 | 2.64 | ns |
| 6 mA | STD | 1.55 | 3.45 | 0.26 | 0.97 | 1.36 | 1.10 | 3.51 | 3.32 | 2.43 | 3.03 | ns |
| 8 mA | STD | 1.55 | 3.45 | 0.26 | 0.97 | 1.36 | 1.10 | 3.51 | 3.32 | 2.43 | 3.03 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-39 •*** **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 2.68 | 0.26 | 0.97 | 1.36 | 1.10 | 2.72 | 2.26 | 2.19 | 2.74 | ns |
| 4 mA | STD | 1.55 | 2.68 | 0.26 | 0.97 | 1.36 | 1.10 | 2.72 | 2.26 | 2.19 | 2.74 | ns |
| 6 mA | STD | 1.55 | 2.31 | 0.26 | 0.97 | 1.36 | 1.10 | 2.34 | 1.90 | 2.43 | 3.14 | ns |
| 8 mA | STD | 1.55 | 2.31 | 0.26 | 0.97 | 1.36 | 1.10 | 2.34 | 1.90 | 2.43 | 3.14 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Applies to 1.2 V DC Core Voltage***

***Table 2-49 •*** **2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 4.61 | 0.26 | 1.21 | 1.39 | 1.10 | 4.55 | 4.61 | 2.15 | 2.43 | ns |
| 4 mA | STD | 1.55 | 4.61 | 0.26 | 1.21 | 1.39 | 1.10 | 4.55 | 4.61 | 2.15 | 2.43 | ns |
| 6 mA | STD | 1.55 | 3.86 | 0.26 | 1.21 | 1.39 | 1.10 | 3.82 | 3.86 | 2.41 | 2.89 | ns |
| 8 mA | STD | 1.55 | 3.86 | 0.26 | 1.21 | 1.39 | 1.10 | 3.82 | 3.86 | 2.41 | 2.89 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-50 •*** **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 1.55 | 2.68 | 0.26 | 1.21 | 1.39 | 1.10 | 2.72 | 2.54 | 2.15 | 2.51 | ns |
| 4 mA | STD | 1.55 | 2.68 | 0.26 | 1.21 | 1.39 | 1.10 | 2.72 | 2.54 | 2.15 | 2.51 | ns |
| 6 mA | STD | 1.55 | 2.30 | 0.26 | 1.21 | 1.39 | 1.10 | 2.33 | 2.04 | 2.41 | 2.99 | ns |
| 8 mA | STD | 1.55 | 2.30 | 0.26 | 1.21 | 1.39 | 1.10 | 2.33 | 2.04 | 2.41 | 2.99 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-83 • Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.60 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 1.09 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 1.16 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.99 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.24 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 160.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-90 •*** **AGLN020 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.21 | 1.55 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.23 | 1.65 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-91 •*** **AGLN060 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.32 | 1.62 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.34 | 1.71 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.38 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-94 • AGLN010 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.71 | 2.09 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.78 | 2.31 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.53 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-95 • AGLN015 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.81 | 2.26 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.90 | 2.51 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.61 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-102 • RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.69 | ns |
| $t_{AH}$ | Address hold time | 0.13 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.68 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 1.37 | ns |
| $t_{BKH}$ | BLK hold time | 0.13 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.59 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.30 | ns |
| $t_{CKQ1}$ | Clock HIGH to new data valid on DOUT (output retained, WMODE = 0) | 2.94 | ns |
| | Clock HIGH to new data valid on DOUT (flow-through, WMODE = 1) | 2.55 | ns |
| $t_{CKQ2}$ | Clock HIGH to new data valid on DOUT (pipelined) | 1.51 | ns |
| $t_{C2CWWL}$[1] | Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge | 0.23 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.35 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 0.41 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 1.72 | ns |
| | RESET Low to data out Low on DOUT (pipelined) | 1.72 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.51 | ns |
| $t_{RECRSTB}$ | RESET recovery | 2.68 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

*Notes:*

1. *For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### Timing Waveforms

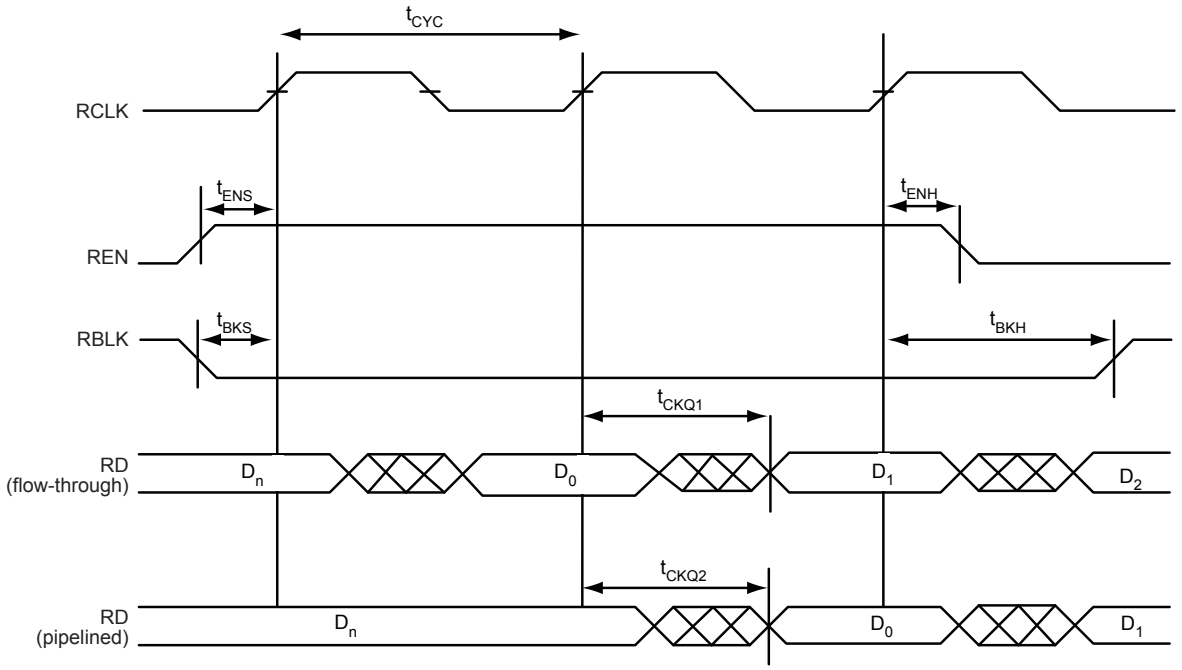



***Figure 2-34 •*** **FIFO Read**

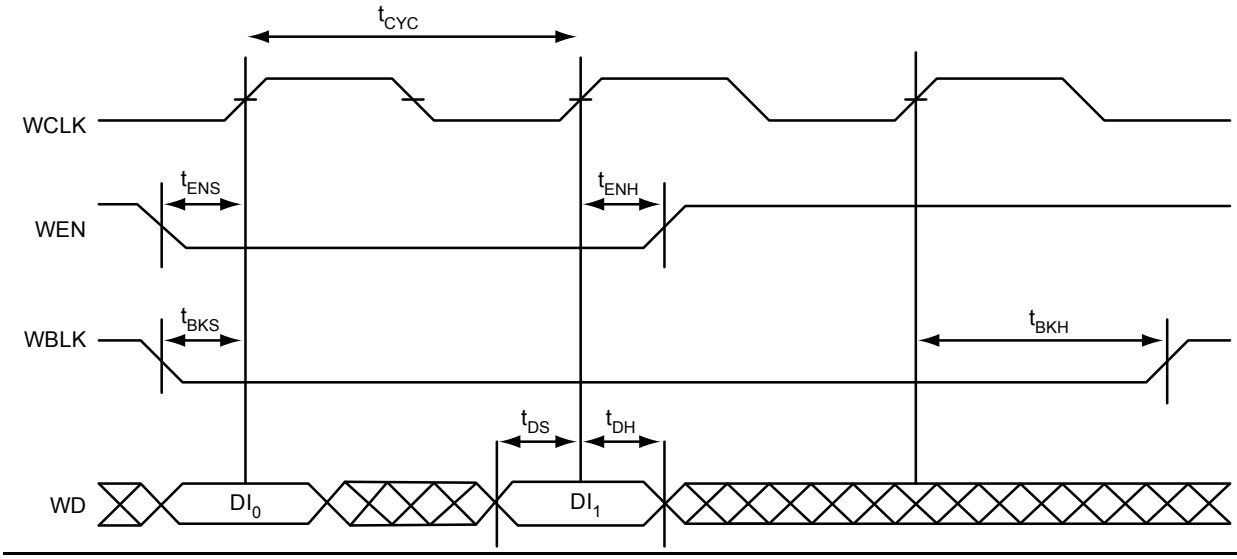



***Figure 2-35 •*** **FIFO Write**

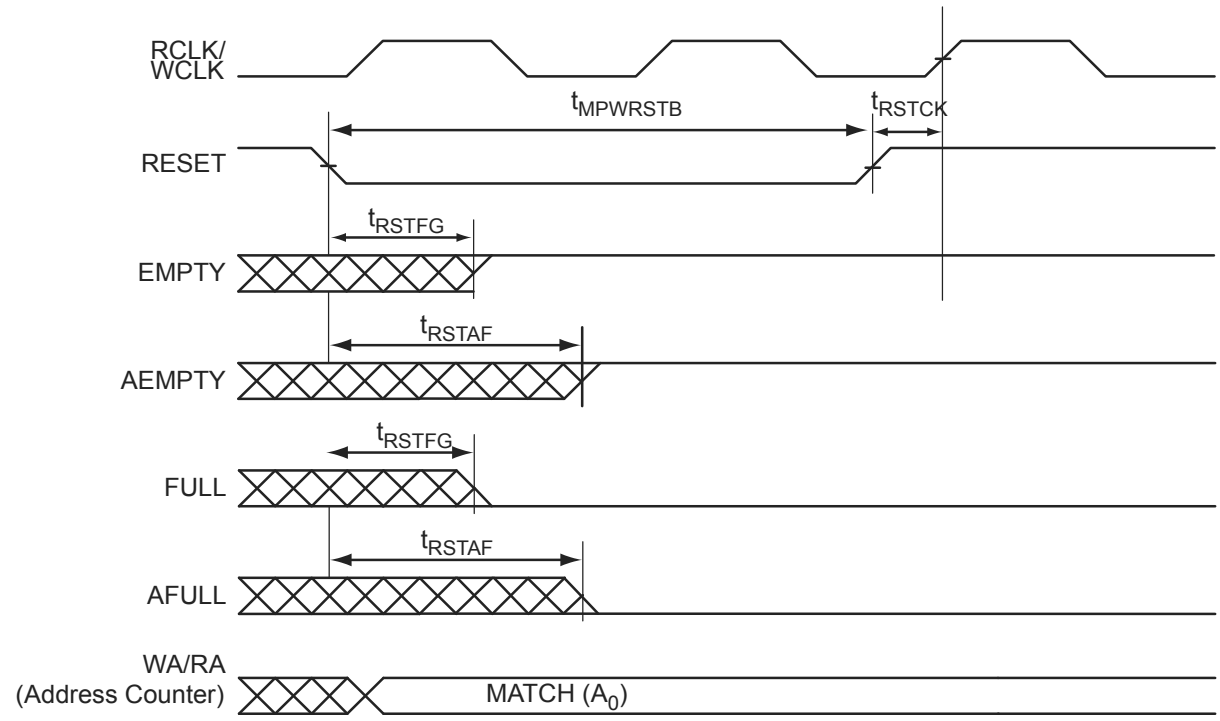



***Figure 2-36 •*** **FIFO Reset**

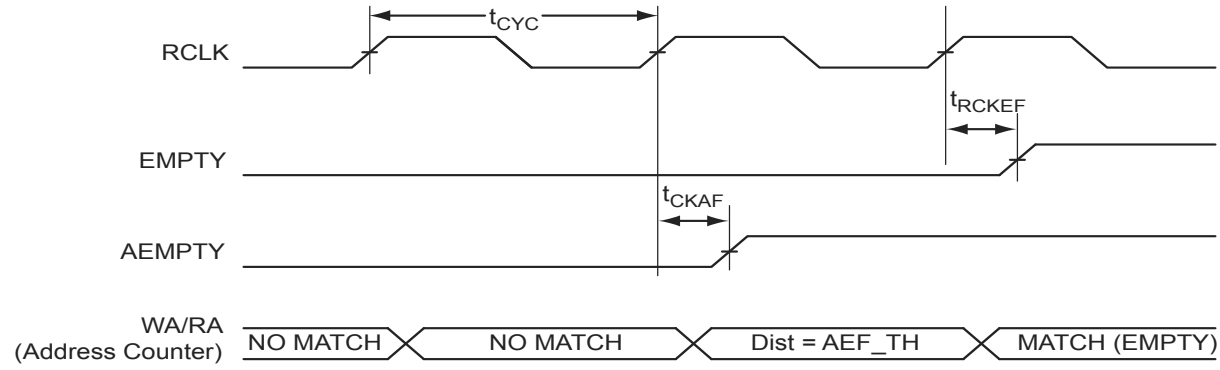
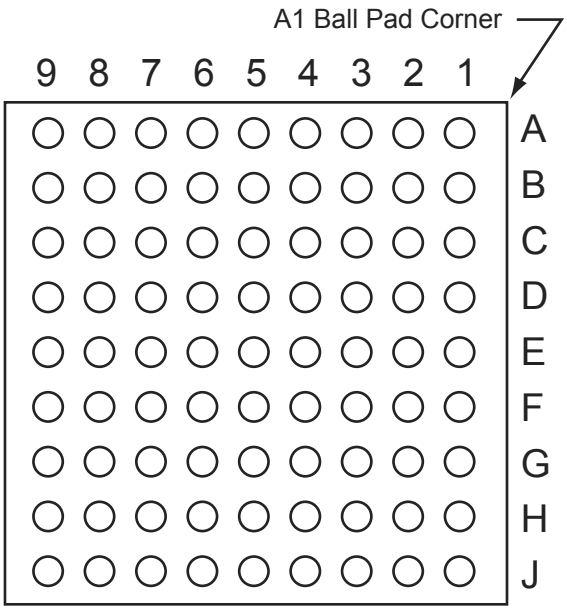



***Figure 2-37 •*** **FIFO EMPTY Flag and AEMPTY Flag Assertion**

# CS81

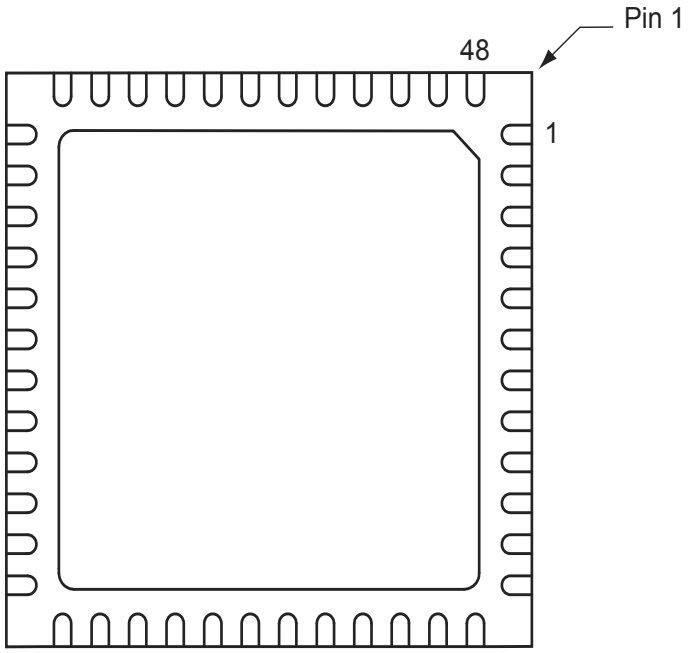



*Note: This is the bottom view of the package.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

# QN48




*Notes:*

1. *This is the bottom view of the package.*
2. *The die attach paddle of the package is tied to ground (GND).*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| VQ100 | |
|---|---|
| **Pin Number** | **AGLN060Z Function** |
| 1 | GND |
| 2 | GAA2/IO51RSB1 |
| 3 | IO52RSB1 |
| 4 | GAB2/IO53RSB1 |
| 5 | IO95RSB1 |
| 6 | GAC2/IO94RSB1 |
| 7 | IO93RSB1 |
| 8 | IO92RSB1 |
| 9 | GND |
| 10 | GFB1/IO87RSB1 |
| 11 | GFB0/IO86RSB1 |
| 12 | VCOMPLF |
| 13 | GFA0/IO85RSB1 |
| 14 | VCCPLF |
| 15 | GFA1/IO84RSB1 |
| 16 | GFA2/IO83RSB1 |
| 17 | VCC |
| 18 | VCCIB1 |
| 19 | GEC1/IO77RSB1 |
| 20 | GEB1/IO75RSB1 |
| 21 | GEB0/IO74RSB1 |
| 22 | GEA1/IO73RSB1 |
| 23 | GEA0/IO72RSB1 |
| 24 | VMV1 |
| 25 | GNDQ |
| 26 | GEA2/IO71RSB1 |
| 27 | FF/GEB2/IO70RSB1 |
| 28 | GEC2/IO69RSB1 |
| 29 | IO68RSB1 |
| 30 | IO67RSB1 |
| 31 | IO66RSB1 |
| 32 | IO65RSB1 |
| 33 | IO64RSB1 |
| 34 | IO63RSB1 |

| VQ100 | |
|---|---|
| **Pin Number** | **AGLN060Z Function** |
| 35 | IO62RSB1 |
| 36 | IO61RSB1 |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB1 |
| 40 | IO60RSB1 |
| 41 | IO59RSB1 |
| 42 | IO58RSB1 |
| 43 | IO57RSB1 |
| 44 | GDC2/IO56RSB1 |
| 45* | GDB2/IO55RSB1 |
| 46 | GDA2/IO54RSB1 |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV1 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO49RSB0 |
| 58 | GDC0/IO46RSB0 |
| 59 | GDC1/IO45RSB0 |
| 60 | GCC2/IO43RSB0 |
| 61 | GCB2/IO42RSB0 |
| 62 | GCA0/IO40RSB0 |
| 63 | GCA1/IO39RSB0 |
| 64 | GCC0/IO36RSB0 |
| 65 | GCC1/IO35RSB0 |
| 66 | VCCIB0 |
| 67 | GND |
| 68 | VCC |

| VQ100 | |
|---|---|
| **Pin Number** | **AGLN060Z Function** |
| 69 | IO31RSB0 |
| 70 | GBC2/IO29RSB0 |
| 71 | GBB2/IO27RSB0 |
| 72 | IO26RSB0 |
| 73 | GBA2/IO25RSB0 |
| 74 | VMV0 |
| 75 | GNDQ |
| 76 | GBA1/IO24RSB0 |
| 77 | GBA0/IO23RSB0 |
| 78 | GBB1/IO22RSB0 |
| 79 | GBB0/IO21RSB0 |
| 80 | GBC1/IO20RSB0 |
| 81 | GBC0/IO19RSB0 |
| 82 | IO18RSB0 |
| 83 | IO17RSB0 |
| 84 | IO15RSB0 |
| 85 | IO13RSB0 |
| 86 | IO11RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO10RSB0 |
| 91 | IO09RSB0 |
| 92 | IO08RSB0 |
| 93 | GAC1/IO07RSB0 |
| 94 | GAC0/IO06RSB0 |
| 95 | GAB1/IO05RSB0 |
| 96 | GAB0/IO04RSB0 |
| 97 | GAA1/IO03RSB0 |
| 98 | GAA0/IO02RSB0 |
| 99 | IO01RSB0 |
| 100 | IO00RSB0 |

*Note: *The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin 45 in AGLN060Z-VQ100.*

| VQ100 | |
|---|---|
| Pin Number | AGLN250Z Function |
| 1 | GND |
| 2 | GAA2/IO67RSB3 |
| 3 | IO66RSB3 |
| 4 | GAB2/IO65RSB3 |
| 5 | IO64RSB3 |
| 6 | GAC2/IO63RSB3 |
| 7 | IO62RSB3 |
| 8 | IO61RSB3 |
| 9 | GND |
| 10 | GFB1/IO60RSB3 |
| 11 | GFB0/IO59RSB3 |
| 12 | VCOMPLF |
| 13 | GFA0/IO57RSB3 |
| 14 | VCCPLF |
| 15 | GFA1/IO58RSB3 |
| 16 | GFA2/IO56RSB3 |
| 17 | VCC |
| 18 | VCCIB3 |
| 19 | GFC2/IO55RSB3 |
| 20 | GEC1/IO54RSB3 |
| 21 | GEC0/IO53RSB3 |
| 22 | GEA1/IO52RSB3 |
| 23 | GEA0/IO51RSB3 |
| 24 | VMV3 |
| 25 | GNDQ |
| 26 | GEA2/IO50RSB2 |
| 27 | FF/GEB2/IO49RSB2 |
| 28 | GEC2/IO48RSB2 |
| 29 | IO47RSB2 |
| 30 | IO46RSB2 |
| 31 | IO45RSB2 |
| 32 | IO44RSB2 |
| 33 | IO43RSB2 |
| 34 | IO42RSB2 |
| 35 | IO41RSB2 |
| 36 | IO40RSB2 |

| VQ100 | |
|---|---|
| Pin Number | AGLN250Z Function |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB2 |
| 40 | IO39RSB2 |
| 41 | IO38RSB2 |
| 42 | IO37RSB2 |
| 43 | GDC2/IO36RSB2 |
| 44 | GDB2/IO35RSB2 |
| 45 | GDA2/IO34RSB2 |
| 46 | GNDQ |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV2 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO33RSB1 |
| 58 | GDC0/IO32RSB1 |
| 59 | GDC1/IO31RSB1 |
| 60 | IO30RSB1 |
| 61 | GCB2/IO29RSB1 |
| 62 | GCA1/IO27RSB1 |
| 63 | GCA0/IO28RSB1 |
| 64 | GCC0/IO26RSB1 |
| 65 | GCC1/IO25RSB1 |
| 66 | VCCIB1 |
| 67 | GND |
| 68 | VCC |
| 69 | IO24RSB1 |
| 70 | GBC2/IO23RSB1 |
| 71 | GBB2/IO22RSB1 |
| 72 | IO21RSB1 |

| VQ100 | |
|---|---|
| Pin Number | AGLN250Z Function |
| 73 | GBA2/IO20RSB1 |
| 74 | VMV1 |
| 75 | GNDQ |
| 76 | GBA1/IO19RSB0 |
| 77 | GBA0/IO18RSB0 |
| 78 | GBB1/IO17RSB0 |
| 79 | GBB0/IO16RSB0 |
| 80 | GBC1/IO15RSB0 |
| 81 | GBC0/IO14RSB0 |
| 82 | IO13RSB0 |
| 83 | IO12RSB0 |
| 84 | IO11RSB0 |
| 85 | IO10RSB0 |
| 86 | IO09RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO08RSB0 |
| 91 | IO07RSB0 |
| 92 | IO06RSB0 |
| 93 | GAC1/IO05RSB0 |
| 94 | GAC0/IO04RSB0 |
| 95 | GAB1/IO03RSB0 |
| 96 | GAB0/IO02RSB0 |
| 97 | GAA1/IO01RSB0 |
| 98 | GAA0/IO00RSB0 |
| 99 | GNDQ |
| 100 | VMV0 |

# 5 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each version of the IGLOO nano datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 19 (October 2015) | Modified the note to include device/package obsoletion information in "Features and Benefits" section (SAR 69724). | 1-I |
| | Added a note under Security Feature "Y" in "IGLOO nano Ordering Information" section (SAR 70553). | 1-IV |
| | Modified AGLN250 pin assignment table to match with I/O Attribute Editor tool from Libero in "CS81" Package (SAR 59049). | 4-6 |
| | Modified the nominal area to 25 for CS81 Package in Table 1 (SAR 71127). | 1-II |
| | Modified the title of AGLN125Z pin assignment table for "CS81" Package (SAR 71127). | 4-6 |
| Revision 18 (November 2013) | Modified the "Device Marking" section and updated Figure 1 • Example of Device Marking for Small Form Factor Packages to reflect updates suggested per CN1004 published on 5/10/2010 (SAR 52036). | V |
| Revision 17 (May 2013) | Deleted details related to Ambient temperature from "Enhanced Commercial Temperature Range", "IGLOO nano Ordering Information", "Temperature Grade Offerings", and Table 2-2 • Recommended Operating Conditions [1] to remove ambiguities arising due to the same, and modified Note 2 (SAR 47063). | I, IV, VI, and 2-2 |
| Revision 16 (December 2012) | The "IGLOO nano Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43174). | IV |
| | The note in Table 2-100 • IGLOO nano CCC/PLL Specification and Table 2-101 • IGLOO nano CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42565). | 2-70, 2-71 |
| | Live at Power-Up (LAPU) has been replaced with ’Instant On’. | NA |
| Revision 15 (September 2012) | The status of the AGLN125 device has been modified from ’Advance’ to ’Production’ in the "IGLOO nano Device Status" section (SAR 41416). | III |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40274). | NA |
| Revision 14 (September 2012) | The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-2 |
| Revision 13 (June 2012) | Figure Figure 2-34 • FIFO Read and Figure 2-35 • FIFO Write have been added (SAR 34842). | 2-82 |
| | The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38319). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement. | 3-1 |