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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	68
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln250v5-vqg100i

IGLOO nano Devices	AGLN010	AGLN015 ¹	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices ¹				AGLN030Z ¹	AGLN060Z ¹	AGLN125Z ¹	AGLN250Z ¹
Package Pins							
UC/CS	UC36		UC81,	UC81, CS81	CS81	CS81	CS81
QFN	QN48	QN68	CS81	QN48, QN68			
VQFP			QN68	VQ100	VQ100	VQ100	VQ100

Notes:

1. Not recommended for new designs. Few devices/packages are obsoleted. For more information on obsoleted devices/packages, refer to the PDN 1503 - IGLOO nano Z and ProASIC3 nano Z Families.
2. AGLN030 and smaller devices do not support this feature.
3. AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs.
4. For higher densities and support of additional features, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOOe Low-Power Flash FPGAs Datasheet.

I/Os Per Package

IGLOO nano Devices	AGLN010	AGLN015 ¹	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices ¹				AGLN030Z ¹	AGLN060Z ¹	AGLN125Z ¹	AGLN250Z ¹
Known Good Die	34	—	52	83	71	71	68
UC36	23	—	—	—	—	—	—
QN48	34	—	—	34	—	—	—
QN68	—	49	49	49	—	—	—
UC81	—	—	52	66	—	—	—
CS81	—	—	52	66	60	60	60
VQ100	—	—	—	77	71	71	68

Notes:

1. Not recommended for new designs.
2. When considering migrating your design to a lower- or higher-density device, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOO FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.
3. When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.
4. "G" indicates RoHS-compliant packages. Refer to "IGLOO nano Ordering Information" on page IV for the location of the "G" in the part number. For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.

Table 1 • IGLOO nano FPGAs Package Sizes Dimensions

Packages	UC36	UC81	CS81	QN48	QN68	VQ100
Length × Width (mm\mm)	3 x 3	4 x 4	5 x 5	6 x 6	8 x 8	14 x 14
Nominal Area (mm ²)	9	16	25	36	64	196
Pitch (mm)	0.4	0.4	0.5	0.4	0.4	0.5
Height (mm)	0.80	0.80	0.80	0.90	0.90	1.20

Flash Advantages

Low Power

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

Security

Nonvolatile, flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO nano devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO nano device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Microsemi flash-based IGLOO nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano flash FPGAs enable the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 μ s) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$ for V5 devices, and $0.75\text{ V} \pm 0.2\text{ V}$ for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

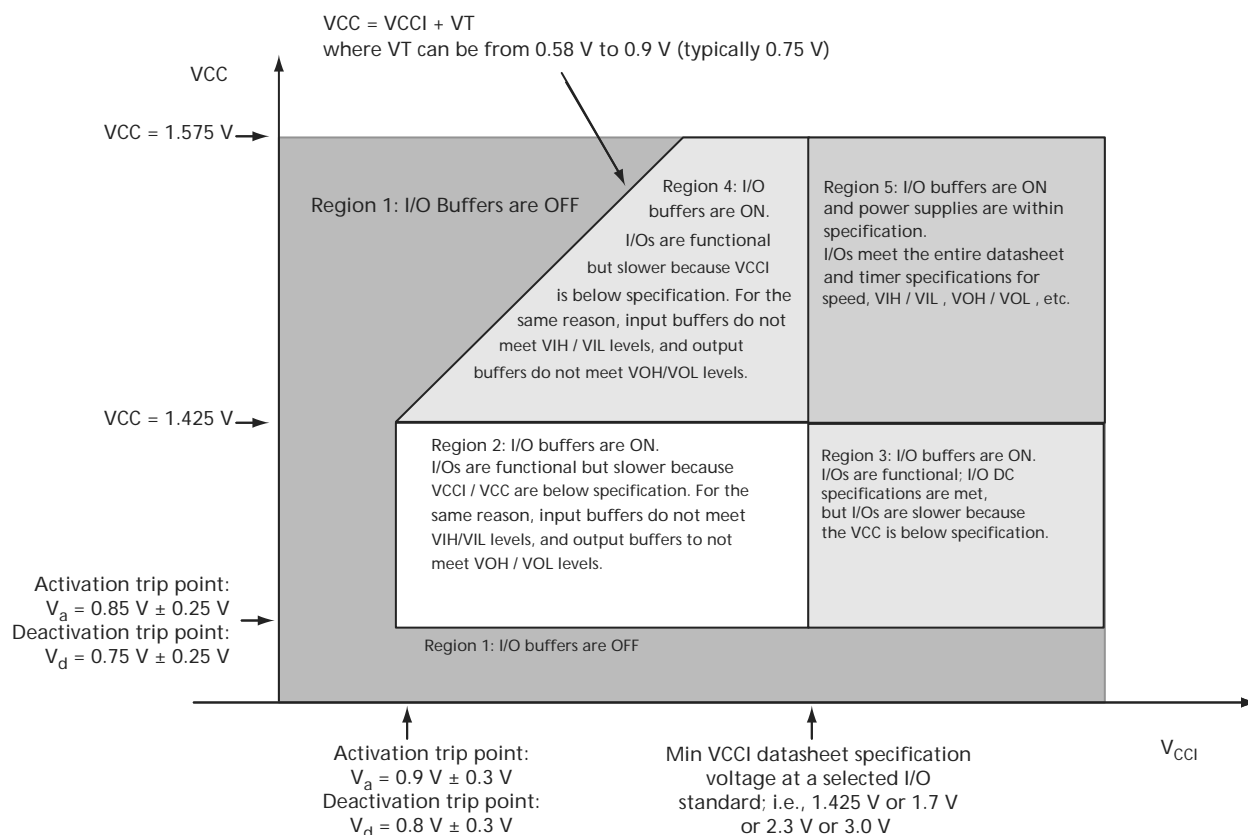


Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

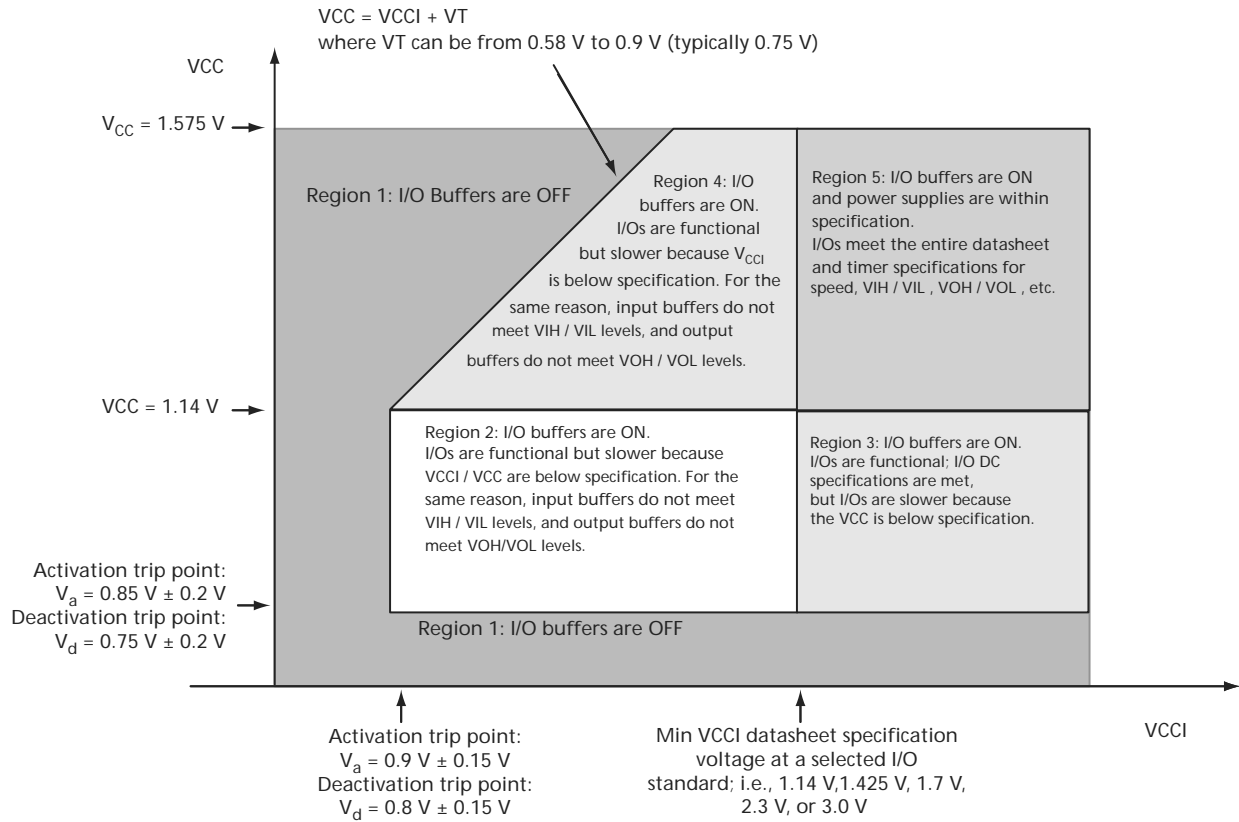


Figure 2-2 • V2 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels

Power Consumption of Various Internal Resources

Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage

Parameter	Definition	Device Specific Dynamic Power ($\mu\text{W}/\text{MHz}$)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	4.421	4.493	2.700	0	0	0
PAC2	Clock contribution of a Global Spine	2.704	1.976	1.982	4.002	4.002	2.633
PAC3	Clock contribution of a VersaTile row	1.496	1.504	1.511	1.346	1.346	1.340
PAC4	Clock contribution of a VersaTile used as a sequential module	0.152	0.153	0.153	0.148	0.148	0.143
PAC5	First contribution of a VersaTile used as a sequential module	0.057					
PAC6	Second contribution of a VersaTile used as a sequential module	0.207					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.17					
PAC8	Average contribution of a routing net	0.7					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9.					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14.					
PAC11	Average contribution of a RAM block during a read operation	25.00			N/A		
PAC12	Average contribution of a RAM block during a write operation	30.00			N/A		
PAC13	Dynamic contribution for PLL	2.70			N/A		

Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage

Parameter	Definition	Device -Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8					
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7					
PDC4 ¹	Static PLL contribution	1.84			N/A		
PDC5	Bank quiescent power (VCCI-dependent) ²	See Table 2-12 on page 2-8					

Notes:

1. Minimum contribution of the PLL when running at lowest frequency.
2. For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 8 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40°C	> 20 years
–20°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

**Table 2-32 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers**

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTTL / LVCMOS (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (100°C)
LVTTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Applies to 1.2 V DC Core Voltage

Table 2-43 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 μA	4 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 μA	6 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns
100 μA	8 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-44 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 μA	4 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 μA	6 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
100 μA	8 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
3. Software default selection highlighted in gray.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5 V applications.

Table 2-45 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ³	Max., mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operating conditions where $-0.3 < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions where $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

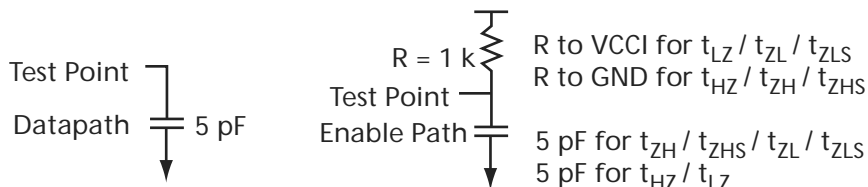


Figure 2-8 • AC Loading

Table 2-46 • 2.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = V_{trip} . See Table 2-23 on page 2-20 for a complete table of trip points.

1.2 V DC Core Voltage

Table 2-75 • Output Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OCKMPWH}	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
t_{OCKMPWL}	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-80 • Input DDR Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.76	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.94	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.93	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.84	ns
t_{DDRILD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRILD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
t_{DDRWCCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

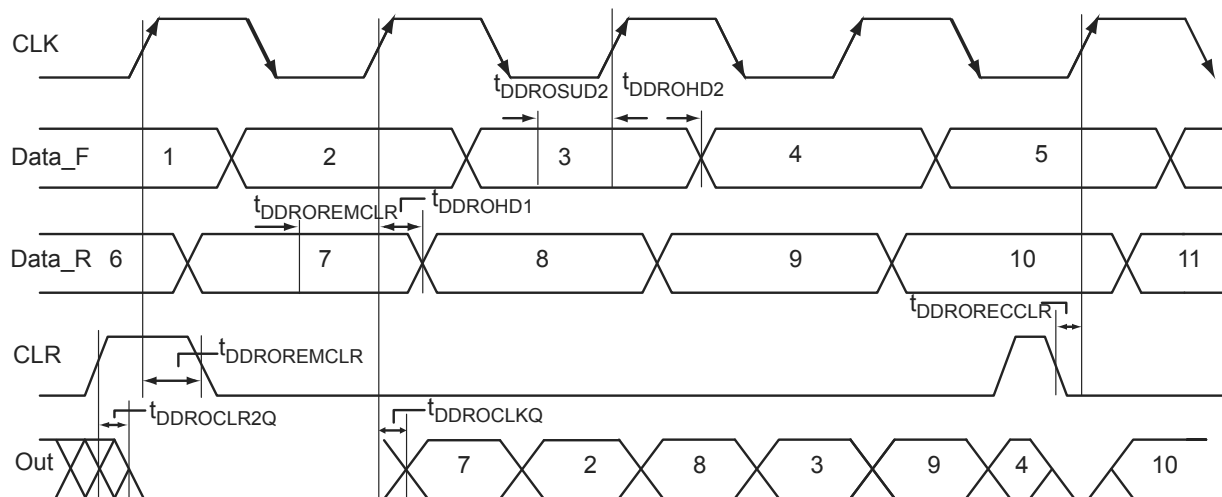


Figure 2-20 • Output DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • Output DDR Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	1.07	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.67	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.67	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{\text{DDROEMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{\text{DDROECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-101 • IGLOO nano CCC/PLL Specification
For IGLOO nano V2 Devices, 1.2 V DC Core Supply Voltage

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		160	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}			580 ³		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Serial Clock (SCLK) for Dynamic PLL ^{4,9}				60	
Input Cycle-to-Cycle Jitter (peak magnitude)				0.25	ns
Acquisition Time					
	LockControl = 0			300	μs
	LockControl = 1			6.0	ms
Tracking Jitter ⁵					
	LockControl = 0			4	ns
	LockControl = 1			3	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay ^{1, 2}		2.3		20.86	ns
Delay Range in Block: Programmable Delay ^{1, 2}		0.025		20.86	ns
Delay Range in Block: Fixed Delay ^{1, 2}			5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} ⁶		Max Peak-to-Peak Period Jitter ^{6,7,8}			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16	
0.75 MHz to 50MHz		0.50	1.20	2.00	3.00 %
50 MHz to 100 MHz		2.50	5.00	7.00	15.00 %

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.2\text{ V}$.
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
4. Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
6. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.
7. Measurements done with LVTTTL 3.3 V 8 mA I/O drive strength and high slew rate. $V_{CC}/V_{CCPLL} = 1.14\text{ V}$, $V_{CCI} = 3.3\text{ V}$, VQ/PQ/TQ type of packages, 20 pF load.
8. SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within $\pm 200\text{ ps}$ of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO nano FPGA Fabric User's Guide.
9. The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.

Table 2-105 • RAM512X18

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.13	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{DS}	Input data (WD) setup time	1.10	ns
t_{DH}	Input data (WD) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	6.56	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	2.67	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.87	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.04	ns
t_{RSTBQ}	RESET LOW to data out LOW on RD (flow through)	3.21	ns
	RESET LOW to data out LOW on RD (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

FIFO

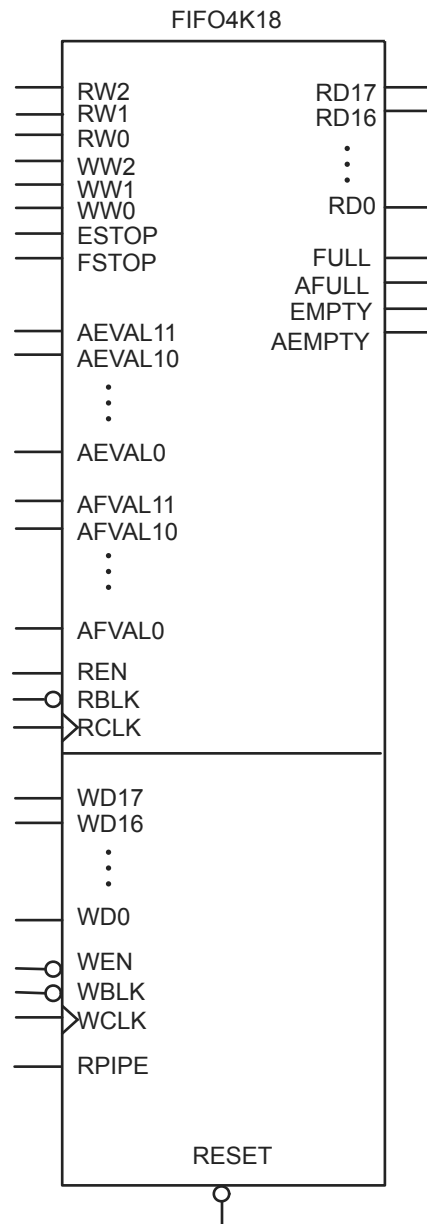


Figure 2-33 • FIFO Model

Timing Waveforms

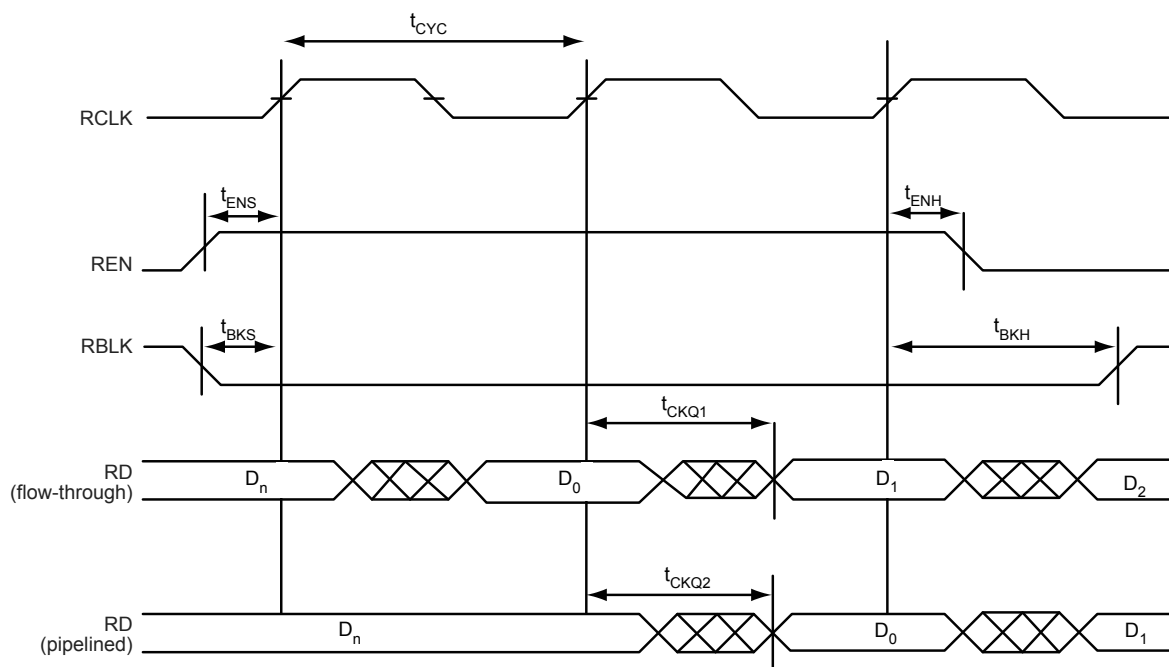


Figure 2-34 • FIFO Read

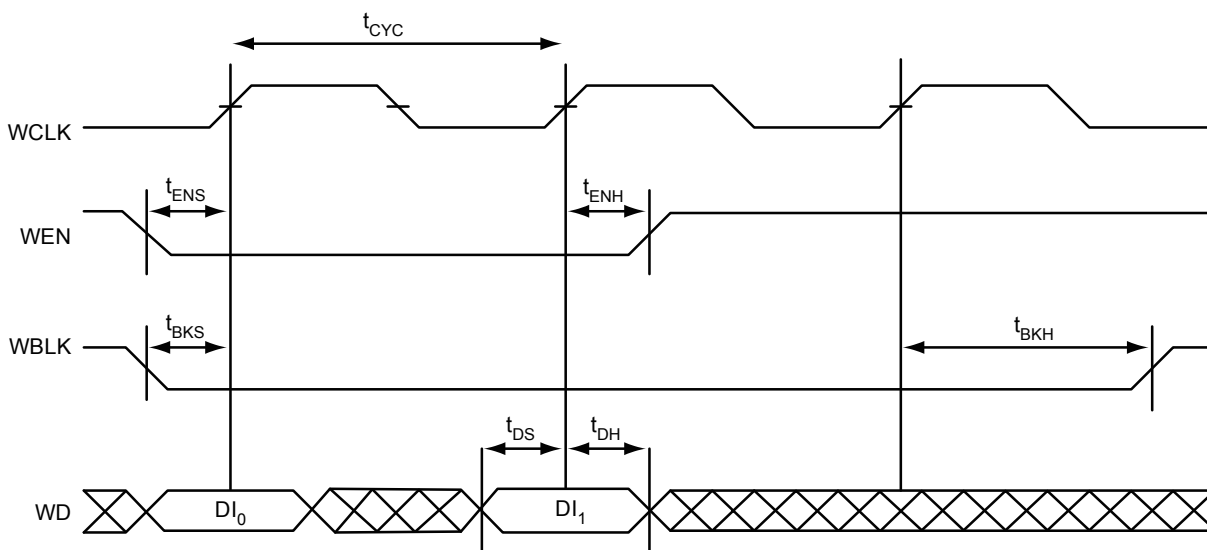


Figure 2-35 • FIFO Write

Timing Characteristics

1.5 V DC Core Voltage

Table 2-106 • FIFO

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	ns
t_{ENH}	REN, WEN Hold Time	0.13	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.63	ns
t_{DH}	Input Data (WD) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET Low to Data Out LOW on RD (flow-through)	1.68	ns
	RESET Low to Data Out LOW on RD (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET Removal	0.51	ns
$t_{RECRSTB}$	RESET Recovery	2.68	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-107 • FIFO

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.30	ns
t_{DH}	Input Data (DI) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET LOW to Data Out Low on RD (flow-through)	3.41	ns
	RESET LOW to Data Out Low on RD (pipelined)	4.09	3.41
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Embedded FlashROM Characteristics

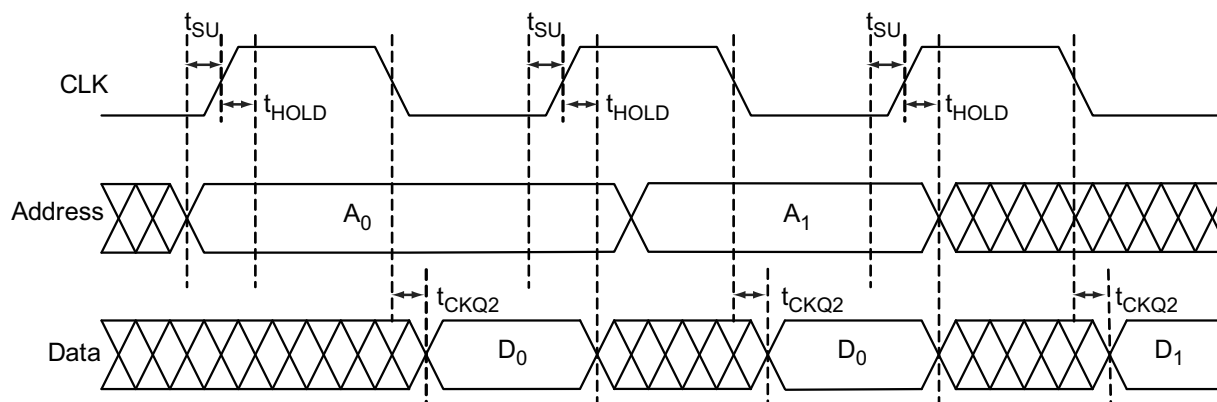


Figure 2-41 • Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-108 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	20.90	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-109 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	35.74	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-110 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
t_{TRSTREM}	ResetB Removal Time	0.58	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-111 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
t_{TRSTREM}	ResetB Removal Time	1.18	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO nano devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO nano devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO nano FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 • Flash*Freeze Pin Locations for IGLOO nano Devices

Package	Flash*Freeze Pin
CS81/UC81	H2
QN48	14
QN68	18
VQ100	27
UC36	E2

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 • Recommended Tie-Off Values for the TCK and TRST Pins

VJTAG	Tie-Off Resistance ^{1,2}
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Notes:

1. The TCK pin can be pulled-up or pulled-down.
2. The TRST pin is pulled-down.
3. Equivalent parallel resistance if more than one device is on the JTAG chain