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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	68
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln250v5-zvqg100i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



IGLOO nano Devices	AGLN010	AGLN015 ¹	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices ¹				AGLN030Z ¹	AGLN060Z ¹	AGLN125Z ¹	AGLN250Z ¹
Package Pins							
UC/CS	UC36		UC81,	UC81, CS81	CS81	CS81	CS81
QFN	QN48	QN68	CS81	QN48, QN68			
VQFP			QN68	VQ100	VQ100	VQ100	VQ100

Notes:

Not recommended for new designs. Few devices/packages are obsoleted. For more information on obsoleted devices/packages, refer to the PDN 1503 - IGLOO nano Z and ProASIC3 nano Z Families.

AGLN030 and smaller devices do not support this feature.

3.

AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. For higher densities and support of additional features, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOOe 4. Low-Power Flash FPGAs Datasheet .

I/Os Per Package

IGLOO nano Devices	AGLN010	AGLN015 ¹	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices ¹				AGLN030Z ¹	AGLN060Z ¹	AGLN125Z ¹	AGLN250Z ¹
Known Good Die	34	-	52	83	71	71	68
UC36	23	-	-	_	-	-	-
QN48	34	-	-	34	-	-	-
QN68	-	49	49	49	-	-	-
UC81	-	-	52	66	-	-	-
CS81	-	-	52	66	60	60	60
VQ100	_	_	_	77	71	71	68

Notes:

Not recommended for new designs.

2. When considering migrating your design to a lower- or higher-density device, refer to the DS0095: IGLOO Low Power Flash FPGAs Datasheet and IGLOO FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.

3. When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of singleended user I/Os available is reduced by one.

4. "G" indicates RoHS-compliant packages. Refer to "IGLOO nano Ordering Information" on page IV for the location of the "G" in the part number. For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.

Table 1 • IGLOO nano FPGAs Package Sizes Dimensions

Packages	UC36	UC81	CS81	QN48	QN68	VQ100
Length × Width (mm\mm)	3 x 3	4 x 4	5 x 5	6 x 6	8 x 8	14 x 14
Nominal Area (mm ²)	9	16	25	36	64	196
Pitch (mm)	0.4	0.4	0.5	0.4	0.4	0.5
Height (mm)	0.80	0.80	0.80	0.90	0.90	1.20

1 – IGLOO nano Device Overview

General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO nano devices enables entering and exiting an ultra-low power mode that consumes nanoPower while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO nano device is completely functional in the system. This allows the IGLOO nano device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO nano devices the advantage of being a secure, low power, single-chip solution that is Instant On. The IGLOO nano device is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGLN030 and smaller devices have no PLL or RAM support. IGLOO nano devices have up to 250 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

IGLOO nano devices increase the breadth of the IGLOO product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Features such as smaller footprint packages designed with two-layer PCBs in mind, power consumption measured in nanoPower, Schmitt trigger, and bus hold (hold previous I/O state in Flash*Freeze mode) functionality make these devices ideal for deployment in applications that require high levels of flexibility and low cost.

Flash*Freeze Technology

The IGLOO nano device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO nano devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO nano V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, HIGH, or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and small-footprint packages make IGLOO nano devices the best fit for portable electronics.



Figure 1-3 • IGLOO Device Architecture Overview with Two I/O Banks (AGLN060, AGLN125)



Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)

vcci	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/ Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Table 2-4 • Overshoot and Undershoot Limits ¹

Notes:

1. Based on reliability requirements at 85°C.

 The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO nano device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO nano I/Os are activated only if ALL of the following three conditions are met:

- 1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
- 2. VCCI > VCC 0.75 V (typical)
- 3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC Trip Point:

Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

IGLOO nano DC and Switching Characteristics

Power Consumption of Various Internal Resources

 Table 2-15 •
 Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices

 For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage

			Device Sp	ecific Dyna	mic Power	· (µW/MHz)			
Parameter	Definition	AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010		
PAC1	Clock contribution of a Global Rib	4.421	4.493	2.700	0	0	0		
PAC2	Clock contribution of a Global Spine	2.704	1.976	1.982	4.002	4.002	2.633		
PAC3	Clock contribution of a VersaTile row	1.496	1.504	1.511	1.346	1.346	1.340		
PAC4	Clock contribution of a VersaTile used as a sequential module	0.152	0.153	0.153	0.148	0.148	0.143		
PAC5	First contribution of a VersaTile used as a sequential module			0.0	57				
PAC6	Second contribution of a VersaTile used as a sequential module	0.207							
PAC7	Contribution of a VersaTile used as a combinatorial module			0.	17				
PAC8	Average contribution of a routing net			0.	.7				
PAC9	Contribution of an I/O input pin (standard-dependent)		Se	e Table 2-13	3 on page 2	2-9.			
PAC10	Contribution of an I/O output pin (standard-dependent)			See Tab	le 2-14.				
PAC11	Average contribution of a RAM block during a read operation	K 25.00 N/A							
PAC12	Average contribution of a RAM block during a write operation	. 30.00 N/A							
PAC13	Dynamic contribution for PLL		2.70			N/A			

Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO nano Devices For IGLOO nano V2 or V5 Devices, 1.5 V Core Supply Voltage

			Device	-Specific	Static Powe	er (mW)				
Parameter	Definition	AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010			
PDC1	Array static power in Active mode		Se	e Table 2-1	2 on page	2-8				
PDC2	Array static power in Static (Idle) mode	See Table 2-12 on page 2-8								
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7								
PDC4 ¹	Static PLL contribution		1.84			N/A				
PDC5	Bank quiescent power (VCCI-dependent) ²	See Table 2-12 on page 2-8								

Notes:

1. Minimum contribution of the PLL when running at lowest frequency.

2. For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC.

Combinatorial Cells Contribution—P_{C-CELL}

 $P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

 α_{1} is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

 $\mathsf{F}_{\mathsf{CLK}}$ is the global clock signal frequency.

Routing Net Contribution—P_{NET}

 $P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

 $N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

 α_{1} is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—PINPUTS

 $P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—POUTPUTS

 $P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

N_{OUTPUTS} is the number of I/O output buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

 β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-20 on page 2-14.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

 $\mathsf{P}_{\mathsf{MEMORY}} = \mathsf{PAC11} * \mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{F}_{\mathsf{READ-CLOCK}} * \beta_2 + \mathsf{PAC12} * \mathsf{N}_{\mathsf{BLOCK}} * \mathsf{F}_{\mathsf{WRITE-CLOCK}} * \beta_3$

 $N_{\mbox{\scriptsize BLOCKS}}$ is the number of RAM blocks used in the design.

 $\mathsf{F}_{\mathsf{READ-CLOCK}}$ is the memory read clock frequency.

 β_2 is the RAM enable rate for read operations.

F_{WRITE-CLOCK} is the memory write clock frequency.

 β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-20 on page 2-14.

PLL Contribution—P_{PLL}

P_{PLL} = PDC4 + PAC13 *F_{CLKOUT}

F_{CLKOUT} is the output clock frequency.¹

1. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution (PAC13* FCLKOUT product) to the total PLL contribution.

IGLOO nano DC and Switching Characteristics



Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

IGLOO nano DC and Switching Characteristics

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-23 • Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
3.3 V LVCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
1.2 V LVCMOS	0.60 V
1.2 V LVCMOS Wide Range	0.60 V

Table 2-24 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t _{DP}	Data to Pad delay through the Output Buffer
t _{PY}	Pad to Data delay through the Input Buffer
t _{DOUT}	Data to Output Buffer delay through the I/O interface
t _{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer to Data delay through the I/O interface
t _{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t _{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t _{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t _{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t _{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t _{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

IGLOO nano DC and Switching Characteristics

Applies to IGLOO nano at 1.2 V Core Operating Conditions

Table 2-26 • Summary of I/O Timing Characteristics—Software Default SettingsSTD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	teouт	top	t _{DIN}	t _P y)	teys	teour	tzı	tzH	tız	tHz	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
3.3 V LVCMOS Wide Range ²	100 µA	8 mA	High	5 pF	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
2.5 V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
1.8 V LVCMOS	4 mA	4 mA	High	5 pF	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns
1.5 V LVCMOS	2 mA	2 mA	High	5 pF	1.55	2.78	0.26	1.27	1.77	1.10	2.82	2.62	2.44	2.74	ns
1.2 V LVCMOS	1 mA	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns
1.2 V LVCMOS Wide Range ³	100 µA	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

Notes:

 The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.

3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V side range as specified in the JESD8-12 specification.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	0.97	3.52	0.19	0.86	1.16	0.66	3.59	3.42	1.75	1.90	ns
4 mA	STD	0.97	3.52	0.19	0.86	1.16	0.66	3.59	3.42	1.75	1.90	ns
6 mA	STD	0.97	2.90	0.19	0.86	1.16	0.66	2.96	2.83	1.98	2.29	ns
8 mA	STD	0.97	2.90	0.19	0.86	1.16	0.66	2.96	2.83	1.98	2.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T₁ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	0.97	2.16	0.19	0.86	1.16	0.66	2.20	1.80	1.75	1.99	ns
4 mA	STD	0.97	2.16	0.19	0.86	1.16	0.66	2.20	1.80	1.75	1.99	ns
6 mA	STD	0.97	1.79	0.19	0.86	1.16	0.66	1.83	1.45	1.98	2.38	ns
8 mA	STD	0.97	1.79	0.19	0.86	1.16	0.66	1.83	1.45	1.98	2.38	ns

Notes:

1. Software default selection highlighted in gray.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-47 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	0.97	4.13	0.19	1.10	1.24	0.66	4.01	4.13	1.73	1.74	ns
4 mA	STD	0.97	4.13	0.19	1.10	1.24	0.66	4.01	4.13	1.73	1.74	ns
8 mA	STD	0.97	3.39	0.19	1.10	1.24	0.66	3.31	3.39	1.98	2.19	ns
8 mA	STD	0.97	3.39	0.19	1.10	1.24	0.66	3.31	3.39	1.98	2.19	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-48 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	0.97	2.19	0.19	1.10	1.24	0.66	2.23	2.11	1.72	1.80	ns
4 mA	STD	0.97	2.19	0.19	1.10	1.24	0.66	2.23	2.11	1.72	1.80	ns
6 mA	STD	0.97	1.81	0.19	1.10	1.24	0.66	1.85	1.63	1.97	2.26	ns
8 mA	STD	0.97	1.81	0.19	1.10	1.24	0.66	1.85	1.63	1.97	2.26	ns

Notes:

1. Software default selection highlighted in gray.

IGLOO nano DC and Switching Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-49 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
4 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
6 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns
8 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-50 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
4 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
6 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
8 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns

Notes:

1. Software default selection highlighted in gray.

IGLOO nano DC and Switching Characteristics

1.2 V DC Core Voltage

Table 2-73 •Input Data Register Propagation Delays
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t _{ICLKQ}	Clock-to-Q of the Input Data Register	0.68	ns
t _{ISUD}	Data Setup Time for the Input Data Register	0.97	ns
t _{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t _{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
t _{IREMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
t _{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
t _{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
t _{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t _{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t _{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
t _{ICKMPWH}	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
t _{ICKMPWL}	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

IGLOO nano DC and Switching Characteristics



Figure 2-22 • Timing Model and Waveforms



IGLOO nano DC and Switching Characteristics

VersaTile Specifications as a Sequential Module

The IGLOO nano library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO*, *ProASIC3*, *SmartFusion and Fusion Macro Library Guide for Software v10.1*.



Figure 2-23 • Sample of Sequential Cells

Table 2-90 •AGLN020 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

		S	Std.	
Parameter	Description	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.21	1.55	ns
t _{RCKH}	Input High Delay for Global Clock	1.23	1.65	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.40		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.65		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-91 • AGLN060 Global Resource

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

		Std.		
Parameter	Description	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
t _{RCKH}	Input High Delay for Global Clock	1.34	1.71	ns
t _{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock	1.40		ns
t _{RCKMPWL}	Minimum Pulse Width LOW for Global Clock	1.65		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.38	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

IGLOO nano DC and Switching Characteristics

Table 2-103 • RAM512X18

Parameter	Description	Std.	Units
t _{AS}	Address setup time	0.69	ns
t _{AH}	Address hold time	0.13	ns
t _{ENS}	REN, WEN setup time	0.61	ns
t _{ENH}	REN, WEN hold time	0.07	ns
t _{DS}	Input data (WD) setup time	0.59	ns
t _{DH}	Input data (WD) hold time	0.30	ns
t _{CKQ1}	Clock HIGH to new data valid on RD (output retained)	3.51	ns
t _{CKQ2}	Clock HIGH to new data valid on RD (pipelined)	1.43	ns
t _{C2CRWH} 1	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t _{C2CWRH} 1	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.42	ns
t _{RSTBQ}	RESET Low to data out Low on RD (flow-through)	1.72	ns
	RESET Low to data out Low on RD (pipelined)	1.72	ns
t _{REMRSTB}	RESET removal	0.51	0.51
t _{RECRSTB}	RESET recovery	2.68	ns
t _{MPWRSTB}	RESET minimum pulse width	0.68	ns
t _{CYC}	Clock cycle time	6.24	ns
F _{MAX}	Maximum frequency	160	MHz

Notes:

1. For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.

IGLOO nano DC and Switching Characteristics

Table 2-105 • RAM512X18

Commercial-Case Conditions: T	J = 70°C, Worst-Case VCC	; = 1.14 V
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Parameter	Description	Std.	Units
t _{AS}	Address setup time	1.28	ns
t _{AH}	Address hold time	0.25	ns
t _{ENS}	REN, WEN setup time	1.13	ns
t _{ENH}	REN, WEN hold time	0.13	ns
t _{DS}	Input data (WD) setup time	1.10	ns
t _{DH}	Input data (WD) hold time	0.55	ns
t _{CKQ1}	Clock High to new data valid on RD (output retained)	6.56	ns
t _{CKQ2}	Clock High to new data valid on RD (pipelined)	2.67	ns
t _{C2CRWH} 1	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.87	ns
t _{C2CWRH} 1	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.04	ns
t _{RSTBQ}	RESET LOW to data out LOW on RD (flow through)	3.21	ns
	RESET LOW to data out LOW on RD (pipelined)	3.21	ns
t _{REMRSTB}	RESET removal	0.93	ns
t _{RECRSTB}	RESET recovery	4.94	ns
t _{MPWRSTB}	RESET minimum pulse width	1.18	ns
t _{CYC}	Clock cycle time	10.90	ns
F _{MAX}	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.



Datasheet Information

Revision / Version	Changes	Page
Revision 2 (Dec 2008) Product Brief Advance v0.4	The second table note in "IGLOO nano Devices" table was revised to state, "AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. AGLN030 and smaller devices do not support this feature."	II
	The I/Os per package for CS81 were revised to 60 for AGLN060, AGLN125, and AGLN250 in the "I/Os Per Package"table.	II
Packaging Advance v0.3	The "UC36" pin table is new.	4-2
Revision 1 (Nov 2008) Product Brief Advance v0.3	The "Advanced I/Os" section was updated to include wide power supply voltage support for 1.14 V to 1.575 V.	I
	The AGLN030 device was added to product tables and replaces AGL030 entries that were formerly in the tables.	VI
	The "I/Os Per Package"table was updated for the CS81 package to change the number of I/Os for AGLN060, AGLN125, and AGLN250 from 66 to 64.	
	The "Wide Range I/O Support" section is new.	1-8
	The table notes and references were revised in Table 2-2 • Recommended Operating Conditions ¹ . VMV was included with VCCI and a table note was added stating, "VMV pins must be connected to the corresponding VCCI pins. See <i>Pin Descriptions</i> for further information." Please review carefully.	2-2
	VJTAG was added to the list in the table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Flash*Freeze Mode*. Values were added for AGLN010, AGLN015, and AGLN030 for 1.5 V.	2-7
	VCCI was removed from the list in the table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode*.	2-8
	Values for I _{CCA} current were updated for AGLN010, AGLN015, and AGLN030 in Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode ¹ .	2-8
	Values for PAC1 and PAC2 were added to Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices and Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices.	2-10, 2-11
	Table notes regarding wide range support were added to Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels.	2-19
	1.2 V LVCMOS wide range values were added to Table 2-22 • Summary of Maximum and Minimum DC Input Levels and Table 2-23 • Summary of AC Measuring Points.	2-19, 2-20
	The following table note was added to Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings and Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings: "All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification."	2-21
	3.3 V LVCMOS Wide Range and 1.2 V Wide Range were added to Table 2-28 • I/O Output Buffer Maximum Resistances ¹ andTable 2-30 • I/O Short Currents IOSH/IOSL.	2-23, 2-24



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