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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str910faw32x6

List of tables

3.7 Non-volatile memories

There are two independent 32-bit wide burst Flash memories enabling true read-while-write operation. The Flash memories are single-voltage erase/program with 20 year minimum data retention and 100K minimum erase cycles. The primary Flash memory is much larger than the secondary Flash.

Both Flash memories are blank when devices are shipped from ST. The CPU can boot only from Flash memory (configurable selection of which Flash bank).

Flash memories are programmed half-word (16 bits) at a time, but are erased by sector or by full array.

3.7.1 Primary Flash memory

Using the STR91xFA device configuration software tool and 3rd party Integrated Developer Environments, it is possible to specify that the primary Flash memory is the default memory from which the CPU boots at reset, or otherwise specify that the secondary Flash memory is the default boot memory. This choice of boot memory is non-volatile and stored in a location that can be programmed and changed only by JTAG In-System Programming. See *Section 6: Memory mapping*, for more detail.

The primary Flash memory has equal length 64K byte sectors. See *Table 3* for number of sectors per device type.

Table 3. Sectoring of primary Flash memory

Size of primary Flash	256 Kbytes	512 Kbytes	1 Mbyte	2 Mbytes
Number of sectors	4	8	16	32
Size of each sector	64 Kbytes		64 Kbytes	

3.7.2 Secondary Flash memory

The smaller of the two Flash memories can be used to implement a bootloader, capable of storing code to perform robust In-Application Programming (IAP) of the primary Flash memory. The CPU executes code from the secondary Flash, while updating code in the primary Flash memory. New code for the primary Flash memory can be downloaded over any of the interfaces on the STR91xFA (USB, Ethernet, CAN, UART, etc.)

Additionally, the secondary Flash memory may also be used to store small data sets by emulating EEPROM through firmware, eliminating the need for external EEPROM memories. This raises the data security level because passcodes and other sensitive information can be securely locked inside the STR91xFA device.

The secondary Flash memory is sectored as shown in *Table 4* according to device type.

Both the primary Flash memory and the secondary Flash memory can be programmed with code and/or data using the JTAG In-System Programming (ISP) channel, totally independent of the CPU. This is excellent for iterative code development and for manufacturing.

3.16 Embedded trace module (ARM ETM9, v. r2p2)

The ETM9 interface provides greater visibility of instruction and data flow happening inside the CPU core by streaming compressed data at a very high rate from the STR91xFA though a small number of ETM9 pins to an external Trace Port Analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or other high-speed channel. Real-time instruction flow and data activity can be recorded and later formatted and displayed on the host computer running debugger software, and this software is typically integrated with the debug software used for EmbeddedICE-RT functions such as single-step, breakpoints, etc. Tracing may be triggered and filtered by many sources, such as instruction address comparators, data watchpoints, context ID comparators, and counters. State sequencing of up to three triggers is also provided. TPA hardware is commercially available and operates with debugging software tools.

The ETM9 interface is nine pins total, four of which are data lines, and all pins can be used for GPIO after tracing is no longer needed. The ETM9 interface is used in conjunction with the JTAG interface for trace configuration. When tracing begins, the ETM9 engine compresses the data by various means before broadcasting data at high speed to the TPA over the four data lines. The most common ETM9 compression technique is to only output address information when the CPU branches to a location that cannot be inferred from the source code. This means the host computer must have a static image of the code being executed for decompressing the ETM9 data. Because of this, self-modified code cannot be traced.

3.17 Ethernet MAC interface with DMA

STR91xFA devices in 128-pin and 144-ball packages provide an IEEE-802.3-2002 compliant Media Access Controller (MAC) for Ethernet LAN communications through an industry standard Medium Independent Interface (MII). The STR91xFA requires an external Ethernet physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the STR91xFA MII port using as many as 18 signals (see pins which have signal names MII_* in *Table 8*).

The MAC corresponds to the OSI Data Link layer and the PHY corresponds to the OSI Physical layer. The STR91xFA MAC is responsible for:

- Data encapsulation, including frame assembly before transmission, and frame parsing/error detection during and after reception.
- Media access control, including initiation of frame transmission and recover from transmission failure.

The STR91xFA MAC includes the following features:

- Supports 10 and 100 Mbps rates
- Tagged MAC frame support (VLAN support)
- Half duplex (CSMA/CD) and full duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. Transmit FIFO depth is 4 words (32 bits each), and the receive FIFO is 16 words deep.

A 32-bit burst DMA channel residing on the AHB is dedicated to the Ethernet MAC for high-speed data transfers, side-stepping the CPU for minimal CPU impact during transfers. This DMA channel includes the following features:

- Direct SRAM to MAC transfers of transmit frames with the related status, by descriptor chain
- Direct MAC to SRAM transfers of receive frames with the related status, by descriptor chain
- Open and Closed descriptor chain management

3.18 USB 2.0 slave device interface with DMA

The STR91xFA provides a USB slave controller that implements both the OSI Physical and Data Link layers for direct bus connection by an external USB host on pins USBDP and USBPN. The USB interface detects token packets, handles data transmission and reception, and processes handshake packets as required by the USB 2.0 standard.

The USB slave interface includes the following features:

- Supports USB low and full-speed transfers (12 Mbps), certified to comply with the USB 2.0 specification
- Supports isochronous, bulk, control, and interrupt endpoints
- Configurable number of endpoints allowing a mixture of up to 20 single-buffered monodirectional endpoints or up to 10 double-buffered bidirectional endpoints
- Dedicated, dual-port 2 Kbyte USB Packet Buffer SRAM. One port of the SRAM is connected by a Packet Buffer Interface (PBI) on the USB side, and the CPU connects to the other SRAM port.
- CRC generation and checking
- NRZI encoding-decoding and bit stuffing
- USB suspend resume operations

3.22.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service each SSP channel for fast and direct transfers between the SSP bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive. Burst transfers require that FIFOs are enabled.

3.23 General purpose I/O

There are up to 80 GPIO pins available on 10 I/O ports for 128-pin and 144-ball devices, and up to 40 GPIO pins on 5 I/O ports for 80-pin devices. Each and every GPIO pin by default (during and just after a reset condition) is in high-impedance input mode, and some GPIO pins are additionally routed to certain peripheral function inputs. CPU firmware may initialize GPIO pins to have alternate input or output functions as listed in *Table 8*. At any time, the logic state of any GPIO pin may be read by firmware as a GPIO input, regardless of its reassigned input or output function.

Bit masking is available on each port, meaning firmware may selectively read or write individual port pins, without disturbing other pins on the same port during a write.

Firmware may designate each GPIO pin to have open-drain or push-pull characteristics.

All GPIO pins are 5 V tolerant, meaning they can drive a voltage level up to VDDQ, and can be safely driven by a voltage up to 5 V.

3.24 A/D converter (ADC) with DMA

The STR91xFA provides an eight-channel, 10-bit successive approximation analog-to-digital converter. The ADC input pins are multiplexed with other functions on Port 4 as shown in *Table 8*. Following are the major ADC features:

- Fast conversion time, as low as 0.7 usec
- Accuracy. Integral and differential non-linearity are typically within 4 conversion counts.
- 0 to 3.6 V input range. External reference voltage input pin (AVREF) available on 128-pin packages for better accuracy on low-voltage inputs. See *Table 11: Operating conditions*, for restrictions to the relative voltage levels of VDDQ, AVDD, AVREF, and AVREF_AVDD.
- CPU Firmware may convert one ADC input channel at a time, or it has the option to set the ADC to automatically scan and convert all eight ADC input channels sequentially before signalling an end-of-conversion
- Automatic continuous conversion mode is available for any number of designated ADC input channels
- Analog watchdog mode provides automatic monitoring of any ADC input, comparing it against two programmable voltage threshold values. The ADC unit will set a flag or it will interrupt the CPU if the input voltage rises above the higher threshold, or drops below the lower threshold.
- The ADC unit goes to stand-by mode (very low-current consumption) after any reset event. CPU firmware may also command the ADC unit to stand-by mode at any time.
- ADC conversion can be started or triggered by software command as well as triggers from Timer/Counter (TIM), Motor Controller and input from external pin.

3.27 External memory interface (EMI)

STR91xFA devices in 128-pin and 144-ball packages offer an external memory bus for connecting external parallel peripherals and memories. The EMI bus resides on ports 7, 8, and 9 and operates with either an 8 or 16-bit data path. The configuration of 8 or 16 bit mode is specified by CPU firmware writing to configuration registers at run-time. If the application does not use the EMI bus, then these port pins may be used for general purpose I/O as shown in *Table 8*.

The EMI has the following features:

- Supports static asynchronous memory access cycles, including page mode for non-mux operation. The bus control signals include:
  - EMI_RDn - read signal, x8 or x16 mode
  - EMI_BWR_WRLn - write signal in x8 mode and write low byte signal in x16 mode
  - EMI_WRHn - write high byte signal in x16 mode
  - EMI_ALE - address latch signal for x8 or x16 mux bus mode with programmable polarity
- Four configurable memory regions, each with a chip select output (EMI_CS0n ... EMI_CS3n)
- Programmable wait states per memory region for both write and read operations
- ***16-bit multiplexed data mode*** (*Figure 4*): 16 bits of data and 16 bits of low-order address are multiplexed together on ports 8 and 9, while port 7 contains eight more high-order address signals. The output signal on pin EMI_ALE is used to demultiplex the signals on ports 8 and 9, and the polarity of EMI_ALE is programmable. The output signals on pins EMI_BWR_WRLn and EMI_WRHn are the write strobes for the low and high data bytes respectively. The output signal EMI_RDn is the read strobe for both the low and high data bytes.
- ***8-bit multiplexed data mode***: This is a variant of the 16-bit multiplexed mode. Although this mode can provide 24 bits of address and 8 bits of data, it does require an external latch device on Port 8. However, this mode is most efficient when connecting devices that only require 8 bits of address on an 8-bit multiplexed address/data bus, and have simple read, write, and latch inputs as shown in *Figure 5*

To use all 24 address bits, the following applies: 8 bits of lowest-order data and 8 bits of lowest-order address are multiplexed on port 8. On port 9, 8-bits of mid-order address are multiplexed with 8 bits of data, but these 8 data values are always at logic zero on this port during a write operation, and these 8 data bits are ignored during a read operation. An external latch device is needed to de-multiplex the mid-order 8 address bits that are generated on port 8. Port 7 outputs the 8 highest-order address signals directly (not multiplexed). The output signal on pin EMI_ALE is used to demultiplex the signals on ports 8 and 9, and the polarity of EMI_ALE is programmable. The output signal on pin

5.1 LFBGA144 ball connections

- In *Table 7* balls labelled NC are no connect balls. These NC balls are reserved for future devices and should NOT be connected to ground or any other signal. There are total of 9 NC (no connection) balls.
- Balls H1 and G4 are assigned as EMI bus write signals (EMI_BWR_WRLn and EMI_WRHn). These two balls can also be configured by the user as EMI low or high byte select signals (EMI_LBn and EMI_UBn).
- The PLLGND (B8) and PLLVDDQ (C9) balls can be connected to VSSQ and VDDQ.

Table 7. STR91x LFBGA144 ball connections

	A	B	C	D	E	F	G	H	J	K	L	M
1	P4.2	P7.2	NC	P7.0	VDDQ	P7.3	P7.4	EMI_WRHn (EMI_UBn)	VDDQ	PHYCLK_ P5.2(1)	P8.0	P2.2
2	AVREF	P4.1	P4.0	P7.1	P2.0	NC	P6.2	P5.3	P8.2	P8.3	VSSQ	P8.6
3	AVDD	P4.3	AVSS	NC	P2.1	VSS	P6.3	P8.1	P6.1	P2.3	P8.4	VBATT
4	P4.6	P4.5	P4.4	VSSQ	P5.0	VDD	EMI_BWR_ WRLn (EMI_LBn)	P6.0	P8.5	VSSQ	P2.4	X2_ RTC
5	P7.7	VDDQ	VSSQ	P4.7	P7.5	NC	VSSQ	VSS	P2.5	P8.7	VDDQ	X1_ RTC
6	JTMS	JTDO	JTDI	P1.7	P7.6	P5.1	P2.6	P9.4	P9.3	P9.2	VDD	P9.0
7	P1.5	P1.4	NC	VDD	VSS	P1.6	P6.5	VDDQ	VSSQ	P3.0	USBCLK _P2.7 (2)	P9.1
8	VSSQ	PLLVSSQ	P1.3	JRSTn	JTCK	VSSQ	P6.4	EMI_BAAn	P3.3	EMI_ WAITn	P9.5	EMI_ BCLK
9	RESET_ OUTn	P1.2	PLLVDDQ	VDDQ	P6.6	VDDQ	NC	P5.6	EMI_ RDn	P9.7	P3.4	P9.6
10	X1_CPU	P1.0	P1.1	USBDN(3)	TAMPER_ IN	NC	VSS	P0.4	EMI_ ALE	P0.1	P3.5	P3.1
11	X2_CPU	JRTCK	USBDP(2)	MII_ MDIO(3)	P0.6	P0.5	VDD	P5.5	P0.2	P3.7	P0.0	P3.2
12	EMI_ WEn	P0.7	RESET_ INn	P6.7	NC	NC	P5.7	P0.3	P5.4	VDDQ	VSSQ	P3.6

1. No PHYCLK function on STR910FAW devices.
2. No USBCLK function on STR910FAW devices.
3. NU (Not Used) on STR910FAW devices. D10 is not connected, C11 must be pulled up by a 1.5 kOhm resistor to VDDQ.

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	118	E6	P7.6	I/O	GPIO_7.6, GP Input, HiZ	EXINT30, External Intr	TIM3_ICAP1, Input Capture	GPIO_7.6, GP Output	8b) EMI_A6, 16b) EMI_A22	EMI_CS1n, EMI Chip Select
-	119	A5	P7.7	I/O	GPIO_7.7, GP Input, HiZ	EXINT31, External Intr	TIM3_ICAP2, Input Capture	GPIO_7.7, GP Output	EMI_CS0n, EMI chip select	16b) EMI_A23, 8b) EMI_A7
-	26	L1	P8.0	I/O	GPIO_8.0, GP Input, HiZ	-	-	GPIO_8.0, GP Output	8b) EMI_D0, 16b) EMI_AD0	-
-	28	H3	P8.1	I/O	GPIO_8.1, GP Input, HiZ	-	-	GPIO_8.1, GP Output	8b) EMI_D1, 16b) EMI_AD1	-
-	30	J2	P8.2	I/O	GPIO_8.2, GP Input, HiZ	-	-	GPIO_8.2, GP Output	8b) EMI_D2, 16b) EMI_AD2	-
-	32	K2	P8.3	I/O	GPIO_8.3, GP Input, HiZ	-	-	GPIO_8.3, GP Output	8b) EMI_D3, 16b) EMI_AD3	-
-	34	L3	P8.4	I/O	GPIO_8.4, GP Input, HiZ	-	-	GPIO_8.4, GP Output	8b) EMI_D4, 16b) EMI_AD4	-
-	36	J4	P8.5	I/O	GPIO_8.5, GP Input, HiZ	-	-	GPIO_8.5, GP Output	8b) EMI_D5, 16b) EMI_AD5	-
-	38	M2	P8.6	I/O	GPIO_8.6, GP Input, HiZ	-	-	GPIO_8.6, GP Output	8b) EMI_D6, 16b) EMI_AD6	-
-	44	K5	P8.7	I/O	GPIO_8.7, GP Input, HiZ	-	-	GPIO_8.7, GP Output	8b) EMI_D7, 16b) EMI_AD7	-
-	46	M6	P9.0	I/O	GPIO_9.0, GP Input, HiZ	-	-	GPIO_9.0, GP Output	8b) EMI_A8 16b) EMI_AD8	-
-	47	M7	P9.1	I/O	GPIO_9.1, GP Input, HiZ	-	-	GPIO_9.1, GP Output	8b) EMI_A9, 16b) EMI_AD9	-
-	50	K6	P9.2	I/O	GPIO_9.2, GP Input, HiZ	-	-	GPIO_9.2, GP Output	8b) EMI_A10, 16b)EMI_AD10	-
-	51	J6	P9.3	I/O	GPIO_9.3, GP Input, HiZ	-	-	GPIO_9.3, GP Output	8b) EMI_A11, 16b)EMI_AD11	-
-	52	H6	P9.4	I/O	GPIO_9.4, GP Input, HiZ	-	-	GPIO_9.4, GP Output	8b) EMI_A12, 16b)EMI_AD12	-
-	58	L8	P9.5	I/O	GPIO_9.5, GP Input, HiZ	-	-	GPIO_9.5, GP Output	8b) EMI_A13, 16b)EMI_AD13	-
-	62	M9	P9.6	I/O	GPIO_9.6, GP Input, HiZ	-	-	GPIO_9.6, GP Output	8b) EMI_A14, 16b)EMI_AD14	-
-	64	K9	P9.7	I/O	GPIO_9.7, GP Input, HiZ	-	-	GPIO_9.7, GP Output	8b) EMI_A15, 16b)EMI_AD15	-

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	21	G4	EMI_ BWR_ WRLn	O	EMI byte write strobe (8 bit mode) or low byte write strobe (16 bit mode) Can also be configured as EMI_LBn in BGA package	N/A				
-	22	H1	EMI_ WRHn	O	EMI high byte write strobe (16-bit mode) Can also be configured as EMI_UBn in BGA package	N/A				
-	74	J10	EMI_ALE	O	EMI address latch enable (mux mode)	N/A				
-	75	J9	EMI_ RDn	O	EMI read strobe	N/A				
-	-	H8	EMI_ BAAn	O	EMI Burst address advance	N/A				
-	-	K8	EMI_ WAITn	I	EMI Wait input for burst mode device	N/A				
-	-	M8	EMI_ BCLK	O	EMI bus clock	N/A				
-	-	A12	EMI_ WEn	O	EMI write enable	N/A				
-	91	E10	TAMPER _IN	I	Tamper detection input	N/A				
-	94	D11	MII_ MDIO	I/O	MAC/PHY management data line	N/A				
59	95	D10	USBDN	I/O	USB data (-) bus connect	N/A				
60	96	C11	USBDP	I/O	USB data (+) bus connect	N/A				
56	89	C12	RESET _INn	I	External reset input	N/A				
62	100	A9	RESET _OUTn	O	Global or System reset output	N/A				
65	104	A10	X1_CPU	I	CPU oscillator or crystal input	N/A				
64	103	A11	X2_CPU	O	CPU crystal connection	N/A				

6 Memory mapping

The ARM966E-S CPU addresses a single linear address space of 4 giga-bytes (2^{32}) from address 0x0000.0000 to 0xFFFF.FFFF as shown in *Figure 9*. Upon reset the CPU boots from address 0x0000.0000, which is chip-select zero at address zero in the Flash Memory Interface (FMI).

The Instruction TCM and Data TCM enable high-speed CPU operation without incurring any performance or power penalties associated with accessing the system buses (AHB and APB). I-TCM and D-TCM address ranges are shown at the bottom of the memory map in *Figure 9*.

6.1 Buffered and non-buffered writes

The CPU makes use of write buffers on the AHB and the D-TCM to decouple the CPU from any wait states associated with a write operation. The user may choose to use write with buffers on the AHB by setting bit 3 in control register CP15 and selecting the appropriate AHB address range when writing. By default at reset, buffered writes are disabled (bit 3 of CP15 is clear) and all AHB writes are non-buffered until enabled. *Figure 9* shows that most addressable items on the AHB are aliased at two address ranges, one for buffered writes and another for non-buffered writes. A buffered write will allow the CPU to continue program execution while the write-back is performed through a FIFO to the final destination on the AHB. If the FIFO is full, the CPU is stalled until FIFO space is available. A non-buffered write will impose an immediate delay to the CPU, but results in a direct write to the final AHB destination, ensuring data coherency. Read operations from AHB locations are always direct and never buffered.

6.2 System (AHB) and peripheral (APB) buses

The CPU will access SRAM, higher-speed peripherals (USB, Ethernet, Programmable DMA), and the external bus (EMI) on the AHB at their respective base addresses indicated in *Figure 9*. Lower-speed peripherals reside on the APB and are accessed using two separate AHB-to-APB bridge units (APB0 and APB1). These bridge units are essentially address windows connecting the AHB to the APB. To access an individual APB peripheral, the CPU will place an address on the AHB bus equal to the base address of the appropriate bridge unit APB0 or APB1, plus the offset of the particular peripheral, plus the offset of the individual data location within the peripheral. *Figure 9* shows the base addresses of bridge units APB0 and APB1, and also the base address of each APB peripheral. Please consult the STR91xFA Reference manual for the address of data locations within each individual peripheral.

6.3 SRAM

The SRAM is aliased at three separate address ranges as shown in *Figure 9*. When the CPU accesses SRAM starting at 0x0400.0000, the SRAM appears on the D-TCM. When CPU access starts at 0x4000.0000, SRAM appears in the buffered AHB range. Beginning at CPU address 0x5000.0000, SRAM is in non-buffered AHB range. The SRAM size must be specified by CPU intitialization firmware writing to a control register after any reset condition. Default SRAM size is 32K bytes, with option to set to 64K bytes on STR91xFAx3x devices, and to 96K bytes on STR91xFAx4x devices.

When other AHB bus masters (such as a DMA controller) write to SRAM, their access is never buffered. Only the CPU can make use of buffered AHB writes.

6.4 Two independent Flash memories

The STR91xFA has two independent Flash memories, the larger primary Flash and the small secondary Flash. It is possible for the CPU to erase/write to one of these Flash memories while simultaneously reading from the other.

One or the other of these two Flash memories may reside at the “boot” address position of 0x0000.0000 at power-up or at reset as shown in *Figure 9*. The default configuration is that the first sector of primary Flash memory is enabled and residing at the boot position, and the secondary Flash memory is disabled. This default condition may be optionally changed as described below.

6.4.1 Default configuration

When the primary Flash resides at boot position, typical CPU initialization firmware would set the start address and size of the main Flash memory, and go on to enable the secondary Flash, define it’s start address and size. Most commonly, firmware would place the secondary Flash start address at the location just after the end of the primary Flash memory. In this case, the primary Flash is used for code storage, and the smaller secondary Flash can be used for data storage (EEPROM emulation).

6.4.2 Optional configuration

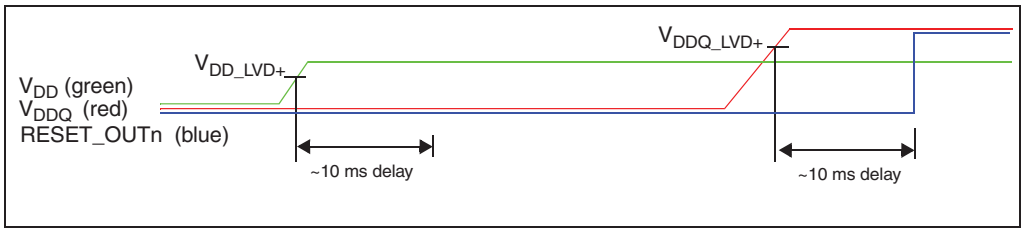
Using the STR91xFA device configuration software tool, or IDE from 3rd party, one can specify that the smaller secondary Flash memory is at the boot location at reset and the primary Flash is disabled. The selection of which Flash memory is at the boot location is programmed in a non-volatile Flash-based configuration bit during JTAG ISP. The boot selection choice will remain as the default until the bit is erased and re-written by the JTAG interface. The CPU cannot change this choice for boot Flash, only the JTAG interface has access.

In this case where the secondary Flash defaults to the boot location upon reset, CPU firmware would typically initialize the Flash memories the following way. The secondary Flash start address and size is specified, then the primary Flash is enabled and its start address and size is specified. The primary Flash start address would typically be located just after the final address location of the secondary Flash. This configuration is particularly well-suited for In-Application-Programming (IAP). The CPU would boot from the secondary Flash memory, initialize the system, then check the contents of the primary Flash memory (by checksum or other means). If the contents of primary Flash is OK, then CPU execution continues from either Flash memory.

7.5.1 LVD delay timing

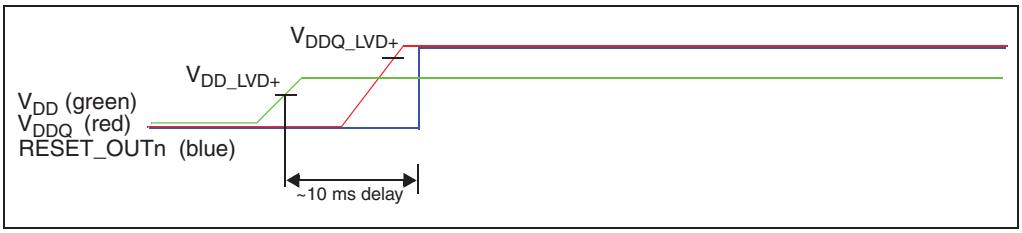
Case 1: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **after** the first ~10 ms delay (introduced by the VDD rising edge), a new ~10 ms delay starts before the release of RESET_OUTn. See *Figure 12.*

Figure 12. LVD reset delay case 1



Case 2: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **before** the first ~10 ms delay (introduced by the VDD rising edge), RESET_OUTn will be released immediately at the end of the delay. No new delay is introduced in this case. See *Figure 13.*

Figure 13. LVD reset delay case 2



Case 3: When V_{DD} reaches the V_{DD_LVD+} threshold **after** the V_{DDQ} rising edge, RESET_OUTn will be released at the end of a ~10 ms delay. See *Figure 14*

Figure 14. LVD reset delay case 3

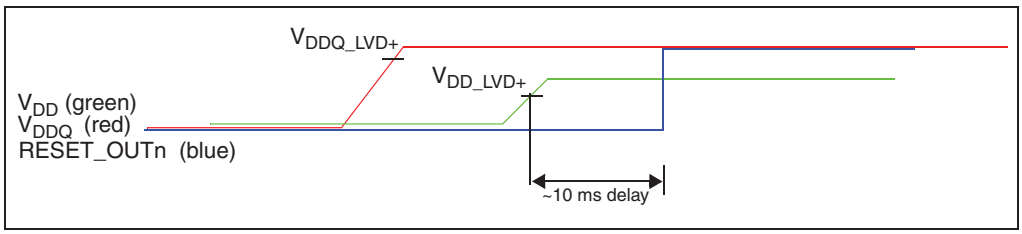
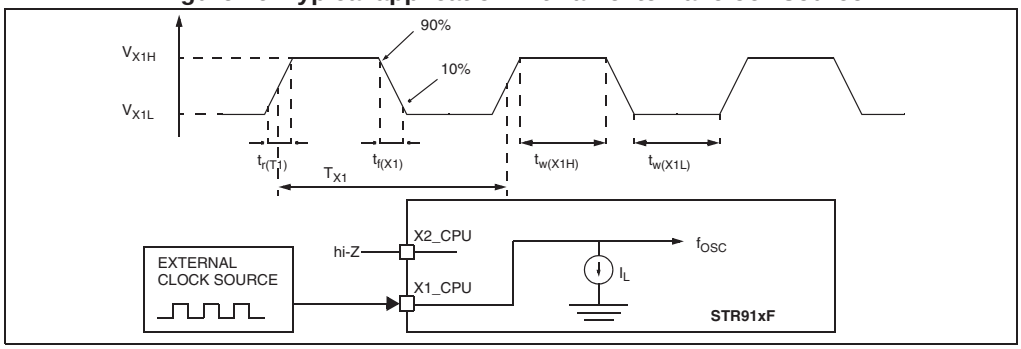


Figure 16. Typical application with an external clock source



7.7.3 RTC clock generated from a crystal/ceramic resonator

The RTC (Real-Time Clock) can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results obtained with typical external components specified in *Table 20* & *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 16 pF range, selected to match the requirements of the crystal or resonator. CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.

Load capacitance CL has the following formula:

CL = CL1 x CL2 / (CL1 + CL2) + Cstray

where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of CL = 6 pF, and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

Conditions: V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 20. RTC oscillator electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
R_F	External feedback resistor			22		MΩ
$V_{START(RTC)}$	Oscillator start voltage		V_{DD_LVD+} (1)			V
g_M	Oscillator transconductance(2)	Start-up	1.8			µA/Volts
$t_{STUP(RTC)}$	Oscillator Start-up Time(2)	V_{DD} stable			1	S

1. Refer to *Table 14* for min. value of V_{DD_LVD+}
2. Data based on bench measurements, not tested in production.

Table 25. Flash memory program/erase characteristics (Flash size = 1 MB / 2 MB)

Parameter		Test conditions	Value			Unit
			Typ(1)	Typ after 100K W/E cycles(1)	Max	
Bank erase	Primary bank (2 Mbytes)		32	36	46	s
	Primary bank (1 Mbytes)		16	18	23	s
	Secondary bank (128 Kbytes)		2.5	3	4	s
Sector erase	Of primary bank (64 Kbytes)		1300	1400	1800	ms
	Of secondary bank (16 Kbytes)		500	600	850	ms
Bank program	Primary bank (2 Mbytes)		15	20	22	s
	Primary bank (1 Mbytes)		7.5	10	11	s
	Secondary bank (128 Kbytes)		1060	1140	1380	ms
Sector program	Of primary bank (64 Kbytes)		500	520	640	ms
	Of secondary bank (16 Kbytes)		120	130	160	ms
Word program		Half word (16 bits)	8	9	11	µs

1. V_{DD} = 1.8 V, V_{DDQ} = 3.3 V, T_A = 2 5°C.

Table 26. Flash memory endurance

Parameter	Test conditions	Value			Unit
		Min	Typ	Max	
Program/erase cycles	Per word	100K			cycles
Data retention		20			years

Page mode read

Figure 22. Page mode read diagram

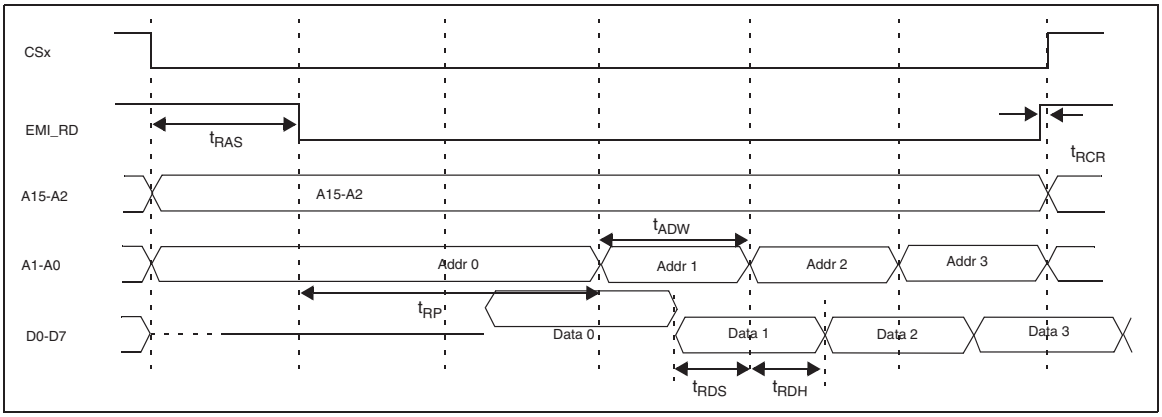
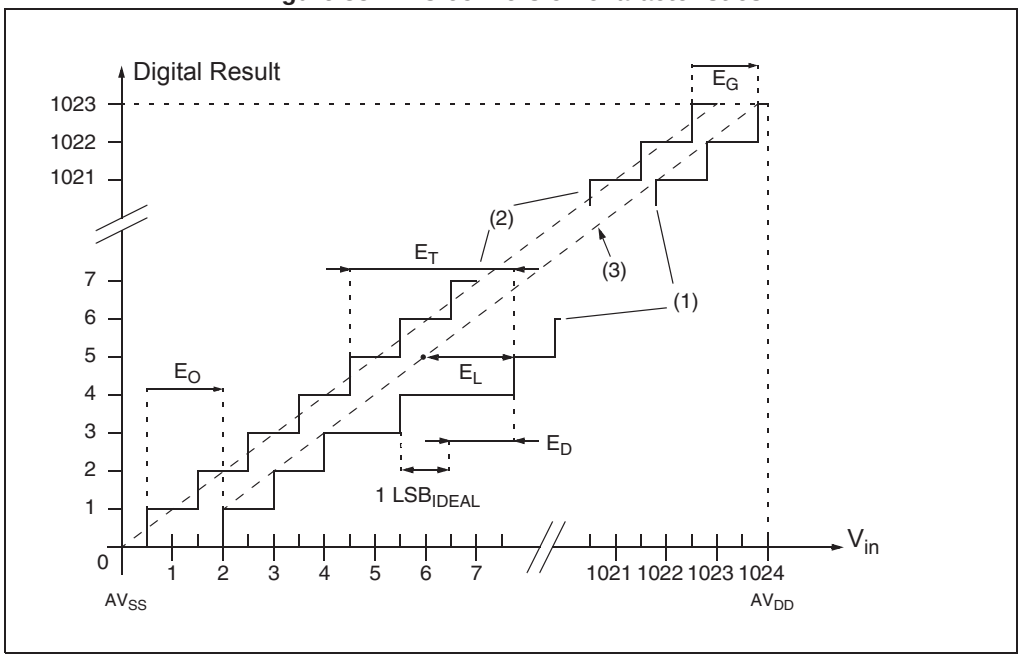


Table 37. Page mode read times

Symbol	Parameter	Value	
		Min	Max
t_{RDH}	Read data hold time	0	
t_{RDS}	Read data setup time	12 ns	-
t_{ADW}	ALE pulse width	(t_{BCLK}) - 1.5 ns	(t_{BCLK})+ 0.5 ns
t_{RAS}	Read address setup time	((WSTOEN) x t_{BCLK})	((WSTOEN) x t_{BCLK}) + 2.5 ns
t_{RP}	Read pulse width	((WSTRD-WSTOEN+1) x t_{BCLK})	((WSTRD-WSTOEN+1) x t_{BCLK}) + 2 ns
t_{RCR}	Read to CSn inactive	0	1 ns

Figure 33. ADC conversion characteristics



1. Legend:
   (1) Example of an actual transfer curve
   (2) The ideal transfer curve
   (3) End point correlation line
   E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset Error: deviation between the first actual transition and the first ideal one.
   E_G = Gain Error: deviation between the last ideal transition and the last actual one.
   E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Equation 1

$$1LSB_{IDEAL} = \frac{V_{DDA} - V_{SSA}}{1024}$$

8.2 STR91xFAx46 / STR91xFAx47

Figure 38. Device marking for revision A LQFP80 and LQFP128 packages

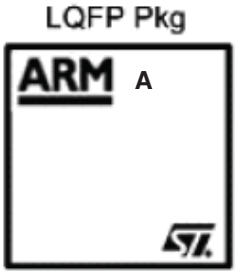


Figure 39. Device marking for revision A LFBGA144 packages

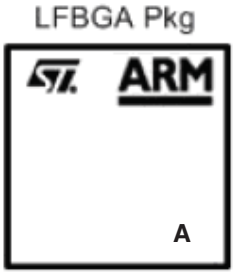
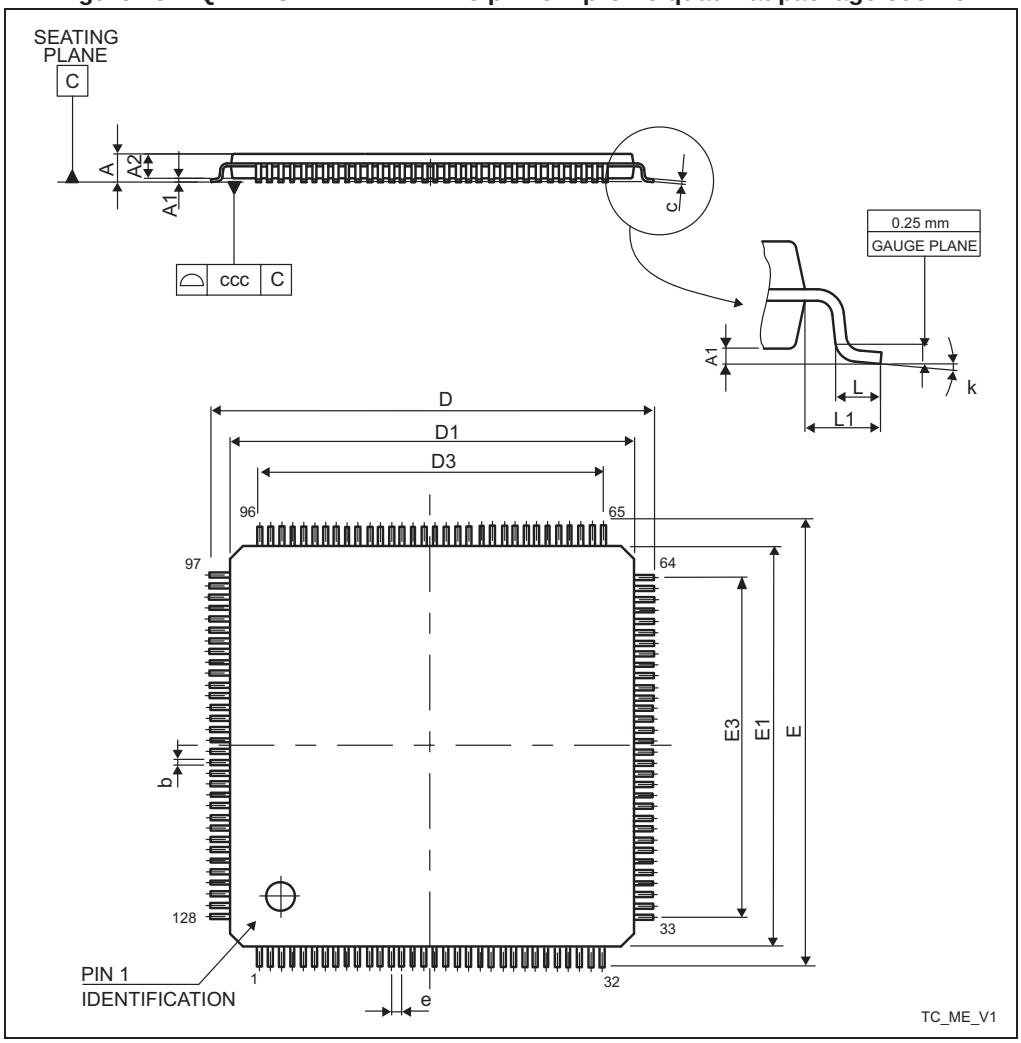


Figure 43. LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline

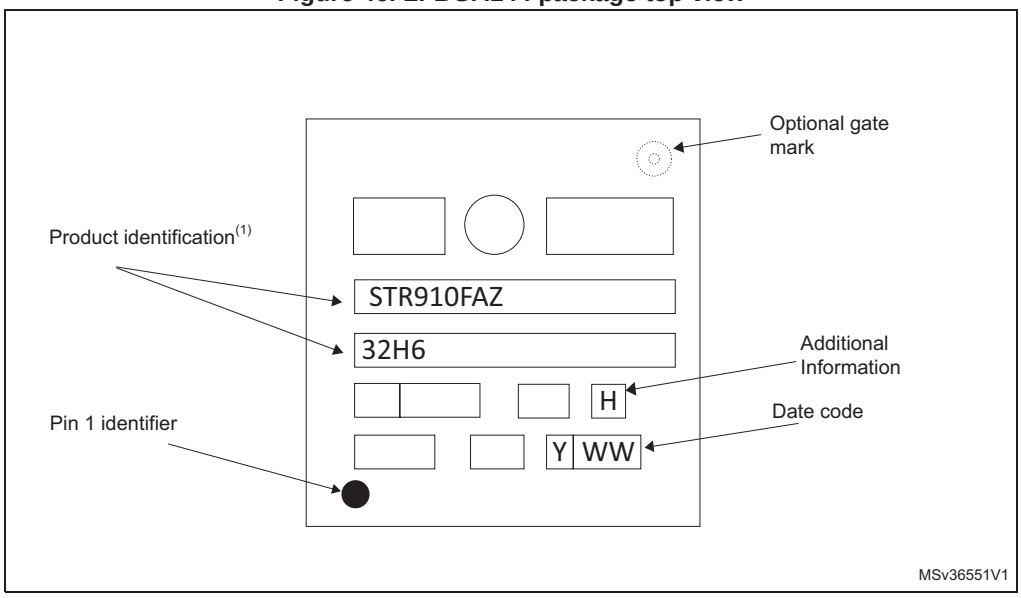


1. Drawing is not to scale.

Marking of engineering samples for LFBGA144

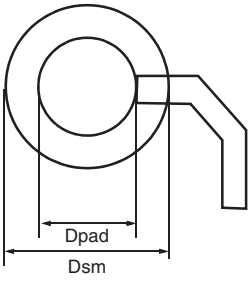
The following figure shows the engineering sample marking for the LFBGA package. Only the information field containing the engineering sample marking is shown.

Figure 46. LFBGA144 package top view



1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 47. Recommended PCB design rules (0.80/0.75 mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

9.1 ECOPACK

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions, and product status are available at *www.st.com*.

9.2 Thermal characteristics

The average chip-junction temperature, T_J must never exceed 125 °C.

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the power dissipation on input and output pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories. The worst case P_{INT} of the STR91xFA is 500 mW ($I_{DD} \times V_{DD}$, or 250 mA x 2.0 V).

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 53. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	***Thermal resistance junction-ambient*** LQFP 80 - 12 x 12 mm / 0.5 mm pitch	41.5	°C/W
Θ_{JA}	***Thermal resistance junction-ambient*** LQFP128 - 14 x 14 mm / 0.4 mm pitch	38	°C/W
Θ_{JA}	***Thermal resistance junction-ambient*** LFBGA 144 - 10 x 10 x 1.7 mm	36.5	°C/W