Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	40
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str911fam44x6t

List of tables

3.9 Vectored interrupt controller (VIC)

Interrupt management in the STR91xFA is implemented from daisy-chaining two standard ARM VIC units. This combined VIC has 32 prioritized interrupt request channels and generates two interrupt output signals to the CPU. The output signals are FIQ and IRQ, with FIQ having higher priority.

3.9.1 FIQ handling

FIQ (Fast Interrupt reQuest) is the only non-vectored interrupt and the CPU can execute an Interrupt Service Routine (ISR) directly without having to determine/prioritize the interrupt source, minimizing ISR latency. Typically only one interrupt source is assigned to FIQ. An FIQ interrupt has its own set of banked registers to minimize the time to make a context switch. Any of the 32 interrupt request input signals coming into the VIC can be assigned to FIQ.

3.9.2 IRQ handling

IRQ is a vectored interrupt and is the logical OR of all 32 interrupt request signals coming into the 32 IRQ channels. Priority of individual vectored interrupt requests is determined by hardware (IRQ channel Intr 0 is highest priority, IRQ channel Intr 31 is lowest).

However, inside the same VIC (primary or secondary VIC), CPU firmware may re-assign individual interrupt sources to individual hardware IRQ channels, meaning that firmware can effectively change interrupt priority levels as needed within the same VIC (from priority 0 to priority 16).

Note: VIC0 (primary VIC) interrupts always have higher priority than VIC1 (secondary VIC) interrupts

When the IRQ signal is activated by an interrupt request, VIC hardware will resolve the IRQ interrupt priority, then the ISR reads the VIC to determine both the interrupt source and the vector address to jump to the service code.

The STR91xFA has a feature to reduce ISR response time for IRQ interrupts. Typically, it requires two memory accesses to read the interrupt vector address from the VIC, but the STR91xFA reduces this to a single access by adding a 16th entry in the instruction branch cache, dedicated for interrupts. This 16th cache entry always holds the instruction that reads the interrupt vector address from the VIC, eliminating one of the memory accesses typically required in traditional ARM implementations.

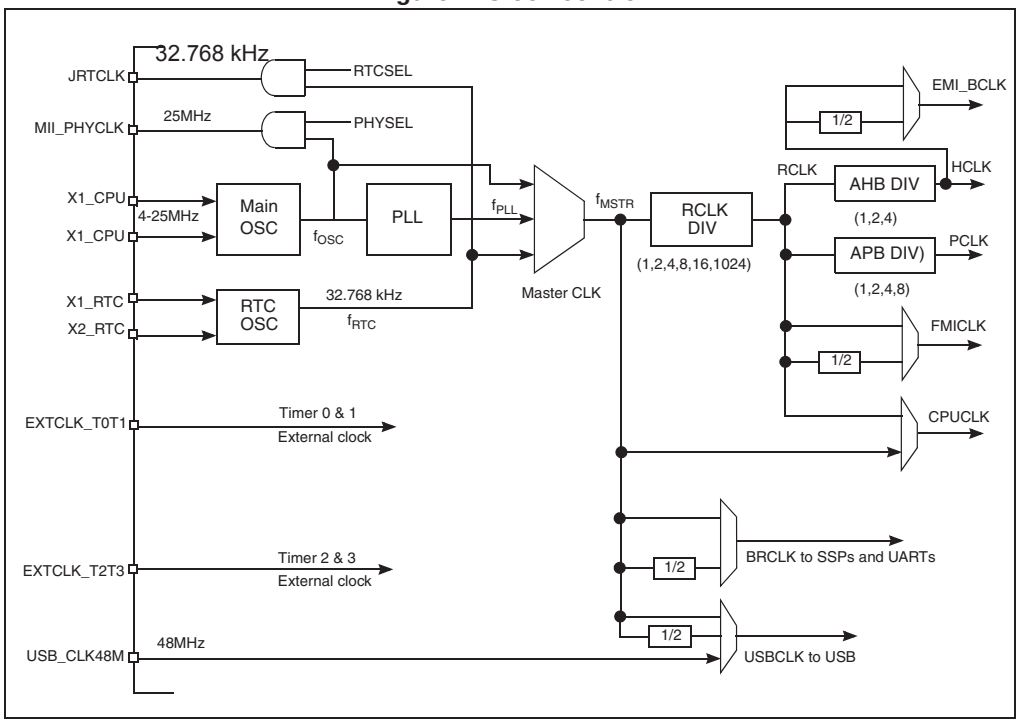
3.9.3 Interrupt sources

The 32 interrupt request signals coming into the VIC on 32 IRQ channels are from various sources; 5 from a wake-up unit and the remaining 27 come from internal sources on the STR91xFA such as on-chip peripherals, see *Table 6*. Optionally, firmware may force an interrupt on any IRQ channel.

One of the 5 interrupt requests generated by the wake-up unit (IRQ25 in *Table 6*) is derived from the logical OR of all 32 inputs to the wake-up unit. Any of these 32 inputs may be used to wake up the CPU and cause an interrupt. These 32 inputs consist of 30 external interrupts on selected and enabled GPIO pins, plus the RTC interrupt, and the USB Resume interrupt.

As an option, there are a number of peripherals that do not have to receive a clock sourced from the CCU. The USB interface can receive an external clock on pin P2.7, TIM timers TIM0/ TIM1 can receive an external clock on pin P2.4, and timers TIM2/TIM3 on pin P2.5.

Figure 2. Clock control



3.10.2 Reference clock (RCLK)

The main clock (f_{MSTR}) can be divided to operate at a slower frequency reference clock (RCLK) for the ARM core and all the peripherals. The RCLK provides the divided clock for the ARM core, and feeds the dividers for the AHB, APB, External Memory Interface, and FMI units.

3.10.3 AHB clock (HCLK)

The RCLK can be divided by 1, 2 or 4 to generate the AHB clock. The AHB clock is the bus clock for the AHB bus and all bus transfers are synchronized to this clock. The maximum HCLK frequency is 96 MHz.

3.10.4 APB clock (PCLK)

The RCLK can be divided by 1, 2, 4 or 8 to generate the APB clock. The APB clock is the bus clock for the APB bus and all bus transfers are synchronized to this clock. Many of the peripherals that are connected to the AHB bus also use the PCLK as the source for external bus data transfers. The maximum PCLK frequency is 48 MHz.

3.13.2 Supply voltage dropout

LVD circuitry will always cause a global reset if the CPU's V_{DD} source drops below it's fixed threshold of 1.4 V.

However, the LVD trigger threshold to cause a global reset for the I/O ring's V_{DDQ} source is set to one of two different levels, depending if V_{DDQ} will be operated in the range of 2.7 V to 3.3 V, or 3.0V to 3.6 V. If V_{DDQ} operation is at 2.7 V to 3.3 V, the LVD dropout trigger threshold is 2.4 V. If V_{DDQ} operation is 3.0 V and 3.6 V, the LVD threshold is 2.7 V. The choice of trigger level is made by STR91xFA device configuration software from STMicroelectronics or IDE from 3rd parties, and is programmed into the STR91xFA device along with other configurable items through the JTAG interface when the Flash memory is programmed.

CPU firmware may prevent some LVD resets if desired by writing a control register at run-time. Firmware may also disable the LVD completely for lowest-power operation when an external LVD device is being used.

3.13.3 Watchdog timer

The STR91xFA has a 16-bit down-counter (not one of the four TIM timers) that can be used as a watchdog timer or as a general purpose free-running timer/counter. The clock source is the peripheral clock from the APB, and an 8-bit clock pre-scaler is available. When enabled by firmware as a watchdog, this timer will cause a system reset if firmware fails to periodically reload this timer before the terminal count of 0x0000 occurs, ensuring firmware sanity. The watchdog function is off by default after a reset and must be enabled by firmware.

3.13.4 External RESET_INn pin

This input signal is active-low with hystereses (V_{HYS}). Other open-drain, active-low system reset signals on the circuit board (such as closure to ground from a push-button) may be connected directly to the RESET_INn pin, but an external pull-up resistor to V_{DDQ} must be present as there is no internal pullup on the RESET_INn pin.

A valid active-low input signal of t_{RINMIN} duration on the RESET_INn pin will cause a system reset within the STR91xFA. There is also a RESET_OUTn pin on the STR91xFA that can drive other system components on the circuit board. RESET_OUTn is active-low and has the same timing of the Power-On-Reset (POR) shown next, t_{POR}.

3.13.5 Power-up

The LVD circuitry will always generate a global reset when the STR91xFA powers up, meaning internal reset is active until V_{DDQ} and V_{DD} are both above the LVD thresholds. This POR condition has a duration of t_{POR}, after which the CPU will fetch its first instruction from address 0x0000.0000 in Flash memory. It is not possible for the CPU to boot from any other source other than Flash memory.

3.13.6 JTAG debug command

When the STR91xFA is in JTAG debug mode, an external device which controls the JTAG interface can command a system reset to the STR91xFA over the JTAG channel.

3.24.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service each ADC conversion result for fast DMA single-transfer.

3.25 Standard timers (TIM) with DMA

The STR91xFA has four independent, free-running 16-bit timer/counter modules designated TIM0, TIM1, TIM2, and TIM3. Each general purpose timer/counter can be configured by firmware for a variety of tasks including; pulse width and frequency measurement (input capture), generation of waveforms (output compare and PWM), event counting, delay timing, and up/down counting.

Each of the four timer units have the following features:

- 16-bit free running timer/counter
- Internal timer/counter clock source from a programmable 8-bit prescale of the CCU PCLK clock output
- Optional external timer/counter clock source from pin P2.4 shared by TIM0/TIM1, and pin P2.5 shared by TIM2/TIM3. Frequency of these external clocks must be at least 4 times less the frequency of the internal CCU PCLK clock output.
- Two dedicated 16-bit Input Capture registers for measuring up to two input signals. Input Capture has programmable selection of input signal edge detection
- Two dedicated 16-bit Output Compare registers for generation up to two output signals
- PWM output generation with 16-bit resolution of both pulse width and frequency
- One pulse generation in response to an external event
- A dedicated interrupt to the CPU with five interrupt flags
- The OCF1 flag (Output Compare 1) from the timer can be configured to trigger an ADC conversion

3.25.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service each timer/counter module TIM0 and TIM1 for fast and direct single transfers.

3.27 External memory interface (EMI)

STR91xFA devices in 128-pin and 144-ball packages offer an external memory bus for connecting external parallel peripherals and memories. The EMI bus resides on ports 7, 8, and 9 and operates with either an 8 or 16-bit data path. The configuration of 8 or 16 bit mode is specified by CPU firmware writing to configuration registers at run-time. If the application does not use the EMI bus, then these port pins may be used for general purpose I/O as shown in *Table 8*.

The EMI has the following features:

- Supports static asynchronous memory access cycles, including page mode for non-mux operation. The bus control signals include:
  - EMI_RDn - read signal, x8 or x16 mode
  - EMI_BWR_WRLn - write signal in x8 mode and write low byte signal in x16 mode
  - EMI_WRHn - write high byte signal in x16 mode
  - EMI_ALE - address latch signal for x8 or x16 mux bus mode with programmable polarity
- Four configurable memory regions, each with a chip select output (EMI_CS0n ... EMI_CS3n)
- Programmable wait states per memory region for both write and read operations
- ***16-bit multiplexed data mode*** (*Figure 4*): 16 bits of data and 16 bits of low-order address are multiplexed together on ports 8 and 9, while port 7 contains eight more high-order address signals. The output signal on pin EMI_ALE is used to demultiplex the signals on ports 8 and 9, and the polarity of EMI_ALE is programmable. The output signals on pins EMI_BWR_WRLn and EMI_WRHn are the write strobes for the low and high data bytes respectively. The output signal EMI_RDn is the read strobe for both the low and high data bytes.
- ***8-bit multiplexed data mode***: This is a variant of the 16-bit multiplexed mode. Although this mode can provide 24 bits of address and 8 bits of data, it does require an external latch device on Port 8. However, this mode is most efficient when connecting devices that only require 8 bits of address on an 8-bit multiplexed address/data bus, and have simple read, write, and latch inputs as shown in *Figure 5*

To use all 24 address bits, the following applies: 8 bits of lowest-order data and 8 bits of lowest-order address are multiplexed on port 8. On port 9, 8-bits of mid-order address are multiplexed with 8 bits of data, but these 8 data values are always at logic zero on this port during a write operation, and these 8 data bits are ignored during a read operation. An external latch device is needed to de-multiplex the mid-order 8 address bits that are generated on port 8. Port 7 outputs the 8 highest-order address signals directly (not multiplexed). The output signal on pin EMI_ALE is used to demultiplex the signals on ports 8 and 9, and the polarity of EMI_ALE is programmable. The output signal on pin

EMI_BWR_WRLn is the data write strobe, and the output on pin EMI_RDn is the data read strobe.

- ***8-bit non-multiplexed data mode*** (*Figure 6*): Eight bits of data are on port 8, while 16 bits of address are output on ports 7 and 9. The output signal on pin EMI_BWR_BWLn is the data write strobe and the output on pin EMI_RDn is the data read strobe.
- ***Burst Mode Support (LFBGA package only)*****:** The EMI bus supports synchronized burst read and write bus cycle in multiplexed and non-multiplexed mode. The additional EMI signals in the LFBGA package that support the burst mode are:
  - EMI_BCLK -the bus clock output. The EMI_BCLK has the same frequency or half of that of the HCLK and can be disabled by the user
  - EMI_WAITn - the not ready or wait input signal for synchronous access
  - EMI_BAAn - burst address advance or burst enable signal
  - EMI_WEn - write enable signal
  - EMI_UBn, EMI_LBn - upper byte and lower byte enable signals. These two signals share the same pins as the EMI_WRLn and EMI_WRHn and are user configurable through the EMI register.

  By defining the bus parameters such as burst length, burst type, read and write timings in the EMI control registers, the EMI bus is able to interface to standard burst memory devices. The burst timing specification and waveform will be provided in the next data sheet release

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	21	G4	EMI_ BWR_ WRLn	O	EMI byte write strobe (8 bit mode) or low byte write strobe (16 bit mode) Can also be configured as EMI_LBn in BGA package	N/A				
-	22	H1	EMI_ WRHn	O	EMI high byte write strobe (16-bit mode) Can also be configured as EMI_UBn in BGA package	N/A				
-	74	J10	EMI_ALE	O	EMI address latch enable (mux mode)	N/A				
-	75	J9	EMI_ RDn	O	EMI read strobe	N/A				
-	-	H8	EMI_ BAAn	O	EMI Burst address advance	N/A				
-	-	K8	EMI_ WAITn	I	EMI Wait input for burst mode device	N/A				
-	-	M8	EMI_ BCLK	O	EMI bus clock	N/A				
-	-	A12	EMI_ WEn	O	EMI write enable	N/A				
-	91	E10	TAMPER _IN	I	Tamper detection input	N/A				
-	94	D11	MII_ MDIO	I/O	MAC/PHY management data line	N/A				
59	95	D10	USBDN	I/O	USB data (-) bus connect	N/A				
60	96	C11	USBDP	I/O	USB data (+) bus connect	N/A				
56	89	C12	RESET _INn	I	External reset input	N/A				
62	100	A9	RESET _OUTn	O	Global or System reset output	N/A				
65	104	A10	X1_CPU	I	CPU oscillator or crystal input	N/A				
64	103	A11	X2_CPU	O	CPU crystal connection	N/A				

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	8	L2	VSSQ	G	Digital Ground for !/O and USB	N/A				
16	24	K4	VSSQ	G						
35	56	C5	VSSQ	G						
-	-	D4	VSSQ	G						
45	72	G5	VSSQ	G						
55	87	J7	VSSQ	G						
25	40	A8	VSSQ	G						
66	105	F8	VSSQ	G						
75	121	L12	VSSQ	G						
11	17	F4	VDD	V	V Source for CPU. 1.65 V - 2.0 V	N/A				
31	49	D7	VDD	V						
50	81	L6	VDD	V						
70	112	G11	VDD	V						
10	16	F3	VSS	G	Digital Ground for CPU	N/A				
30	48	H5	VSS	G						
51	82	G10	VSS	G						
71	113	E7	VSS	G						
-	-	C9	PLLV DDQ	V	V Source for PLL 2.7 to 3.6 V	N/A				
-	-	B8	PLLV SSQ	G	Digital Ground for PLL					

7.3 Operating conditions

Table 11. Operating conditions

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
V_{DD}	Digital CPU supply voltage	Flash size ≤512 KB	1.65	2.0	V
		Flash size = 1 MB / 2 MB, f_{CPUCLK} ≤85 MHz (1)	1.65	2.0	V
		Flash size = 1 MB / 2 MB, f_{CPUCLK} ≤96 MHz (2)	1.77	2.0	V
V_{DDQ}	Digital I/O supply voltage		2.7	3.6	V
V_{BATT}(3)	SRAM backup and RTC supply voltage		2.5	3.6	V
AV_{DD}	Analog ADC supply voltage (128-pin and 144-ball packages)		2.7	V_{DDQ}	V
AV_{REF}	Analog ADC reference voltage (128-pin and 144-ball packages)		2.65	AV_{DD}(4)	V
AV_{REF_AVDD}	Combined analog ADC reference and ADC supply voltage (80-pin package)		2.7	V_{DDQ}	V
T_A	Ambient temperature under bias		-40	+85	C

1. f_{FMICLK} ≤48 MHz during Flash write and 85 MHz during all other operations.
2. f_{FMICLK} ≤48 MHz during Flash write and 96 MHz during all other operations.
3. The V_{BATT} pin should be connected to V_{DDQ} if no battery is installed
4. AV_{REF} must never exceed V_{DDQ}

7.3.1 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Min(1)	Max(1)	Unit
t_{VDD}	V_{DD} rise time rate	10		µs/V
			10	ms/V

1. Data guaranteed by characterization, not tested in production.

7.7.1 Main oscillator electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 18. Main oscillator electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{STUP(OSC)}$	Oscillator Start-up Time	V_{DD} stable (1)		2	3	mS

1. Data characterized with quartz crystal, not tested in production.

7.7.2 X1_CPU external clock source

Subject to general operating conditions for V_{DD} and T_A.

Table 19. External clock characteristics

Symbol	Parameter	Test conditions(1)	Value			Unit
			Min	Typ	Max	
f_{X1}	External clock source frequency	See *Figure 16*	4		25	MHz
V_{X1H}	X1 input pin high level voltage		0.7xV_{DD}		V_{DD}	V
V_{X1L}	X1 input pin low level voltage		V_{SS}		0.3xV_{DD}	V
$t_{w(X1H)}$ $t_{w(X1L)}$	X1 high or low time(2)		6			ns
$t_{r(X1)}$ $t_{f(X1)}$	X1 rise or fall time(2)				20	ns
I_L	X1 input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
$C_{IN(X1)}$	X1 input capacitance(2)			5		pF
$DuCy_{(X1)}$	Duty cycle		45		55	%

1. Data based on typical appilcation software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Table 38. Sync burst write times

Symbol	Parameter	Value	
		Min	Max
t_{D1BAA}	BAA t_{D1}	0	2 ns
t_{D2BAA}	BAA t_{D2}	0.5 ns	2.5 ns
t_{D1ALE}	ALE t_{D1}	1 ns	3.5 ns
t_{D2ALE}	ALE t_{D2}	(t_{BCLK}/2) -0.5 ns	(t_{BCLK}/2) + 3.5 ns
t_{D1WR}	RD t_{D1}	0	2ns
t_{D2WR}	RD t_{D2}	0.5 ns	2.5 ns
t_{D1A}	Address t_{D1}	1.5 ns	4 ns
t_{D2A}	Address t_{D2}	2ns	4.5 ns
t_{D1CS}	CS t_{D1}	0.5ns	3 ns
t_{D2CS}	CS t_{D2}	1 ns	3.5 ns
t_{WS}	WAIT setup time	3 ns	6 ns
t_{DS}	Data setup time	(t_{BCLK}/2) -3.5 ns	(t_{BCLK}/2)+ 0.5 ns
t_{DH}	Data hold time	(t_{BCLK}/2) - 1 ns	(t_{BCLK}/2)+3.5 ns

Figure 31. SPI slave timing diagram with CPHA = 1

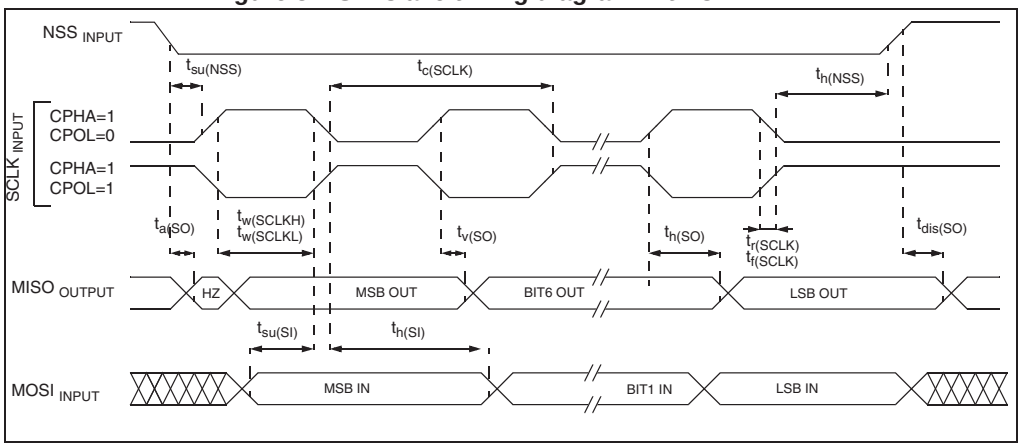
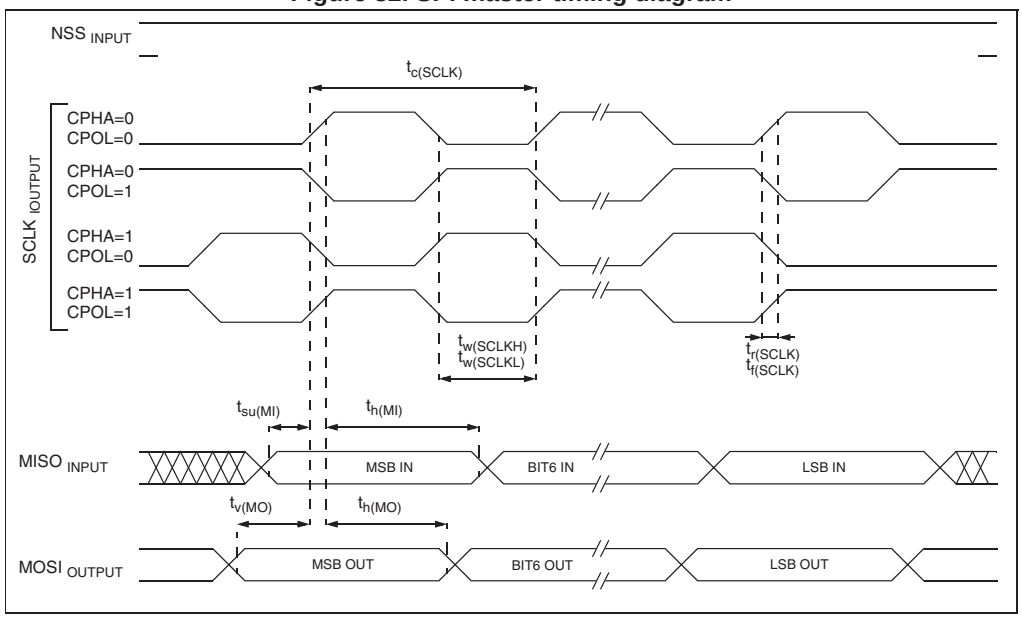


Figure 32. SPI master timing diagram



7.13 ADC electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 47. General ADC electrical characteristics

Symbol	Parameter[1]	Test conditions	Value			Unit
			Min	Typ	Max	
V_{AIN}	Input voltage range		0		AV_{REF}	V
RES	Resolution				10	Bits
N_{CH}	Number of input channels				8	N
f_{ADC}	ADC clock frequency				25	MHz
$t_{POR(ADC)}$	POR bit set to Standby mode				500	ms
$t_{ck\_off(ADC)}$	ADC clock disabled before conversion (2)				1	ms
t_{STAB}	Stabilization time				15	µs
C_{IN}	Input capacitance			5		pF
E_D	Differential non-linearity	(3) (4)		1	3	LSB[5]
E_L	Integral non-linearity	(3)		3	6	LSB[5]
E_O	Offset error	(3)		3	6	LSB[5]
E_G	Gain error	(3)		0.5	2	LSB[5]
E_T	Total unadjusted error	(3)		4	6	LSB[5]
I_{ADC}	Power consumption			4.6		mA
I_{VREF}	Current on VREF input pin	(6) (7)			920	µA

1. Guaranteed by design, not tested in production.
2. The ADC clock can be disabled by setting the ADC bit in the SCU_PCGR1 register or by setting the ACG bit in the SCU_GPIOANA register (for Rev H and higher)
3. Conditions: AV_{SS} = 0 V, AV_{DD} = 3.3 V f_{ADC} = 25 MHz.
4. The A/D is monotonic, there are no missing codes.
5. 1 LSB = (AV_{DD} - AV_{SS})/1024
6. Data based on characterization, not tested in production.
7. Conditions: V_{DD}=1.8 V, f_{CPU}=96 MHz , f_{ADC}=24 MHz

Table 48. ADC conversion time (silicon Rev G)

Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$2*16/f_{ADC}$		$3*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	1.33		2	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			500	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev G. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained on conversions started by trigger in single mode
4. All sucessive conversions in continuous and scan modes.

Table 49. ADC conversion time (silicon Rev H and higher)

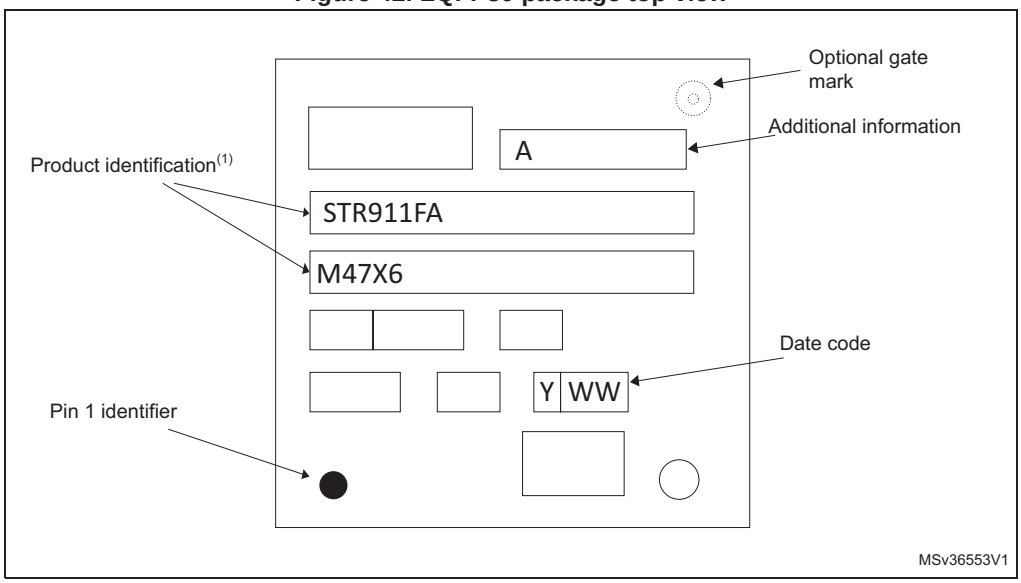
Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$1*16/f_{ADC}$		$2*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	0.66		1.33	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			750	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps
$t_{CONV(FT)}$	Fast trigger mode conversion time(5)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(FT)	Fast trigger mode throughput rate(6)	f_{ADC} = 24 MHz	100		1200	ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev H and higher. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained from conversions started by trigger in single mode
4. All successive conversions in continuous and scan modes.
5. Conversion started by trigger when automatic clock gated mode enabled. Fast trigger mode is available only in devices with silicon Rev H and higher.
6. Value obtained from conversions started by fast trigger in single mode

Marking of engineering samples for LQFP80

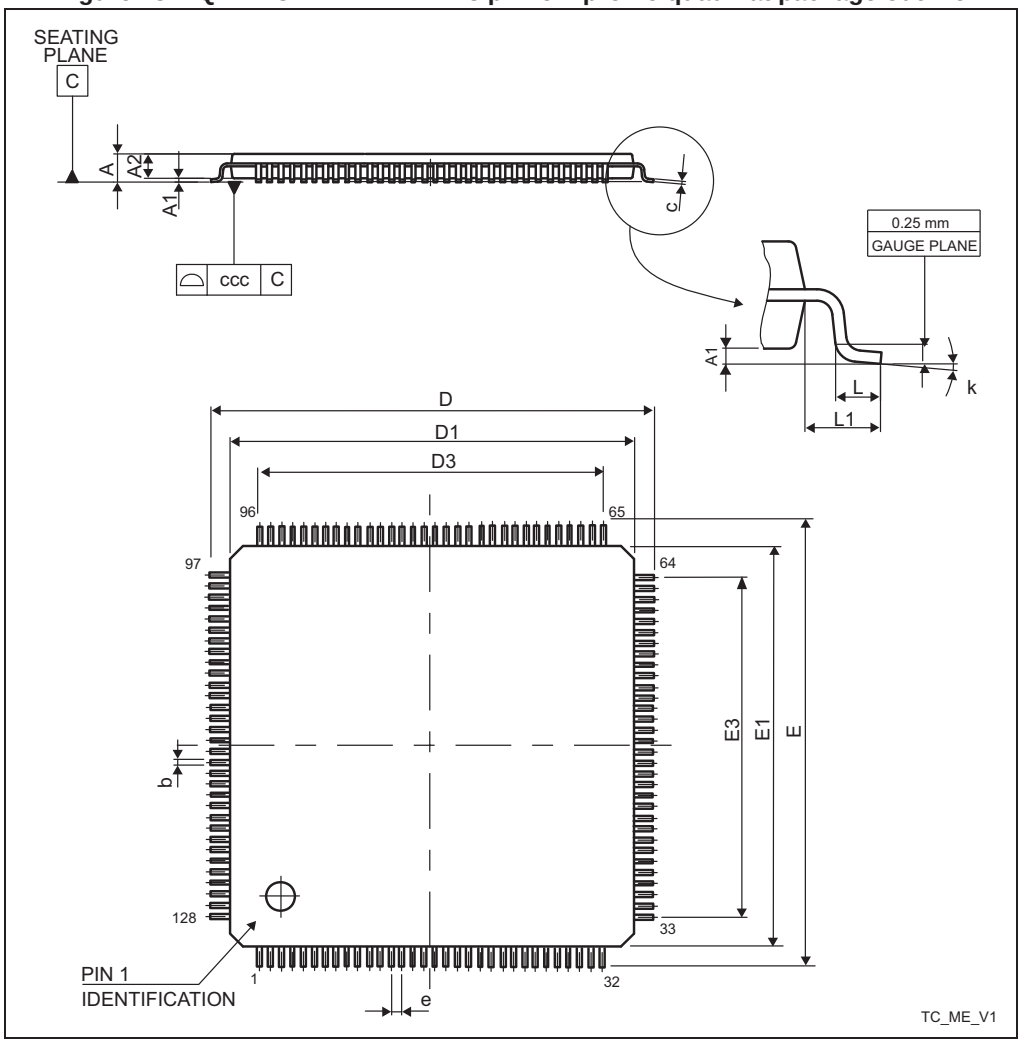
The following figure shows the engineering sample marking for the LQFP80 package. Only the information field containing the engineering sample marking is shown

Figure 42. LQFP80 package top view



1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 43. LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline

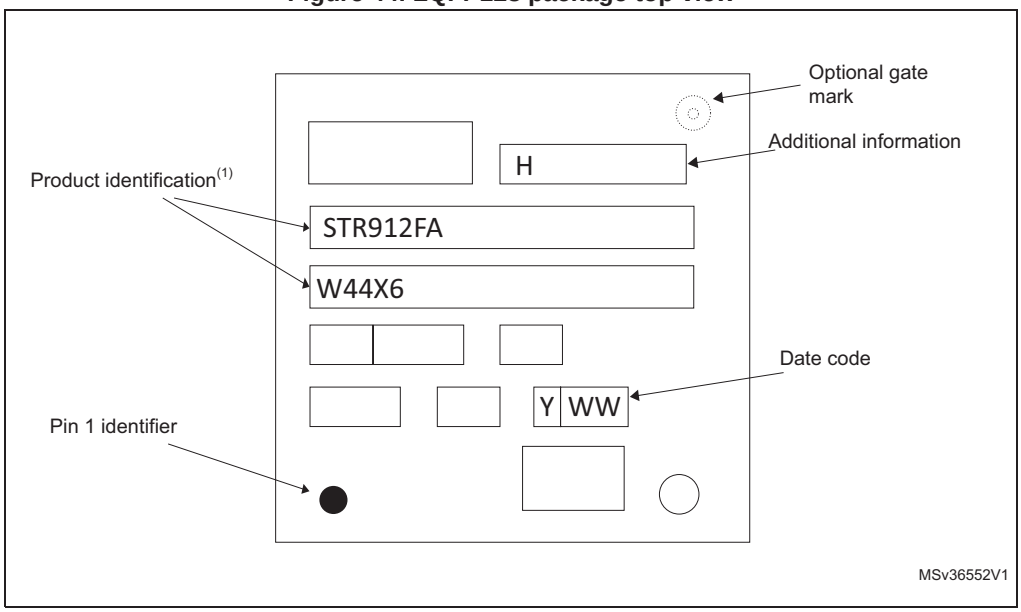


1. Drawing is not to scale.

Marking of engineering samples for LQFP128

The following figure shows the engineering sample marking for the LQFP128 package. Only the information field containing the engineering sample marking is shown.

Figure 44. LQFP128 package top view



1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 52.LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A[2]	-	-	1.700			0.0669
A1	0.210	-	-	0.0083		
A2	-	1.060	-		0.0417	
A3		0.026			0.0010	
A4	-	0.800	-	-	0.0315	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	8.800	-	-	0.3465	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	0.100			0.0039		
eee	0.150			0.0059		
fff	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.