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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	40
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str911fam47x6

1 Description

STR91xFA is a series of ARM®-powered microcontrollers which combines a 16/32-bit ARM966E-S RISC processor core, dual-bank Flash memory, large SRAM for data or code, and a rich peripheral set to form an ideal embedded controller for a wide variety of applications such as point-of-sale terminals, industrial automation, security and surveillance, vending machines, communication gateways, serial protocol conversion, and medical equipment. The ARM966E-S core can perform single-cycle DSP instructions, good for speech processing, audio algorithms, and low-end imaging.

3.5 SRAM (64 Kbytes or 96 Kbytes)

A 32-bit wide SRAM resides on the CPU's Data TCM (D-TCM) interface, providing single-cycle data accesses. As shown in *Figure 1*, the D-TCM shares SRAM access with the Advanced High-performance Bus (AHB). Sharing is controlled by simple arbitration logic to allow the DMA unit on the AHB to also access the SRAM.

3.5.1 Arbitration

Zero-wait state access occurs for either the D-TCM or the AHB when only one of the two is requesting SRAM. When both request SRAM simultaneously, access is granted on an interleaved basis so neither requestor is starved, granting one 32-bit word transfer to each requestor before relinquishing SRAM to the other. When neither the D-TCM or the AHB are requesting SRAM, the arbiter leaves access granted to the most recent user (if D-TCM was last to use SRAM then the D-TCM will not have to arbitrate to get access next time).

The CPU may execute code from SRAM through the AHB. There are no wait states as long as the D-TCM is not contending for SRAM access and the AHB is not sharing bandwidth with peripheral traffic. The ARM966E-S CPU core has a small pre-fetch queue built into this instruction path through the AHB to look ahead and fetch instructions during idle bus cycles.

3.5.2 Battery backup

When a battery is connected to the designated battery backup pin (VBATT), SRAM contents are automatically preserved when the operating voltage on the main digital supplies (VDD and VDDQ are lost or sag below the LVD threshold. Automatic switchover to SRAM can be disabled by firmware if it is desired that the battery will power only the RTC and not the SRAM during standby.

3.6 DMA data movement

DMA channels on the Advanced High-performance Bus (AHB) take full advantage of the separate data path provided by the Harvard architecture, moving data rapidly and largely independent of the instruction path. There are two DMA units, one is dedicated to move data between the Ethernet interface and SRAM, the other DMA unit has eight programmable channels with 14 request signals to service other peripherals and interfaces (USB, SSP, ADC, UART, Timers, EMI, and external request pins). Both single word and burst DMA transfers are supported. Memory-to-memory transfers are supported in addition to memory-peripheral transfers. DMA access to SRAM is shared with D-TCM accesses, and arbitration is described in *Section 3.5.1*. Efficient DMA transfers are managed by firmware using linked list descriptor tables. Of the 16 DMA request signals, two are assigned to external inputs. The DMA unit can move data between external devices and resources inside the STR91xFA through the EMI bus.

Table 4. Sectoring of secondary Flash memory

Size of secondary Flash	32 Kbytes	128 Kbytes
Number of sectors	4	8
Size of each sector	8 Kbytes	16 Kbytes

3.8 One-time-programmable (OTP) memory

There are 32 bytes of OTP memory ideally suited for serial numbers, security keys, factory calibration constants, or other permanent data constants. These OTP data bytes can be programmed only one time through either the JTAG interface or by the CPU, and these bytes can never be altered afterwards. As an option, a “lock bit” can be set by the JTAG interface or the CPU which will block any further writing to the this OTP area. The “lock bit” itself is also OTP. If the OTP array is unlocked, it is always possible to go back and write to an OTP byte location that has not been previously written, but it is never possible to change an OTP byte location if any one bit of that particular byte has been written before. The last two OTP bytes (bytes 31 and 30) are reserved for the STR91xFA product ID and revision level.

3.8.1 Product ID and revision level

OTP bytes 31 and 30 are programmed at ST factory before shipment and may be read by firmware to determine the STR91xFA product type and silicon revision so it can optionally take action based on the silicon on which it is running. In Rev H devices and 1MB/2MB Rev A devices, byte 31 contains the major family identifier of "9" (for STR9) in the high-nibble location and the minor family identifier in the low nibble location, which can be used to determine the size of primary flash memory. In all devices, byte 30 contains the silicon revision level indicator. See *Table 5* for values related to the revisions of STR9 production devices and size of primary Flash memory. See *Section 8* for details of external identification of silicon revisions.

Table 5. Product ID and revision level values

Production salestype	Silicon revision	Size of primary Flash	OTP byte 31	OTP byte 30
STR91xFAxxxxx	Rev G	256K or 512K	91h	20h
STR91xFAxxxxx	Rev H	256K	90h	21h
STR91xFAxxxxx	Rev H	512K	91h	21h
STR91xFAx46xx	Rev A	1024K	92h	21h
STR91xFAx47xx	Rev A	2048K	93h	21h

3.9 Vectored interrupt controller (VIC)

Interrupt management in the STR91xFA is implemented from daisy-chaining two standard ARM VIC units. This combined VIC has 32 prioritized interrupt request channels and generates two interrupt output signals to the CPU. The output signals are FIQ and IRQ, with FIQ having higher priority.

3.9.1 FIQ handling

FIQ (Fast Interrupt reQuest) is the only non-vectored interrupt and the CPU can execute an Interrupt Service Routine (ISR) directly without having to determine/prioritize the interrupt source, minimizing ISR latency. Typically only one interrupt source is assigned to FIQ. An FIQ interrupt has its own set of banked registers to minimize the time to make a context switch. Any of the 32 interrupt request input signals coming into the VIC can be assigned to FIQ.

3.9.2 IRQ handling

IRQ is a vectored interrupt and is the logical OR of all 32 interrupt request signals coming into the 32 IRQ channels. Priority of individual vectored interrupt requests is determined by hardware (IRQ channel Intr 0 is highest priority, IRQ channel Intr 31 is lowest).

However, inside the same VIC (primary or secondary VIC), CPU firmware may re-assign individual interrupt sources to individual hardware IRQ channels, meaning that firmware can effectively change interrupt priority levels as needed within the same VIC (from priority 0 to priority 16).

Note: VIC0 (primary VIC) interrupts always have higher priority than VIC1 (secondary VIC) interrupts

When the IRQ signal is activated by an interrupt request, VIC hardware will resolve the IRQ interrupt priority, then the ISR reads the VIC to determine both the interrupt source and the vector address to jump to the service code.

The STR91xFA has a feature to reduce ISR response time for IRQ interrupts. Typically, it requires two memory accesses to read the interrupt vector address from the VIC, but the STR91xFA reduces this to a single access by adding a 16th entry in the instruction branch cache, dedicated for interrupts. This 16th cache entry always holds the instruction that reads the interrupt vector address from the VIC, eliminating one of the memory accesses typically required in traditional ARM implementations.

3.9.3 Interrupt sources

The 32 interrupt request signals coming into the VIC on 32 IRQ channels are from various sources; 5 from a wake-up unit and the remaining 27 come from internal sources on the STR91xFA such as on-chip peripherals, see *Table 6*. Optionally, firmware may force an interrupt on any IRQ channel.

One of the 5 interrupt requests generated by the wake-up unit (IRQ25 in *Table 6*) is derived from the logical OR of all 32 inputs to the wake-up unit. Any of these 32 inputs may be used to wake up the CPU and cause an interrupt. These 32 inputs consist of 30 external interrupts on selected and enabled GPIO pins, plus the RTC interrupt, and the USB Resume interrupt.

Table 6. VIC IRQ channels (continued)

IRQ channel hardware priority	VIC input channel	Logic block	Interrupt source
25	VIC1.9	Wake-Up (all)	Logic OR of all 32 inputs of Wake-Up unit (30 pins, RTC, and USB Resume)
26	VIC1.10	Wake-up Group 0	Logic OR of 8 interrupt sources: RTC, USB Resume, pins P3.2 to P3.7
27	VIC1.11	Wake-up Group 1	Logic OR of 8 interrupts from pins P5.0 to P5.7
28	VIC1.12	Wake-up Group 2	Logic OR of 8 interrupts from pins P6.0 to P6.7
29	VIC1.13	Wake-up Group 3	Logic OR of 8 interrupts from pins P7.0 to P7.7
30	VIC1.14	USB	USB Bus Resume Wake-up (also input to wake-up unit)
31 (low priority)	VIC1.15	PFQ-BC	Special use of interrupts from Prefetch Queue and Branch Cache

3.10 Clock control unit (CCU)

The CCU generates a master clock of frequency f_{MSTR}. From this master clock the CCU also generates individually scaled and gated clock sources to each of the following functional blocks within the STR91xFA.

- CPU, f_{CPUCLK}
- Advanced High-performance Bus (AHB), f_{HCLK}
- Advanced Peripheral Bus (APB), f_{PCLK}
- Flash Memory Interface (FMI), f_{FMICLK}
- External Memory Interface (EMI), f_{BCLK}
- UART Baud Rate Generators, f_{BAUD}
- USB, f_{USB}

3.10.1 Master clock sources

The master clock in the CCU (f_{MSTR}) is derived from one of three clock input sources. Under firmware control, the CPU can switch between the three CCU inputs without introducing any glitches on the master clock output. Inputs to the CCU are:

- Main Oscillator (f_{OSC}). The source for the main oscillator input is a 4 to 25 MHz external crystal connected to STR91xFA pins X1_CPU and X2_CPU, or an external oscillator device connected to pin X1_CPU.
- PLL (f_{PLL}). The PLL takes the 4 to 25 MHz oscillator clock as input and generates a master clock output up to 96 MHz (programmable). By default, at power-up the master clock is sourced from the main oscillator until the PLL is ready (locked) and then the CPU may switch to the PLL source under firmware control. The CPU can switch back to the main oscillator source at any time and turn off the PLL for low-power operation. The PLL is always turned off in Sleep mode.
- RTC (f_{RTC}). A 32.768 kHz external crystal can be connected to pins X1_RTC and X2_RTC, or an external oscillator connected to pin X1_RTC to constantly run the real-time clock unit. This 32.768 kHz clock source can also be used as an input to the CCU to run the CPU in slow clock mode for reduced power.

3.13.2 Supply voltage dropout

LVD circuitry will always cause a global reset if the CPU's V_{DD} source drops below it's fixed threshold of 1.4 V.

However, the LVD trigger threshold to cause a global reset for the I/O ring's V_{DDQ} source is set to one of two different levels, depending if V_{DDQ} will be operated in the range of 2.7 V to 3.3 V, or 3.0V to 3.6 V. If V_{DDQ} operation is at 2.7 V to 3.3 V, the LVD dropout trigger threshold is 2.4 V. If V_{DDQ} operation is 3.0 V and 3.6 V, the LVD threshold is 2.7 V. The choice of trigger level is made by STR91xFA device configuration software from STMicroelectronics or IDE from 3rd parties, and is programmed into the STR91xFA device along with other configurable items through the JTAG interface when the Flash memory is programmed.

CPU firmware may prevent some LVD resets if desired by writing a control register at run-time. Firmware may also disable the LVD completely for lowest-power operation when an external LVD device is being used.

3.13.3 Watchdog timer

The STR91xFA has a 16-bit down-counter (not one of the four TIM timers) that can be used as a watchdog timer or as a general purpose free-running timer/counter. The clock source is the peripheral clock from the APB, and an 8-bit clock pre-scaler is available. When enabled by firmware as a watchdog, this timer will cause a system reset if firmware fails to periodically reload this timer before the terminal count of 0x0000 occurs, ensuring firmware sanity. The watchdog function is off by default after a reset and must be enabled by firmware.

3.13.4 External RESET_INn pin

This input signal is active-low with hystereses (V_{HYS}). Other open-drain, active-low system reset signals on the circuit board (such as closure to ground from a push-button) may be connected directly to the RESET_INn pin, but an external pull-up resistor to V_{DDQ} must be present as there is no internal pullup on the RESET_INn pin.

A valid active-low input signal of t_{RINMIN} duration on the RESET_INn pin will cause a system reset within the STR91xFA. There is also a RESET_OUTn pin on the STR91xFA that can drive other system components on the circuit board. RESET_OUTn is active-low and has the same timing of the Power-On-Reset (POR) shown next, t_{POR}.

3.13.5 Power-up

The LVD circuitry will always generate a global reset when the STR91xFA powers up, meaning internal reset is active until V_{DDQ} and V_{DD} are both above the LVD thresholds. This POR condition has a duration of t_{POR}, after which the CPU will fetch its first instruction from address 0x0000.0000 in Flash memory. It is not possible for the CPU to boot from any other source other than Flash memory.

3.13.6 JTAG debug command

When the STR91xFA is in JTAG debug mode, an external device which controls the JTAG interface can command a system reset to the STR91xFA over the JTAG channel.

3.20 UART interfaces with DMA

The STR91xFA supports three independent UART serial interfaces, designated UART0, UART1, and UART2. Each interface is very similar to the industry-standard 16C550 UART device. All three UART channels support IrDA encoding/decoding, requiring only an external LED transceiver to pins UARTx_RX and UARTx_Tx for communication. One UART channel (UART0) supports full modem control signals.

UART interfaces include the following features:

- Maximum baud rate of 1.5 Mbps
- Separate FIFOs for transmit and receive, each 16 deep, each FIFO can be disabled by firmware if desired
- Programmable FIFO trigger levels between 1/8 and 7/8
- Programmable baud rate generator based on CCU master clock, or CCU master clock divided by two
- Programmable serial data lengths of 5, 6, 7, or 8 bits with start bit and 1 or 2 stop bits
- Programmable selection of even, odd, or no-parity bit generation and detection
- False start-bit detection
- Line break generation and detection
- Support of IrDA SIR ENDEC functions for data rates of up to 115.2K bps
- IrDA bit duration selection of 3/16 or low-power (1.14 to 2.23 µsec)
- Channel UART0 supports modem control functions CTS, DCD, DSR, RTS, DTR, and RI

For your reference, only two standard 16550 UART features are not supported, 1.5 stop bits and independent receive clock.

3.20.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service channels UART0 and UART1 for fast and direct transfers between the UART bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive. Burst transfers require that UART FIFOs are enabled.

3.21 I^2C interfaces

The STR91xFA supports two independent I2C serial interfaces, designated I2C0, and I2C1. Each interface allows direct connection to an I2C bus as either a bus master or bus slave device (firmware configurable). I2C is a two-wire communication channel, having a bi-directional data signal and a single-directional clock signal based on open-drain line drivers, requiring external pull-up resistors.

Byte-wide data is transferred between a Master device and a Slave device on two wires. More than one bus Master is allowed, but only one Master may control the bus at any given time. Data is not lost when another Master requests the use of a busy bus because I2C supports collision detection and arbitration. More than one Slave device may be present on the bus, each having a unique address. The bus Master initiates all data movement and generates the clock that permits the transfer. Once a transfer is initiated by the Master, any device that is addressed is considered a Slave. Automatic clock synchronization allows I2C devices with different bit rates to communicate on the same physical bus.

3.27 External memory interface (EMI)

STR91xFA devices in 128-pin and 144-ball packages offer an external memory bus for connecting external parallel peripherals and memories. The EMI bus resides on ports 7, 8, and 9 and operates with either an 8 or 16-bit data path. The configuration of 8 or 16 bit mode is specified by CPU firmware writing to configuration registers at run-time. If the application does not use the EMI bus, then these port pins may be used for general purpose I/O as shown in *Table 8*.

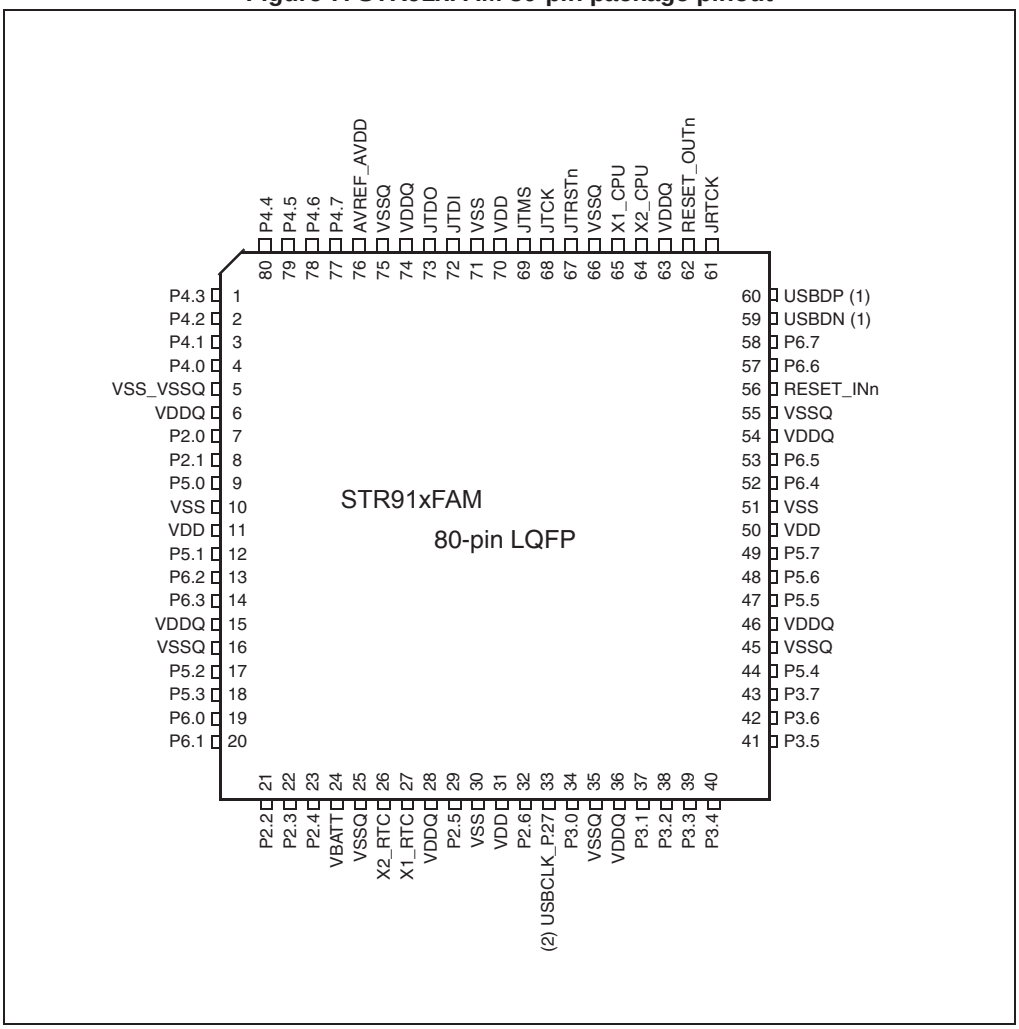
The EMI has the following features:

- Supports static asynchronous memory access cycles, including page mode for non-mux operation. The bus control signals include:
  - EMI_RDn - read signal, x8 or x16 mode
  - EMI_BWR_WRLn - write signal in x8 mode and write low byte signal in x16 mode
  - EMI_WRHn - write high byte signal in x16 mode
  - EMI_ALE - address latch signal for x8 or x16 mux bus mode with programmable polarity
- Four configurable memory regions, each with a chip select output (EMI_CS0n ... EMI_CS3n)
- Programmable wait states per memory region for both write and read operations
- ***16-bit multiplexed data mode*** (*Figure 4*): 16 bits of data and 16 bits of low-order address are multiplexed together on ports 8 and 9, while port 7 contains eight more high-order address signals. The output signal on pin EMI_ALE is used to demultiplex the signals on ports 8 and 9, and the polarity of EMI_ALE is programmable. The output signals on pins EMI_BWR_WRLn and EMI_WRHn are the write strobes for the low and high data bytes respectively. The output signal EMI_RDn is the read strobe for both the low and high data bytes.
- ***8-bit multiplexed data mode***: This is a variant of the 16-bit multiplexed mode. Although this mode can provide 24 bits of address and 8 bits of data, it does require an external latch device on Port 8. However, this mode is most efficient when connecting devices that only require 8 bits of address on an 8-bit multiplexed address/data bus, and have simple read, write, and latch inputs as shown in *Figure 5*

To use all 24 address bits, the following applies: 8 bits of lowest-order data and 8 bits of lowest-order address are multiplexed on port 8. On port 9, 8-bits of mid-order address are multiplexed with 8 bits of data, but these 8 data values are always at logic zero on this port during a write operation, and these 8 data bits are ignored during a read operation. An external latch device is needed to de-multiplex the mid-order 8 address bits that are generated on port 8. Port 7 outputs the 8 highest-order address signals directly (not multiplexed). The output signal on pin EMI_ALE is used to demultiplex the signals on ports 8 and 9, and the polarity of EMI_ALE is programmable. The output signal on pin

5 Pin description

Figure 7. STR91xFAM 80-pin package pinout



1. NU (Not Used) on STR910FAM devices. Pin 59 is not connected, pin 60 must be pulled up by a 1.5Kohm resistor to VDDQ.
2. No USBCLK function on STR910FAM devices.

5.2 Default pin functions

During and just after reset, all pins on ports 0-9 default to high-impedance input mode until CPU firmware assigns other functions to the pins. This initial input mode routes all pins on ports 0-9 to be read as GPIO inputs as shown in the “Default Pin Function” column of *Table 8*. Simultaneously, certain port pin signals are also routed to other functional inputs as shown in the “Default Input Function” column of *Table 8*, and these pin input functions will remain until CPU firmware makes other assignments. At any time, even after the CPU assigns pins to alternate functions, the CPU may always read the state of any pin on ports 0-9 as a GPIO input. CPU firmware may assign alternate functions to port pins as shown in columns “Alternate Input 1” or “Alternate Output 1, 2, 3” of *Table 8* by writing to control registers at run-time.

5.2.1 General notes on pin usage

1 *Since there are no internal or programmable pull-up resistors on ports 0-9, it is advised to pull down to ground, or pull up to VDDQ (using max. 47 KΩ resistors), all unused pins on port 0-9. Another solution is to use the GPIO control registers to configure the unused pins on ports 0-9 as output low level. The purpose of this is to reduce noise susceptibility, noise generation, and minimize power consumption*

2 *All pins on ports 0 - 9 are 5V tolerant*

3 *Pins on ports 0,1,2,4,5,7,8,9 have 4 mA drive and 4mA sink. Ports 3 and 6 have 8 mA drive and 8 mA sink.*

4 *For 8-bit non-muxed EMI operation: Port 8 is eight bits of data, ports 7 and 9 are 16 bits of address.*

5 *For 16-bit muxed EMI operation: Ports 8 and 9 are 16 bits of muxed address and data bits, port 7 is up to eight additional bits of high-order address*

6 *Signal polarity is programmable for interrupt request inputs, EMI_ALE, timer input capture inputs and output compare/PWM outputs, motor control tach and emergency stop inputs, and motor control phase outputs.*

7 *HiZ = High Impedance, V = Voltage Source, G = Ground, I/O = Input/Output*

8 *STR910FA devices do not support USB. On these devices USBDP and USBDN signals are "Not Used" (USBDN is not connected, USBDP must be pulled up by a 1.5K ohm resistor to VDDQ), and all functions named “USB" are not available.*

9 *STR910FA 128-pin and 144-ball devices do not support Ethernet. On these devices PHYCLK and all functions named “MII*" are not available.*

Table 8. Device pin description

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	67	L11	P0.0	I/O	GPIO_0.0, GP Input, HiZ	MII_TX_CLK, PHY Xmit clock	I2C0_CLKIN, I2C clock in	GPIO_0.0, GP Output	I2C0_CLKOUT, I2C clock out	ETM_PCK0, ETM Packet
-	69	K10	P0.1	I/O	GPIO_0.1, GP Input, HiZ	-	I2C0_DIN, I2C data in	GPIO_0.1, GP Output	I2C0_DOUT, I2C data out	ETM_PCK1, ETM Packet
-	71	J11	P0.2	I/O	GPIO_0.2, GP Input, HiZ	MII_RXD0, PHY Rx data0	I2C1_CLKIN, I2C clock in	GPIO_0.2, GP Output	I2C1_CLKOUT, I2C clock out	ETM_PCK2, ETM Packet
-	76	H12	P0.3	I/O	GPIO_0.3, GP Input, HiZ	MII_RXD1, PHY Rx data	I2C1_DIN, I2C data in	GPIO_0.3, GP Output	I2C1_DOUT, I2C data out	ETM_PCK3, ETM Packet
-	78	H10	P0.4	I/O	GPIO_0.4, GP Input, HiZ	MII_RXD2, PHY Rx data	TIM0_ICAP1, Input Capture	GPIO_0.4, GP Output	EMI_CS0n, EMI Chip Select	ETM_PSTAT0, ETM pipe status
-	85	F11	P0.5	I/O	GPIO_0.5, GP Input, HiZ	MII_RXD3, PHY Rx data	TIM0_ICAP2, Input Capture	GPIO_0.5, GP Output	EMI_CS1n, EMI Chip Select	ETM_PSTAT1, ETM pipe status
-	88	E11	P0.6	I/O	GPIO_0.6, GP Input, HiZ	MII_RX_CLK, PHY Rx clock	TIM2_ICAP1, Input Capture	GPIO_0.6, GP Output	EMI_CS2n, EMI Chip Select	ETM_PSTAT2, ETM pipe status
-	90	B12	P0.7	I/O	GPIO_0.7, GP Input, HiZ	MII_RX_DV, PHY data valid	TIM2_ICAP2, Input Capture	GPIO_0.7, GP Output	EMI_CS3n, EMI Chip Select	ETM_TRSYNC, ETM trace sync
-	98	B10	P1.0	I/O	GPIO_1.0, GP Input, HiZ	MII_RX_ER, PHY rcv error	ETM_EXTRIG, ETM ext. trigger	GPIO_1.0, GP Output	UART1_TX, UART xmit data	SSP1_SCLK, SSP mstr clk out
-	99	C10	P1.1	I/O	GPIO_1.1, GP Input, HiZ	-	UART1_RX, UART rcv data	GPIO_1.1, GP Output	MII_TXD0, MAC Tx data	SSP1_MOSI, SSP mstr dat out
-	101	B9	P1.2	I/O	GPIO_1.2, GP Input, HiZ	-	SSP1_MISO, SSP mstr data in	GPIO_1.2, GP Output	MII_TXD1, MAC Tx data	UART0_TX, UART xmit data
-	106	C8	P1.3	I/O	GPIO_1.3, GP Input, HiZ	-	UART2_RX, UART rcv data	GPIO_1.3, GP Output	MII_TXD2, MAC Tx data	SSP1_NSS, SSP mstr sel out
-	109	B7	P1.4	I/O	GPIO_1.4, GP Input, HiZ	-	I2C0_CLKIN, I2C clock in	GPIO_1.4, GP Output	MII_TXD3, MAC Tx data	I2C0_CLKOUT, I2C clock out
-	110	A7	P1.5	I/O	GPIO_1.5, GP Input, HiZ	MII_COL, PHY collision	CAN_RX, CAN rcv data	GPIO_1.5, GP Output	UART2_TX, UART xmit data	ETM_TRCLK, ETM trace clock
-	114	F7	P1.6	I/O	GPIO_1.6, GP Input, HiZ	MII_CRS, PHY carrier sns	I2C0_DIN, I2C data in	GPIO_1.6, GP Output	CAN_TX, CAN Tx data	I2C0_DOUT, I2C data out
-	116	D6	P1.7	I/O	GPIO_1.7, GP Input, HiZ	-	ETM_EXTRIG, ETM ext. trigger	GPIO_1.7, GP Output	MII_MDC, MAC mgt dat ck	ETM_TRCLK, ETM trace clock
7	10	E2	P2.0	I/O	GPIO_2.0, GP Input, HiZ	UART0_CTS, Clear To Send	I2C0_CLKIN, I2C clock in	GPIO_2.0, GP Output	I2C0_CLKOUT, I2C clock out	ETM_PCK0, ETM Packet
8	11	E3	P2.1	I/O	GPIO_2.1, GP Input, HiZ	UART0_DSR, Data Set Ready	I2C0_DIN, I2C data in	GPIO_2.1, GP Output	I2C0_DOUT, I2C data out	ETM_PCK1, ETM Packet
21	33	M1	P2.2	I/O	GPIO_2.2, GP Input, HiZ	UART0_DCD, Dat Carrier Det	I2C1_CLKIN, I2C clock in	GPIO_2.2, GP Output	I2C1_CLKOUT, I2C clock out	ETM_PCK2, ETM Packet
22	35	K3	P2.3	I/O	GPIO_2.3, GP Input, HiZ	UART0_RI, Ring Indicator	I2C1_DIN, I2C data in	GPIO_2.3, GP Output	I2C1_DOUT, I2C data out	ETM_PCK3, ETM Packet
23	37	L4	P2.4	I/O	GPIO_2.4, GP Input, HiZ	EXTCLK_T0T1E xt clk timer0/1	SSP0_SCLK, SSP slv clk in	GPIO_2.4, GP Output	SSP0_SCLK, SSP mstr clk out	ETM_PSTAT0, ETM pipe status

7.7.1 Main oscillator electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 18. Main oscillator electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{STUP(OSC)}$	Oscillator Start-up Time	V_{DD} stable (1)		2	3	mS

1. Data characterized with quartz crystal, not tested in production.

7.7.2 X1_CPU external clock source

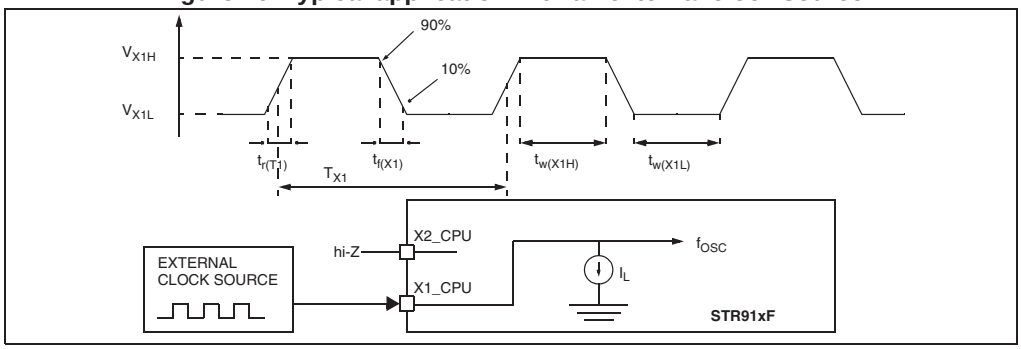
Subject to general operating conditions for V_{DD} and T_A.

Table 19. External clock characteristics

Symbol	Parameter	Test conditions(1)	Value			Unit
			Min	Typ	Max	
f_{X1}	External clock source frequency	See *Figure 16*	4		25	MHz
V_{X1H}	X1 input pin high level voltage		0.7xV_{DD}		V_{DD}	V
V_{X1L}	X1 input pin low level voltage		V_{SS}		0.3xV_{DD}	V
$t_{w(X1H)}$ $t_{w(X1L)}$	X1 high or low time(2)		6			ns
$t_{r(X1)}$ $t_{f(X1)}$	X1 rise or fall time(2)				20	ns
I_L	X1 input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
$C_{IN(X1)}$	X1 input capacitance(2)			5		pF
$DuCy_{(X1)}$	Duty cycle		45		55	%

1. Data based on typical appilcation software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 16. Typical application with an external clock source



7.7.3 RTC clock generated from a crystal/ceramic resonator

The RTC (Real-Time Clock) can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results obtained with typical external components specified in *Table 20* & *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 16 pF range, selected to match the requirements of the crystal or resonator. CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.

Load capacitance CL has the following formula:

CL = CL1 x CL2 / (CL1 + CL2) + Cstray

where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of CL = 6 pF, and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

Conditions: V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 20. RTC oscillator electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
R_F	External feedback resistor			22		MΩ
$V_{START(RTC)}$	Oscillator start voltage		V_{DD_LVD+} (1)			V
g_M	Oscillator transconductance(2)	Start-up	1.8			µA/Volts
$t_{STUP(RTC)}$	Oscillator Start-up Time(2)	V_{DD} stable			1	S

1. Refer to *Table 14* for min. value of V_{DD_LVD+}
2. Data based on bench measurements, not tested in production.

7.9.2 Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 28. EMI data

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}/f_{CPUCLK}]		Unit
				24 MHz / 48 MHz(1)	24 MHz / 96 MHz(1)	
S_{EMI}	Peak level	V_{DDQ} = 3.3 V, V_{DD}=1.8 V, T_A=+25 °C, LQFP128 package(2) conforming to SAE J 1752/3	0.1 MHz to 30 MHz	14	10	dBµV
			30 MHz to 130 MHz	18	19	
			130 MHz to 1GHz	18	22	
			SAE EMI Level	4	4	-

1. Data based on characterization results, not tested in production.
2. BGA and LQFP devices have similar EMI characteristics.

7.9.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

7.9.4 Electro-static discharge (ESD)

Electro-Static Discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 29. ESD data

Symbol	Ratings	Conditions	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A = +25°C conforming to JESD22-A114	2	+/-2000	V
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charged Device Model)	T_A = +25°C conforming to JESD22-C101	II	1000	

1. Data based on characterization results, not tested in production.

7.12.5 SPI electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 46. SPI electrical characteristics

Symbol	Parameter	Test conditions	Value		Unit
			Typ	Max	
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master		24	MHz
		Slave		4	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall times	50pF load	0.1		V/ns
$t_{su(SS)}$	SS setup time	Slave	1		t_{PCLK}
$t_{h(SS)}$	SS hold time	Slave	1		
$t_{w(SCLKH)}$ $t_{w(SCLKL)}$	SCLK high and low time	Master Slave	1		
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master Slave	TBD 5		
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master Slave	TBD 6		
$t_{a(SO)}$	Data output access time	Slave		6	
$t_{dis(SO)}$	Data output disable time	Slave		6	
$t_{v(SO)}$	Data output valid time	Slave (after enable edge)		6	
$t_{h(SO)}$	Data output hold time		0		
$t_{v(MO)}$	Data output valid time	Master (before capture edge)	0.25		
$t_{h(MO)}$	Data output hold time		0.25		

Figure 30. SPI slave timing diagram with CPHA = 0

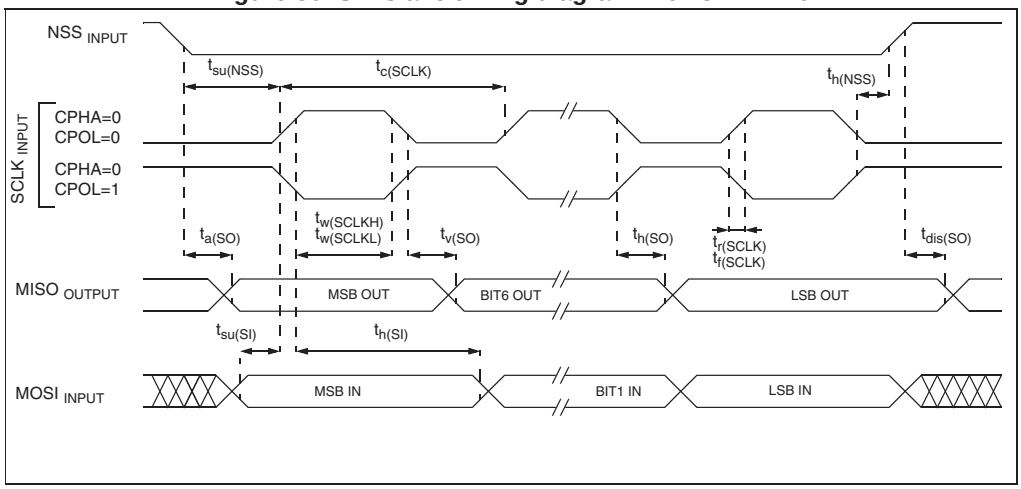
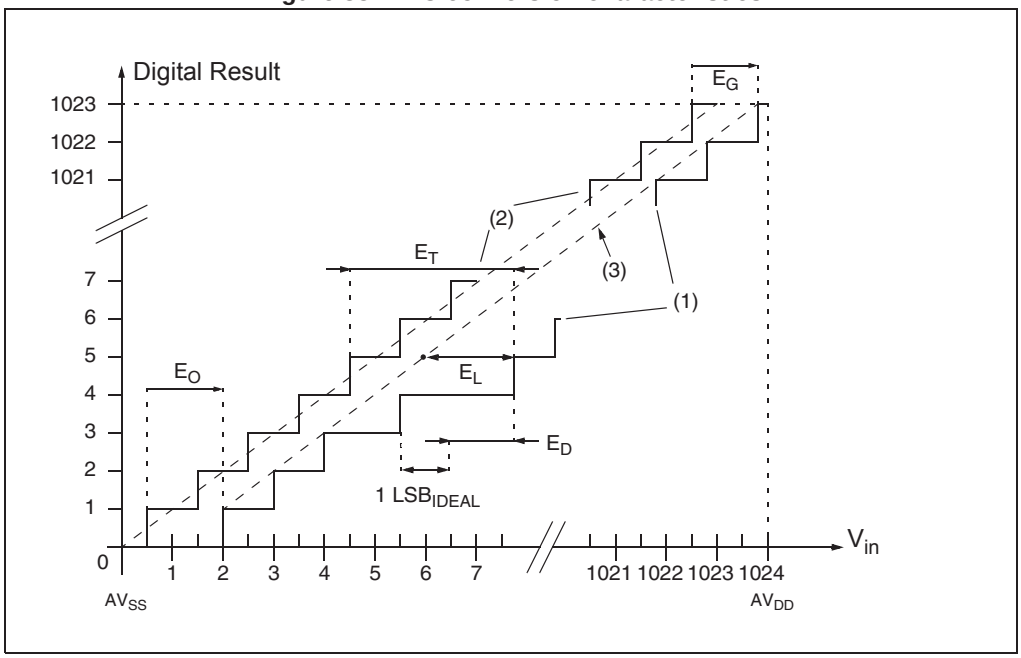


Figure 33. ADC conversion characteristics



1. Legend:
   (1) Example of an actual transfer curve
   (2) The ideal transfer curve
   (3) End point correlation line
   E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset Error: deviation between the first actual transition and the first ideal one.
   E_G = Gain Error: deviation between the last ideal transition and the last actual one.
   E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

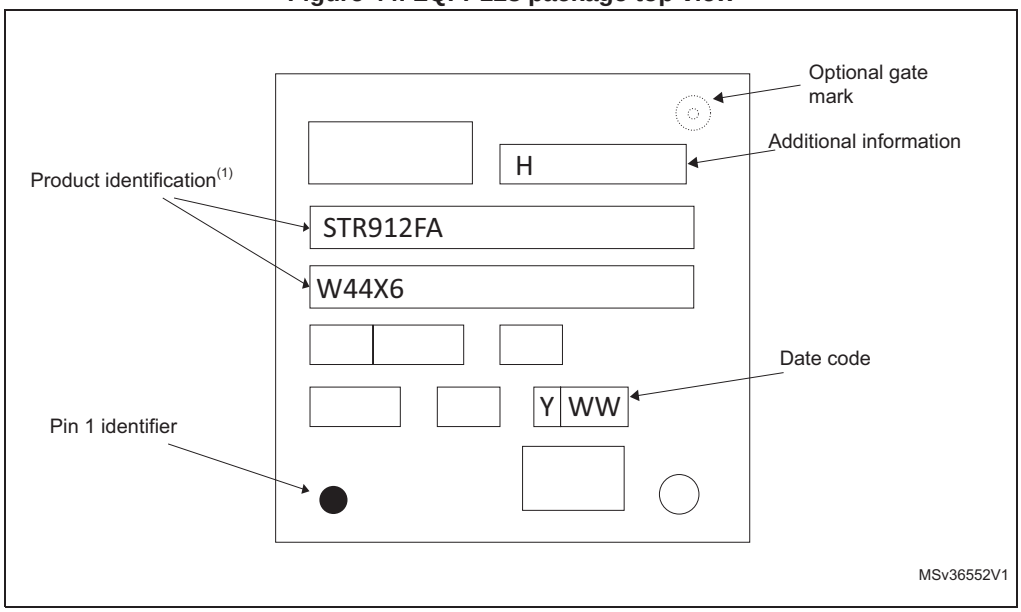
Equation 1

$$1LSB_{IDEAL} = \frac{V_{DDA} - V_{SSA}}{1024}$$

Marking of engineering samples for LQFP128

The following figure shows the engineering sample marking for the LQFP128 package. Only the information field containing the engineering sample marking is shown.

Figure 44. LQFP128 package top view



1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 52.LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A[2]	-	-	1.700			0.0669
A1	0.210	-	-	0.0083		
A2	-	1.060	-		0.0417	
A3		0.026			0.0010	
A4	-	0.800	-	-	0.0315	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	8.800	-	-	0.3465	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	0.100			0.0039		
eee	0.150			0.0059		
fff	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.

11 Revision history

Table 55. Document revision history

Date	Revision	Changes
09-May-2007	1	Initial release
26-Nov-2007	2	Updated Standby current in *Table 15: Supply current characteristics on page 64* Added *Section 7.1: Parameter conditions on page 58* Added *Section 7.7.2: X1_CPU external clock source on page 67* Updated *Section 7.11: External memory bus timings on page 76* Added *Figure 14: LVD reset delay case 3 on page 63* Added *Table 48* and *Table 49* in ADC characteristics section Added min/max values for E, D, E1, D1 in *Figure 43 on page 98*
14-May-2008	3	Added 1MB and 2M devices, creating merged datasheet from seperate STR91xFAx32, 42, 44, 46 and 47 devices. Added STR912FAW32 to *Table 1: Device summary on page 1* Added paragraph on voltage supply shutdown in *Section 3.12 on page 24* Removed DMA feature for I2C in *Section 3.21 on page 33* Updated Sleep mode current in *Table 10: Current characteristics on page 60* Added *Table 16: Typical current consumption at 25 °C on page 65* Updated operating conditions for V_{DD} and f_{CPUCLK} in *Section 7.3 on page 61* and *Section 7.7: Clock and timing characteristics on page 66* Changed SPI master t_{SU} and $t_{H\ to}$ TBD in *Table 46: SPI electrical characteristics on page 88*
17-Jul-2008	4	Updated *Section 3.10.6: UART and SSP clock (BRCLK) on page 22* Updated *Table 11: Operating conditions on page 61* Updated $I_{SLEEP(IDDQ)}$ in *Table 15: Supply current characteristics on page 64* Updated *Table 17: Internal clock frequencies on page 66* Updated *Table 31: I/O characteristics on page 75*
22-Dec-2008	5	Updated *Section 7.7.3 on page 68*. Small text changes.

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