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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str911faw44x6

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3.10.5 Flash memory interface clock (FMICLK)

The FMICLK clock is an internal clock derived from RCLK, defaulting to RCLK frequency at power up. The clock can be optionally divided by 2. The FMICLK determines the bus bandwidth between the ARM core and the Flash memory. Typically, codes in the Flash memory can be fetched one word per FMICLK clock in burst mode. The maximum FMICLK frequency is 96 MHz.

3.10.6 UART and SSP clock (BRCLK)

BRCLK is an internal clock derived from f_{MSTR} that is used to drive the two SSP peripherals and to generate the Baud rate for the three on-chip UART peripherals. The frequency can be optionally divided by 2.

3.10.7 External memory interface bus clock (BCLK)

The BCLK is an internal clock that controls the EMI bus. All EMI bus signals are synchronized to the BCLK. The BCLK is derived from the HCLK and the frequency can be configured to be the same or half that of the HCLK. Refer to *Table 17 on page 66* for the maximum BCLK frequency (f_{BCLK}). The BCLK clock is available on the LFBGA package as an output pin.

3.10.8 USB interface clock

Special consideration regarding the USB interface: The clock to the USB interface must operate at 48 MHz and comes from one of three sources, selected under firmware control:

- CCU master clock output of 48 MHz.
- CCU master clock output of 96 MHz. An optional divided-by-two circuit is available to produce 48 MHz for the USB while the CPU system runs at 96MHz.
- STR91xFA pin P2.7. An external 48 MHz oscillator connected to pin P2.7 can directly source the USB while the CCU master clock can run at some frequency other than 48 or 96 MHz.

3.10.9 Ethernet MAC clock

Special consideration regarding the Ethernet MAC: The external Ethernet PHY interface device requires it's own 25 MHz clock source. This clock can come from one of two sources:

- A 25 MHz clock signal coming from a dedicated output pin (P5.2) of the STR91xFA. In this case, the STR91xFA must use a 25 MHz signal on its main oscillator input in order to pass this 25 MHz clock back out to the PHY device through pin P5.2. The advantage here is that an inexpensive 25 MHz crystal may be used to source a clock to both the STR91xFA and the external PHY device.
- An external 25 MHz oscillator connected directly to the external PHY interface device. In this case, the STR91xFA can operate independent of 25 MHz.

3.10.10 External RTC calibration clock

The RTC_CLK can be enabled as an output on the JRTCK pin. The RTC_CLK is used for RTC oscillator calibration. The RTC_CLK is active in Sleep mode and can be used as a system wake up control clock.

3.10.11 Operation example

As an example of CCU operation, a 25 MHz crystal can be connected to the main oscillator input on pins X1_CPU and X2_CPU, a 32.768 kHz crystal connected to pins X1_RTC and X2_RTC, and the clock input of an external Ethernet PHY device is connected to STR91xFA output pin P5.2. In this case, the CCU can run the CPU at 96 MHz from PLL, the USB interface at 48 MHz, and the Ethernet interface at 25 MHz. The RTC is always running in the background at 32.768 kHz, and the CPU can go to very low power mode dynamically by running from 32.768 kHz and shutting off peripheral clocks and the PLL as needed.

3.11 Flexible power management

The STR91xFA offers configurable and flexible power management control that allows the user to choose the best power option to fit the application. Power consumption can be dynamically managed by firmware and hardware to match the system's requirements. Power management is provided via clock control to the CPU and individual peripherals.

Clocks to the CPU and peripherals can be individually divided and gated off as needed. In addition to individual clock divisors, the CCU master clock source going to the CPU, AHB, APB, EMI, and FMI can be divided dynamically by as much as 1024 for low power operation. Additionally, the CCU may switch its input to the 32.768 kHz RTC clock at any time for low power.

The STR91xFA supports the following three global power control modes:

- ***Run Mode*:** All clocks are on with option to gate individual clocks off via clock mask registers.
- ***Idle Mode*:** CPU and FMI clocks are off until an interrupt, reset, or wake-up occurs. Pre-configured clock mask registers selectively allow individual peripheral clocks to continue run during Idle Mode.
- ***Sleep Mode*:** All clocks off except RTC clock. Wake up unit remains powered, PLL is forced off.

A special mode is used when JTAG debug is active which never gates off any clocks even if the CPU enters Idle or Sleep mode.

3.11.1 Run mode

This is the default mode after any reset occurs. Firmware can gate off or scale any individual clock. Also available is a special Interrupt Mode which allows the CPU to automatically run full speed during an interrupt service and return back to the selected CPU clock divisor rate when the interrupt has been serviced. The advantage here is that the CPU can run at a very low frequency to conserve power until a periodic wake-up event or an asynchronous interrupt occurs at which time the CPU runs full speed immediately.

3.11.2 Idle mode

In this mode the CPU suspends code execution and the CPU and FMI clocks are turned off immediately after firmware sets the Idle Bit. Various peripherals continue to run based on the settings of the mask registers that exist just prior to entering Idle Mode. There are 3 ways to exit Idle Mode and return to Run Mode:

- Any reset (external reset pin, watchdog, low-voltage, power-up, JTAG debug command)
- Any interrupt (external, internal peripheral, RTC alarm or interval)
- Input from wake-up unit on GPIO pins

Note: It is possible to remain in Idle Mode for the majority of the time and the RTC can be programmed to periodically wake up to perform a brief task or check status.

3.11.3 Sleep mode

In this mode all clock circuits except the RTC are turned off and main oscillator input pins X1_CPU and X2_CPU are disabled. The RTC clock is required for the CPU to exit Sleep Mode. The entire chip is quiescent (except for RTC and wake-up circuitry). There are three means to exit Sleep Mode and re-start the system:

- Some resets (external reset pin, low-voltage, power-up, JTAG debug command)
- RTC alarm
- Input from wake-up unit

3.12 Voltage supplies

The STR91xFA requires two separate operating voltage supplies. The CPU and memories operate from a 1.65V to 2.0V on the VDD pins, and the I/O ring operates at 2.7V to 3.6V on the VDDQ pins.

In Standby mode, both VDD and VDDQ must be shut down. Otherwise the specified maximum power consumption for Standby mode (I_{RTC_STBY} and I_{SRAM_STBY}) may be exceeded. Leakage may occur if only one of the voltage supplies is off.

3.12.1 Independent A/D converter supply and reference voltage

The ADC unit on 128-pin and 144-ball packages has an isolated analog voltage supply input at pin AVDD to accept a very clean voltage source, independent of the digital voltage supplies. Additionally, an isolated analog supply ground connection is provided on pin AVSS only on 128-pin and 144-ball packages for further ADC supply isolation. On 80-pin packages, the analog voltage supply is shared with the ADC reference voltage pin (as described next), and the analog ground is shared with the digital ground at a single point in the STR91xFA device on pin AVSS_VSSQ.

A separate external analog reference voltage input for the ADC unit is available on 128-pin and 144-ball packages at the AVREF pin for better accuracy on low voltage inputs. For 80-pin packages, the ADC reference voltage is tied internally to the ADC unit supply voltage at pin AVREF_AVDD, meaning the ADC reference voltage is fixed to the ADC unit supply voltage.

See *Table 11: Operating conditions*, for restrictions to the relative voltage levels of VDDQ, AVDD, AVREF, and AVREF_AVDD.

3.12.2 Battery supply

An optional stand-by voltage from a battery or other source may be connected to pin VBATT to retain the contents of SRAM in the event of a loss of the main digital supplies (V_{DD} and $V_{DDQ)}$. The SRAM will automatically switch its supply from the internal V_{DD} source to the VBATT pin when the voltage of V_{DD} drops below the LVD threshold. In order to use the battery supply, the LVD must be enabled.

The VBATT pin also supplies power to the RTC unit, allowing the RTC to function even when the main digital supplies (V_{DD} and V_{DDQ}) are switched off. By configuring the RTC register, it is possible to select whether or not to power from VBATT only the RTC unit, or power the RTC unit and the SRAM when the STR91xFA device is powered off.

3.13 System supervisor

The STR91xFA monitors several system and environmental inputs and will generate a global reset, a system reset, or an interrupt based on the nature of the input and configurable settings. A global reset clears all functions on the STR91xFA, a system reset will clear all but the Clock Control Unit (CCU) settings and the system status register. At any time, firmware may reset individual on-chip peripherals. System supervisor inputs include:

- GR: CPU voltage supply (V_{DD}) drop out or brown out
- GR: I/O voltage supply (V_{DDQ}) drop out or brown out
- GR: Power-Up condition
- SR: Watchdog timer timeout
- SR: External reset pin (RESET_INn)
- SR: JTAG debug reset command

Note: GR: means the input causes Global Reset, SR: means the input causes System Reset

The CPU may read a status register after a reset event to determine if the reset was caused by a watchdog timer timeout or a voltage supply drop out. This status register is cleared only by a power up reset.

3.13.1 Supply voltage brownout

Each operating voltage source (V_{DD} and V_{DDQ}) is monitored separately by the Low Voltage Detect (LVD) circuitry. The LVD will generate an early warning interrupt to the CPU when voltage sags on either V_{DD} or V_{DDQ} voltage inputs. This is an advantage for battery powered applications because the system can perform an orderly shutdown before the batteries become too weak. The voltage trip point to cause a brown out interrupt is typically 0.25V above the LVD dropout thresholds that cause a reset.

CPU firmware may prevent all brown-out interrupts by writing to interrupt mask registers at run-time.

3.18.1 Packet buffer interface (PBI)

The PBI manages a set of buffers inside the 2 Kbyte Packet Buffer, both for transmission and reception. The PBI will choose the proper buffer according to requests coming from the USB Serial Interface Engine (SIE) and locate it in the Packet SRAM according to addresses pointed by endpoint registers. The PBI will also auto-increment the address after each exchanged byte until the end of packet, keeping track of the number of exchanged bytes and preventing buffer overrun. Special support is provided by the PBI for isochronous and bulk transfers, implementing double-buffer usage which ensures there is always an available buffer for a USB packet while the CPU uses a different buffer.

3.18.2 DMA

A programmable DMA channel may be assigned by CPU firmware to service the USB interface for fast and direct transfers between the USB bus and SRAM with little CPU involvement. This DMA channel includes the following features:

- Direct USB Packet Buffer SRAM to system SRAM transfers of receive packets, by descriptor chain for bulk or isochronous endpoints.
- Direct system SRAM to USB Packet Buffer SRAM transfers of transmit packets, by descriptor chain for bulk or isochronous endpoints.
- Linked-list descriptor chain support for multiple USB packets

3.18.3 Suspend mode

CPU firmware may place the USB interface in a low-power suspend mode when required, and the USB interface will automatically wake up asynchronously upon detecting activity on the USB pins.

3.19 CAN 2.0B interface

The STR91xFA provides a CAN interface complying with CAN protocol version 2.0 parts A and B. An external CAN transceiver device connected to pins CAN_RX and CAN_TX is required for connection to the physical CAN bus.

The CAN interface manages up to 32 Message Objects and Identifier Masks using a Message SRAM and a Message Handler. The Message Handler takes care of low-level CAN bus activity such as acceptance filtering, transfer of messages between the CAN bus and the Message SRAM, handling of transmission requests, and interrupt generation. The CPU has access to the Message SRAM via the Message Handler using a set of 38 control registers.

The follow features are supported by the CAN interface:

- Bit rates up to 1 Mbps
- Disable Automatic Retransmission mode for Time Triggered CAN applications
- 32 Message Objects
- Each Message Object has its own Identifier Mask
- Programmable FIFO mode
- Programmable loopback mode for self-test operation

The CAN interface is not supported by DMA.

3.20 UART interfaces with DMA

The STR91xFA supports three independent UART serial interfaces, designated UART0, UART1, and UART2. Each interface is very similar to the industry-standard 16C550 UART device. All three UART channels support IrDA encoding/decoding, requiring only an external LED transceiver to pins UARTx_RX and UARTx_Tx for communication. One UART channel (UART0) supports full modem control signals.

UART interfaces include the following features:

- Maximum baud rate of 1.5 Mbps
- Separate FIFOs for transmit and receive, each 16 deep, each FIFO can be disabled by firmware if desired
- Programmable FIFO trigger levels between 1/8 and 7/8
- Programmable baud rate generator based on CCU master clock, or CCU master clock divided by two
- Programmable serial data lengths of 5, 6, 7, or 8 bits with start bit and 1 or 2 stop bits
- Programmable selection of even, odd, or no-parity bit generation and detection
- False start-bit detection
- Line break generation and detection
- Support of IrDA SIR ENDEC functions for data rates of up to 115.2K bps
- IrDA bit duration selection of 3/16 or low-power (1.14 to 2.23 µsec)
- Channel UART0 supports modem control functions CTS, DCD, DSR, RTS, DTR, and RI

For your reference, only two standard 16550 UART features are not supported, 1.5 stop bits and independent receive clock.

3.20.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service channels UART0 and UART1 for fast and direct transfers between the UART bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive. Burst transfers require that UART FIFOs are enabled.

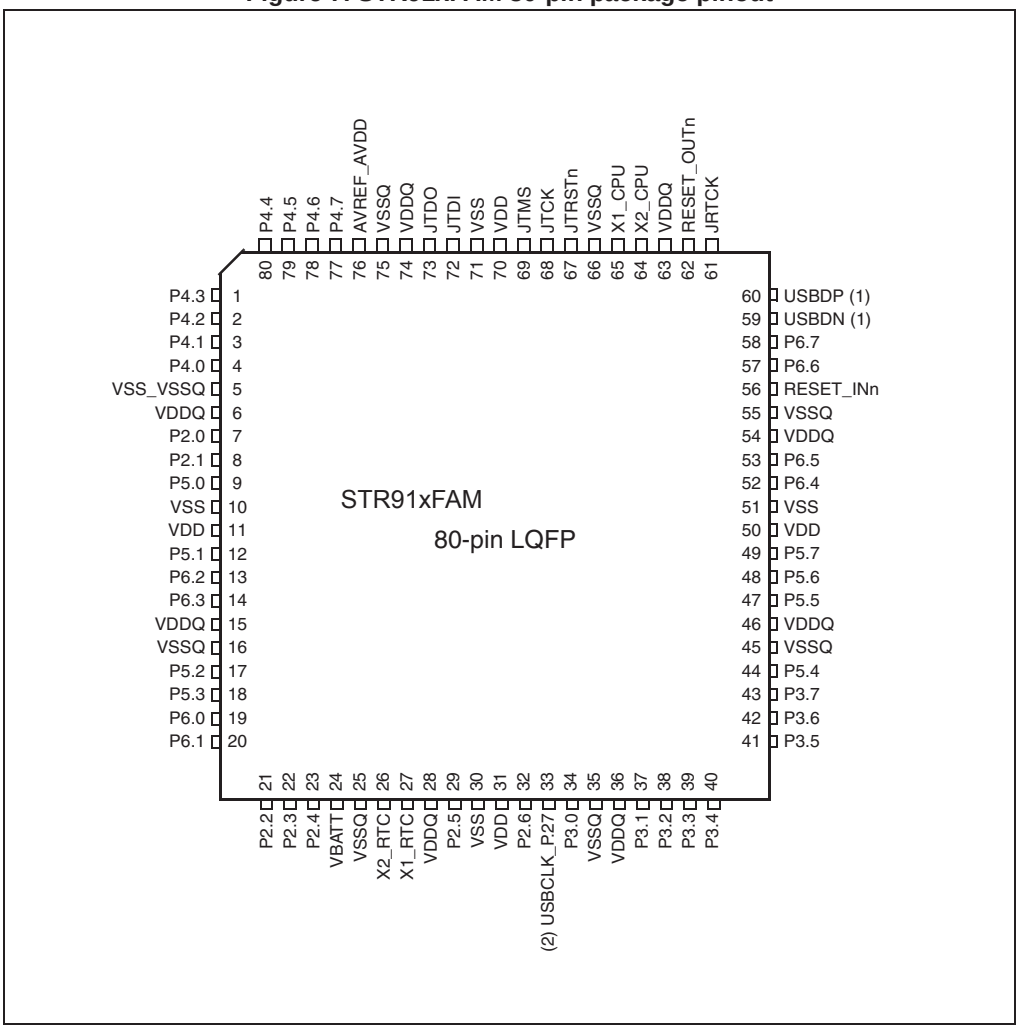
3.21 I^2C interfaces

The STR91xFA supports two independent I2C serial interfaces, designated I2C0, and I2C1. Each interface allows direct connection to an I2C bus as either a bus master or bus slave device (firmware configurable). I2C is a two-wire communication channel, having a bi-directional data signal and a single-directional clock signal based on open-drain line drivers, requiring external pull-up resistors.

Byte-wide data is transferred between a Master device and a Slave device on two wires. More than one bus Master is allowed, but only one Master may control the bus at any given time. Data is not lost when another Master requests the use of a busy bus because I2C supports collision detection and arbitration. More than one Slave device may be present on the bus, each having a unique address. The bus Master initiates all data movement and generates the clock that permits the transfer. Once a transfer is initiated by the Master, any device that is addressed is considered a Slave. Automatic clock synchronization allows I2C devices with different bit rates to communicate on the same physical bus.

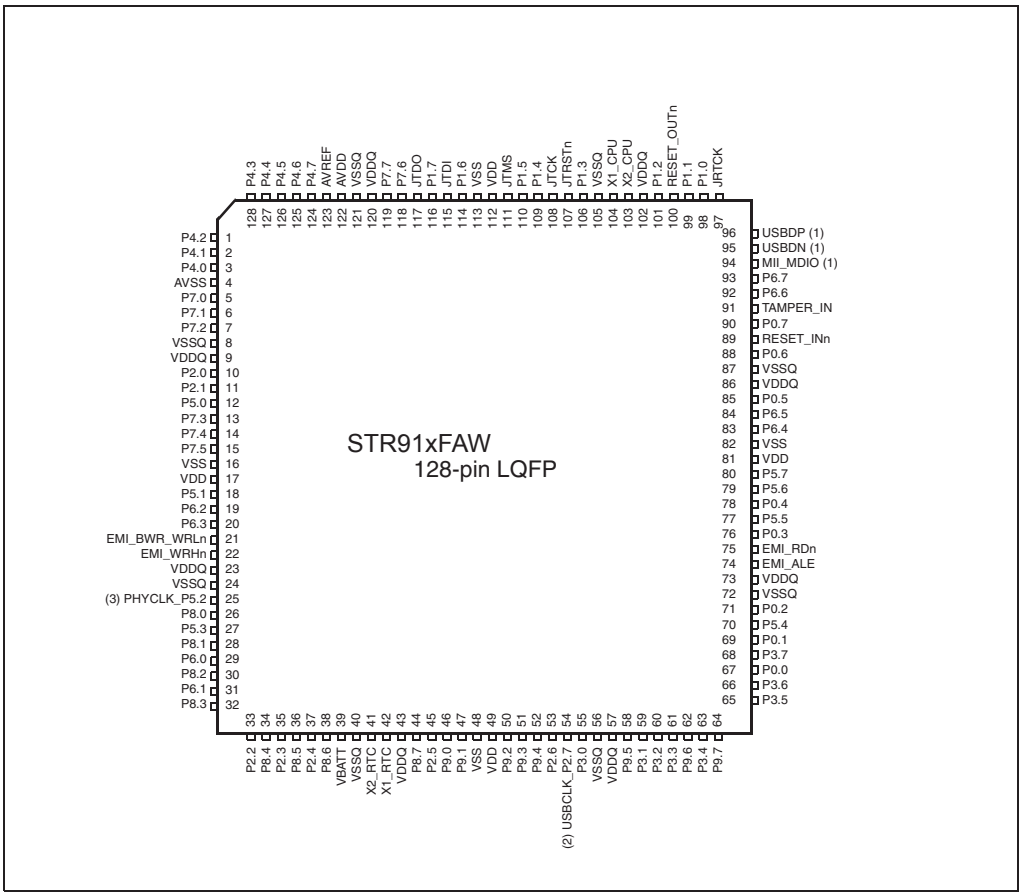
5 Pin description

Figure 7. STR91xFAM 80-pin package pinout



1. NU (Not Used) on STR910FAM devices. Pin 59 is not connected, pin 60 must be pulled up by a 1.5Kohm resistor to VDDQ.
2. No USBCLK function on STR910FAM devices.

Figure 8. STR91xFAW 128-pin package pinout



1. NU (Not Used) on STR910FAW devices. Pin 95 is not connected, pin 96 must be pulled up by a 1.5Kohm resistor to VDDQ.
2. No USBCLK function on STR910FAW devices.
3. No PHYCLK function on STR910FAW devices.

5.1 LFBGA144 ball connections

- In *Table 7* balls labelled NC are no connect balls. These NC balls are reserved for future devices and should NOT be connected to ground or any other signal. There are total of 9 NC (no connection) balls.
- Balls H1 and G4 are assigned as EMI bus write signals (EMI_BWR_WRLn and EMI_WRHn). These two balls can also be configured by the user as EMI low or high byte select signals (EMI_LBn and EMI_UBn).
- The PLLGND (B8) and PLLVDDQ (C9) balls can be connected to VSSQ and VDDQ.

Table 7. STR91x LFBGA144 ball connections

	A	B	C	D	E	F	G	H	J	K	L	M
1	P4.2	P7.2	NC	P7.0	VDDQ	P7.3	P7.4	EMI_WRHn (EMI_UBn)	VDDQ	PHYCLK_ P5.2(1)	P8.0	P2.2
2	AVREF	P4.1	P4.0	P7.1	P2.0	NC	P6.2	P5.3	P8.2	P8.3	VSSQ	P8.6
3	AVDD	P4.3	AVSS	NC	P2.1	VSS	P6.3	P8.1	P6.1	P2.3	P8.4	VBATT
4	P4.6	P4.5	P4.4	VSSQ	P5.0	VDD	EMI_BWR_ WRLn (EMI_LBn)	P6.0	P8.5	VSSQ	P2.4	X2_ RTC
5	P7.7	VDDQ	VSSQ	P4.7	P7.5	NC	VSSQ	VSS	P2.5	P8.7	VDDQ	X1_ RTC
6	JTMS	JTDO	JTDI	P1.7	P7.6	P5.1	P2.6	P9.4	P9.3	P9.2	VDD	P9.0
7	P1.5	P1.4	NC	VDD	VSS	P1.6	P6.5	VDDQ	VSSQ	P3.0	USBCLK _P2.7 (2)	P9.1
8	VSSQ	PLLVSSQ	P1.3	JRSTn	JTCK	VSSQ	P6.4	EMI_BAAn	P3.3	EMI_ WAITn	P9.5	EMI_ BCLK
9	RESET_ OUTn	P1.2	PLLVDDQ	VDDQ	P6.6	VDDQ	NC	P5.6	EMI_ RDn	P9.7	P3.4	P9.6
10	X1_CPU	P1.0	P1.1	USBDN(3)	TAMPER_ IN	NC	VSS	P0.4	EMI_ ALE	P0.1	P3.5	P3.1
11	X2_CPU	JRTCK	USBDP(2)	MII_ MDIO(3)	P0.6	P0.5	VDD	P5.5	P0.2	P3.7	P0.0	P3.2
12	EMI_ WEn	P0.7	RESET_ INn	P6.7	NC	NC	P5.7	P0.3	P5.4	VDDQ	VSSQ	P3.6

1. No PHYCLK function on STR910FAW devices.
2. No USBCLK function on STR910FAW devices.
3. NU (Not Used) on STR910FAW devices. D10 is not connected, C11 must be pulled up by a 1.5 kOhm resistor to VDDQ.

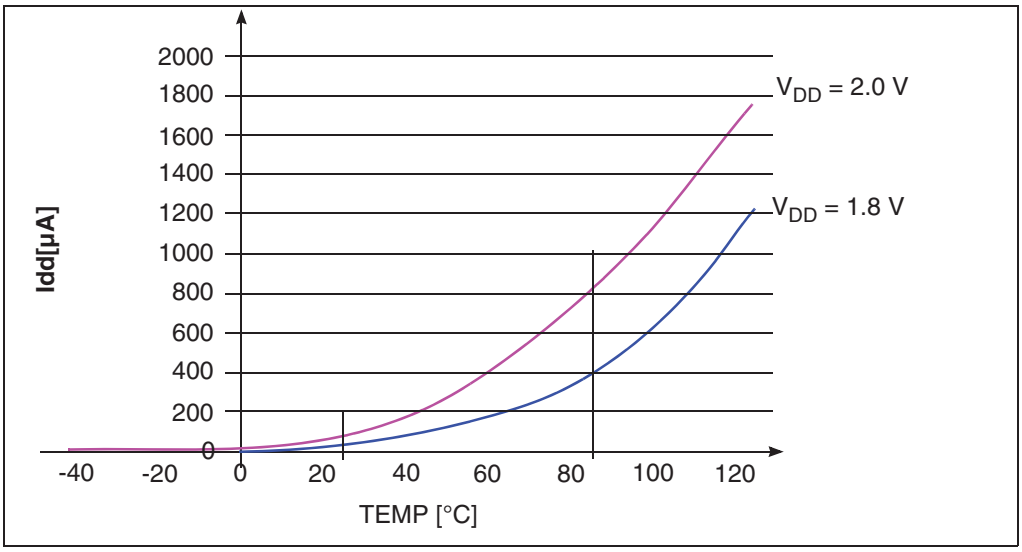
Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
12	18	F6	P5.1	I/0	GPIO_5.1, GP Input, HiZ	EXINT9, External Intr	UART0_RxD, UART rcv data	GPIO_5.1, GP Output	CAN_TX, CAN Tx data	UART2_TX, UART xmit data
17	25	K1	PHYCLK _P5.2	I/O	GPIO_5.2, GP Input, HiZ	EXINT10, External Intr	UART2_RxD, UART rcv data	GPIO_5.2, GP Output	MII_PHYCLK, 25Mhz to PHY	TIM3_OCMP1, Out comp/PWM
18	27	H2	P5.3	I/O	GPIO_5.3, GP Input, HiZ	EXINT11, External Intr	ETM_EXTRIG, ETM ext. trigger	GPIO_5.3, GP Output	MII_TX_EN, MAC xmit enbl	TIM2_OCMP1, Out comp/PWM
44	70	J12	P5.4	I/O	GPIO_5.4, GP Input, HiZ	EXINT12, External Intr	SSP0_SCLK, SSP slv clk in	GPIO_5.4, GP Output	SSP0_SCLK, SSP mstr clk out	EMI_CS0n, EMI Chip Select
47	77	H11	P5.5	I/O	GPIO_5.5, GP Input, HiZ	EXINT13, External Intr	SSP0_MOSI, SSP slv dat in	GPIO_5.5, GP Output	SSP0_MOSI, SSP mstr dat out	EMI_CS1n, EMI Chip Select
48	79	H9	P5.6	I/O	GPIO_5.6, GP Input, HiZ	EXINT14, External Intr	SSP0_MISO, SSP mstr dat in	GPIO_5.6, GP Output	SSP0_MISO, SSP slv data out	EMI_CS2n, EMI Chip Select
49	80	G12	P5.7	I/O	GPIO_5.7, GP Input, HiZ	EXINT15, External Intr	SSP0_NSS, SSP slv select in	GPIO_5.7, GP Output	SSP0_NSS, SSP mstr sel out	EMI_CS3n, EMI Chip Select
19	29	H4	P6.0	I/O	GPIO_6.0, GP Input, HiZ	EXINT16, External Intr	TIM0_ICAP1, Input Capture	GPIO_6.0, GP Output	TIM0_OCMP1, Out comp/PWM	MC_UH, IMC phase U hi
20	31	J3	P6.1	I/O	GPIO_6.1, GP Input, HiZ	EXINT17, External Intr	TIM0_ICAP2, Input Capture	GPIO_6.1, GP Output	TIM0_OCMP2, Out comp	MC_UL, IMC phase U lo
13	19	G2	P6.2	I/O	GPIO_6.2, GP Input, HiZ	EXINT18, External Intr	TIM1_ICAP1, Input Capture	GPIO_6.2, GP Output	TIM1_OCMP1, Out comp/PWM	MC_VH, IMC phase V hi
14	20	G3	P6.3	I/O	GPIO_6.3, GP Input, HiZ	EXINT19, External Intr	TIM1_ICAP2, Input Capture	GPIO_6.3, GP Output	TIM1_OCMP2, Out comp	MC_VL, IMC phase V lo
52	83	G8	P6.4	I/O	GPIO_6.4, GP Input, HiZ	EXINT20, External Intr	TIM2_ICAP1, Input Capture	GPIO_6.4, GP Output	TIM2_OCMP1, Out comp/PWM	MC_WH, IMC phase W hi
53	84	G7	P6.5	I/O	GPIO_6.5, GP Input, HiZ	EXINT21, External Intr	TIM2_ICAP2, Input Capture	GPIO_6.5, GP Output	TIM2_OCMP2, Out comp	MC_WL, IMC phase W lo
57	92	E9	P6.6	I/O	GPIO_6.6, GP Input, HiZ	EXINT22_TRIG, Ext Intr & Tach	UART0_RxD, UART rcv data	GPIO_6.6, GP Output	TIM3_OCMP1, Out comp/PWM	ETM_TRCLK, ETM trace clock
58	93	D12	P6.7	I/O	GPIO_6.7, GP Input, HiZ	EXINT23_STOP, Ext Intr & Estop	ETM_EXTRIG, ETM ext. trigger	GPIO_6.7, GP Output	TIM3_OCMP2, Out comp	UART0_TX, UART xmit data
-	5	D1	P7.0	I/O	GPIO_7.0, GP Input, HiZ	EXINT24, External Intr	TIM0_ICAP1, Input Capture	GPIO_7.0, GP Output	8b) EMI_A0, 16b) EMI_A16	ETM_PCK0, ETM Packet
-	6	D2	P7.1	I/O	GPIO_7.1, GP Input, HiZ	EXINT25, External Intr	TIM0_ICAP2, Input Capture	GPIO_7.1, GP Output	8b) EMI_A1, 16b) EMI_A17	ETM_PCK1, ETM Packet
-	7	B1	P7.2	I/O	GPIO_7.2, GP Input, HiZ	EXINT26, External Intr	TIM2_ICAP1, Input Capture	GPIO_7.2, GP Output	8b) EMI_A2, 16b) EMI_A18	ETM_PCK2, ETM Packet
-	13	F1	P7.3	I/O	GPIO_7.3, GP Input, HiZ	EXINT27, External Intr	TIM2_ICAP2, Input Capture	GPIO_7.3, GP Output	8b) EMI_A3, 16b) EMI_A19	ETM_PCK3, ETM Packet
-	14	G1	P7.4	I/O	GPIO_7.4, GP Input, HiZ	EXINT28, External Intr	UART0_RxD, UART rcv data	GPIO_7.4, GP Output	8b) EMI_A4, 16b) EMI_A20	EMI_CS3n, EMI Chip Select
-	15	E5	P7.5	I/O	GPIO_7.5, GP Input, HiZ	EXINT29, External Intr	ETM_EXTRIG, ETM ext. trigger	GPIO_7.5, GP Output	8b) EMI_A5, 16b) EMI_A21	EMI_CS2n, EMI Chip Select

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	8	L2	VSSQ	G	Digital Ground for !/O and USB	N/A				
16	24	K4	VSSQ	G						
35	56	C5	VSSQ	G						
-	-	D4	VSSQ	G						
45	72	G5	VSSQ	G						
55	87	J7	VSSQ	G						
25	40	A8	VSSQ	G						
66	105	F8	VSSQ	G						
75	121	L12	VSSQ	G						
11	17	F4	VDD	V	V Source for CPU. 1.65 V - 2.0 V	N/A				
31	49	D7	VDD	V						
50	81	L6	VDD	V						
70	112	G11	VDD	V						
10	16	F3	VSS	G	Digital Ground for CPU	N/A				
30	48	H5	VSS	G						
51	82	G10	VSS	G						
71	113	E7	VSS	G						
-	-	C9	PLLV DDQ	V	V Source for PLL 2.7 to 3.6 V	N/A				
-	-	B8	PLLV SSQ	G	Digital Ground for PLL					

Figure 15. Sleep mode current vs temperature with LVD on



7.6.1 Typical power consumption for frequencies below 10 MHz

The following conditions apply to *Table 16*:

- Program is executed from Flash. The program consists of an infinite loop.
- A standard crystal source is used.
- The PLL is off.
- All clock dividers are with their default values.

Table 16. Typical current consumption at 25 °C

Symbol	Parameter		Test conditions	Typical current on V_{DD} (1.8 V)	Unit
IDDRUN	Run mode current	All peripherals ON	$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=1 MHz	2.88	mA
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=2 MHz	5.8	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=4 MHz	10.91	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=6 MHz	15.97	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=8 MHz	20.68	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=10 MHz	25.13	
		All peripherals OFF	$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=1 MHz	1.8	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=2 MHz	3.62	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=4 MHz	6.71	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=6 MHz	9.81	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=8 MHz	12.63	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=10 MHz	15.47	

7.7 Clock and timing characteristics

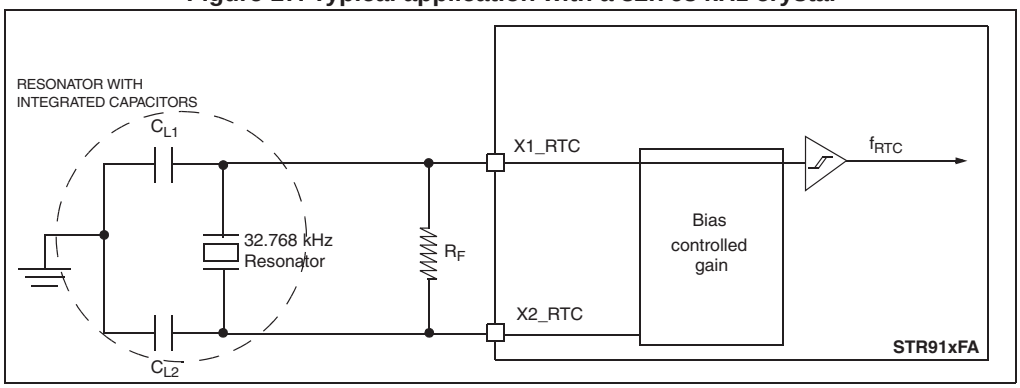
Table 17. Internal clock frequencies

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{MSTR}	CCU Master clock		32.768		$f_{CPUCLKmax}$	kHz
f_{CPUCLK}	CPU Core frequency	Flash size ≤512 KB Executing from SRAM			96	MHz
		Flash size ≤512 KB Executing from Flash			96	MHz
		Flash size = 1 MB / 2 MB, executing from SRAM or Flash V_{DD} ≥1.77 V			96	MHz
		Flash size = 1 MB / 2 MB, executing from SRAM or Flash V_{DD} ≥ 1.65 V			85	MHz
f_{PCLK}	Peripheral clock for APB				48	MHz
f_{HCLK}	Peripheral clock for AHB				$f_{CPUCLKmax}$	MHz
f_{OSC}	Clock input		4		25	MHz
f_{FMICLK}	FMI Flash bus clock (internal clock)				$f_{CPUCLKmax}$	MHz
		Flash size = 1 MB / 2 MB, write operation to Flash memory or Flash registers			48	MHz
f_{BCLK}	External memory bus clock				$f_{CPUCLKmax}$	MHz
f_{RTC}	RTC clock		32.768			kHz
f_{EMAC}	EMAC PHY clock		25			MHz
f_{USB}	USB clock		48			MHz
$f_{TIMCLKEXT}$	Timer external clock		0		$f_{PCLKmax}/4$ = 12	MHz
f_{TIMCLK}	Timer clock when internal clock (PCLK) is selected		0		$f_{PCLKmax}$ = 48	MHz

Table 21. RTC crystal electrical characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			40	kΩ
C_L	Load capacitance			8	pF

Figure 17. Typical application with a 32.768 kHz crystal



7.7.4 PLL electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 22. PLL electrical characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL}	PLL output clock	6.25		$f_{CPUCLKmax}$	MHz
f_{OSC}	Clock input	4		25	MHz
t_{LOCK}	PLL lock time		300	1500	µs
Δt_{JITTER}	PLL jitter (peak to peak)(1)		0.1	0.2	ns

1. Data based on bench measurements, not tested in production

Non-mux read

Figure 19. Non-mux bus read timings

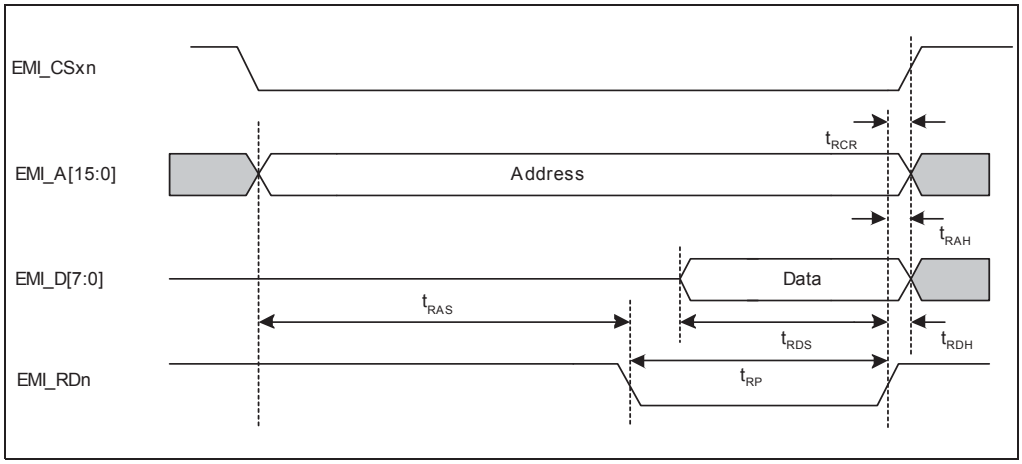


Table 34. EMI read operation

Symbol	Parameter	Value	
		Min	Max
t_{RCR}	Read to CSn inactive	0	1.5 ns
t_{RAS}	Read address setup time	((WSTOEN) x t_{BCLK})- 1.5 ns	(WSTOEN) x t_{BCLK}
t_{RDS}	Read data setup time	12.5	-
t_{RDH}	Read data hold time	0	-
t_{RP}	Read pulse width	((WSTRD-WSTOEN+1) x t_{BCLK})- 0.5 ns	((WSTRD-WSTOEN+1) x t_{BCLK})+ 2 ns

Mux read

Figure 21. Mux read diagram

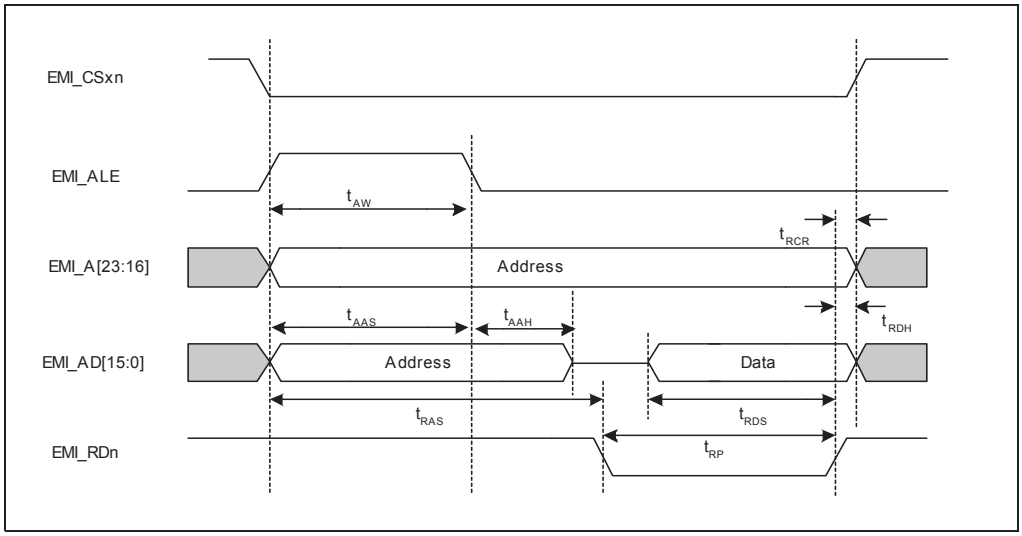


Table 36. Mux read times

Symbol	Parameter	Value	
		Min	Max
t_{RCR}	Read to CSn inactive	0	1.5 ns
t_{RAS}	Read address setup time	((WSTOEN) x t_{BCLK})- 4 ns	((WSTOEN) x t_{BCLK})
t_{RDS}	Read data setup time	12 ns	-
t_{RDH}	Read data hold time	0	
t_{RP}	Read pulse width	((WSTRD-WSTOEN+1) x t_{BCLK}) - 0.5 ns	((WSTRD-WSTOEN+1) x t_{BCLK}) + 2.5 ns
t_{AW}	ALE pulse width	(ALE_LENGTH x t_{BCLK}) - 3.5 ns	(ALE_LENGTH x t_{BCLK})
t_{AAS}	Address to ALE setup time	(ALE_LENGTH x t_{BCLK}) - 3.5 ns	(ALE_LENGTH x t_{BCLK})
t_{AAH}	Address to ALE hold time	(t_{BCLK}/2)- 1 ns	(t_{BCLK}/2) + 2 ns

7.12.5 SPI electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 46. SPI electrical characteristics

Symbol	Parameter	Test conditions	Value		Unit
			Typ	Max	
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master		24	MHz
		Slave		4	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall times	50pF load	0.1		V/ns
$t_{su(SS)}$	SS setup time	Slave	1		t_{PCLK}
$t_{h(SS)}$	SS hold time	Slave	1		
$t_{w(SCLKH)}$ $t_{w(SCLKL)}$	SCLK high and low time	Master Slave	1		
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master Slave	TBD 5		
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master Slave	TBD 6		
$t_{a(SO)}$	Data output access time	Slave		6	
$t_{dis(SO)}$	Data output disable time	Slave		6	
$t_{v(SO)}$	Data output valid time	Slave (after enable edge)		6	
$t_{h(SO)}$	Data output hold time		0		
$t_{v(MO)}$	Data output valid time	Master (before capture edge)	0.25		
$t_{h(MO)}$	Data output hold time		0.25		

Figure 30. SPI slave timing diagram with CPHA = 0

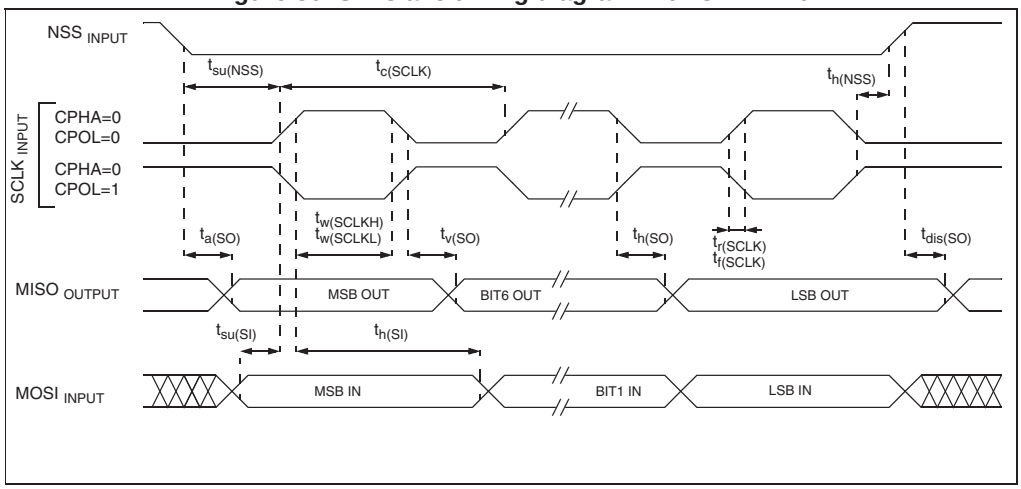
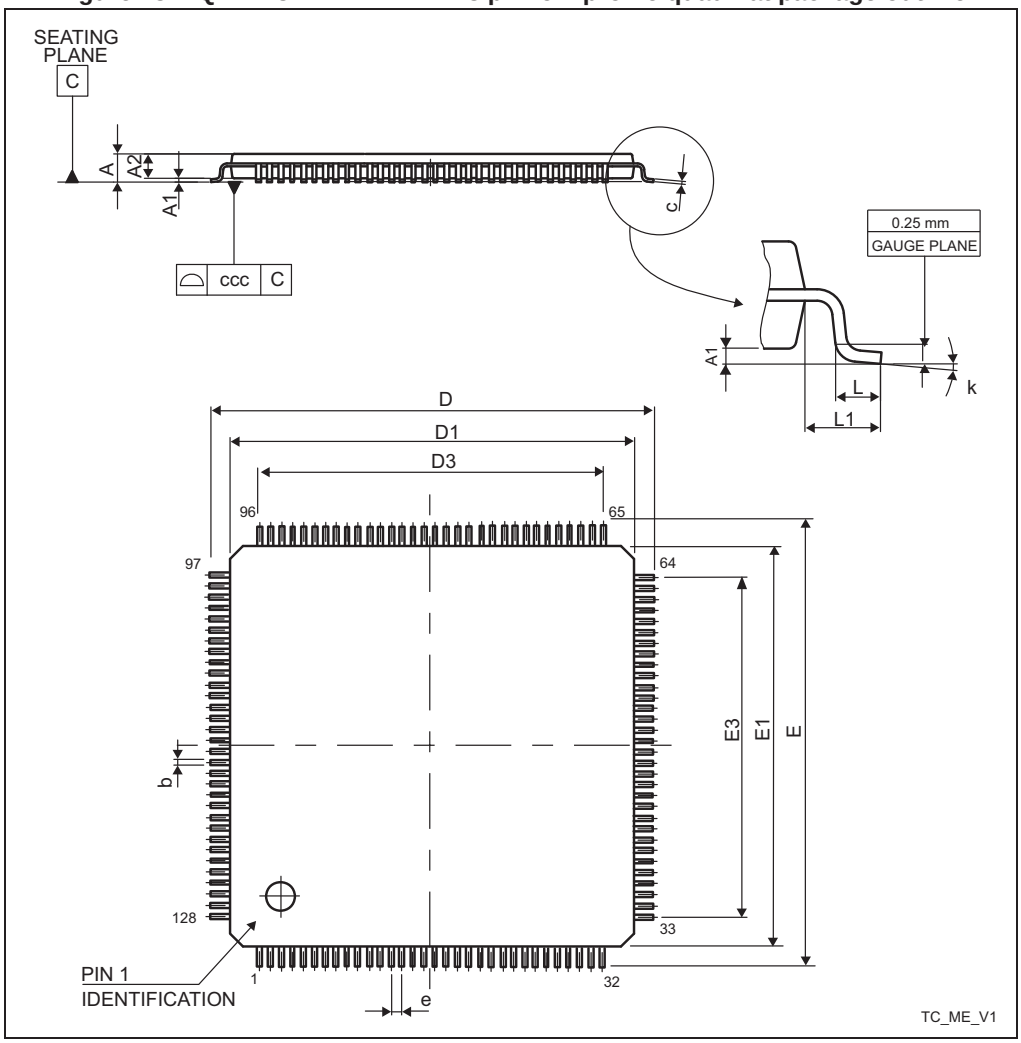


Figure 43. LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline



1. Drawing is not to scale.