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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str911faw44x6t

1 Description

STR91xFA is a series of ARM®-powered microcontrollers which combines a 16/32-bit ARM966E-S RISC processor core, dual-bank Flash memory, large SRAM for data or code, and a rich peripheral set to form an ideal embedded controller for a wide variety of applications such as point-of-sale terminals, industrial automation, security and surveillance, vending machines, communication gateways, serial protocol conversion, and medical equipment. The ARM966E-S core can perform single-cycle DSP instructions, good for speech processing, audio algorithms, and low-end imaging.

2 Device summary

Table 2. Device summary

Part number	Flash KB	RAM KB	Major peripherals	Package
STR910FAM32	**256+32**	64	**CAN, 40 I/Os**	**LQFP80, 12x12 mm**
STR910FAW32	**256+32**	64	**CAN, EMI, 80 I/Os**	**LQFP128, 14x14 mm**
STR910FAZ32	**256+32**	64	**CAN, EMI, 80 I/Os**	LFBGA144 10 x 10 x 1.7
STR911FAM42	**256+32**	96	**USB, CAN, 40 I/Os**	**LQFP80, 12x12mm**
STR911FAM44	**512+32**	96		
STR911FAM46	**1024+128**	96	**USB, CAN, 40 I/Os**	**LQFP80, 12x12mm**
STR911FAM47	**2048+128**	96		
STR911FAW42	**256+32**	96	**USB, CAN, EMI, 80 I/Os**	**LQFP128, 14x14mm**
STR911FAW44	**512+32**	96		
STR911FAW46	**1024+128**	96	**USB, CAN, EMI, 80 I/Os**	**LQFP128, 14x14mm**
STR911FAW47	**2048+128**	96		
STR912FAW32	**256+32**	64	**Ethernet, USB, CAN, EMI, 80 I/Os**	**LQFP128**
STR912FAW42	**256+32**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	**LQFP128**
STR912FAW44	**512+32**	96		
STR912FAW46	**1024+128**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	**LQFP128**
STR912FAW47	**2048+128**	96		
STR912FAZ42	**256+32**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	LFBGA144 10 x 10 x 1.7
STR912FAZ44	**512+32**	96		
STR912FAZ46	**1024+128**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	LFBGA144 10 x 10 x 1.7
STR912FAZ47	**2048+128**	96		

3.5 SRAM (64 Kbytes or 96 Kbytes)

A 32-bit wide SRAM resides on the CPU's Data TCM (D-TCM) interface, providing single-cycle data accesses. As shown in *Figure 1*, the D-TCM shares SRAM access with the Advanced High-performance Bus (AHB). Sharing is controlled by simple arbitration logic to allow the DMA unit on the AHB to also access the SRAM.

3.5.1 Arbitration

Zero-wait state access occurs for either the D-TCM or the AHB when only one of the two is requesting SRAM. When both request SRAM simultaneously, access is granted on an interleaved basis so neither requestor is starved, granting one 32-bit word transfer to each requestor before relinquishing SRAM to the other. When neither the D-TCM or the AHB are requesting SRAM, the arbiter leaves access granted to the most recent user (if D-TCM was last to use SRAM then the D-TCM will not have to arbitrate to get access next time).

The CPU may execute code from SRAM through the AHB. There are no wait states as long as the D-TCM is not contending for SRAM access and the AHB is not sharing bandwidth with peripheral traffic. The ARM966E-S CPU core has a small pre-fetch queue built into this instruction path through the AHB to look ahead and fetch instructions during idle bus cycles.

3.5.2 Battery backup

When a battery is connected to the designated battery backup pin (VBATT), SRAM contents are automatically preserved when the operating voltage on the main digital supplies (VDD and VDDQ are lost or sag below the LVD threshold. Automatic switchover to SRAM can be disabled by firmware if it is desired that the battery will power only the RTC and not the SRAM during standby.

3.6 DMA data movement

DMA channels on the Advanced High-performance Bus (AHB) take full advantage of the separate data path provided by the Harvard architecture, moving data rapidly and largely independent of the instruction path. There are two DMA units, one is dedicated to move data between the Ethernet interface and SRAM, the other DMA unit has eight programmable channels with 14 request signals to service other peripherals and interfaces (USB, SSP, ADC, UART, Timers, EMI, and external request pins). Both single word and burst DMA transfers are supported. Memory-to-memory transfers are supported in addition to memory-peripheral transfers. DMA access to SRAM is shared with D-TCM accesses, and arbitration is described in *Section 3.5.1*. Efficient DMA transfers are managed by firmware using linked list descriptor tables. Of the 16 DMA request signals, two are assigned to external inputs. The DMA unit can move data between external devices and resources inside the STR91xFA through the EMI bus.

Ethernet MII management timings

Figure 27. Ethernet MII management timing diagram

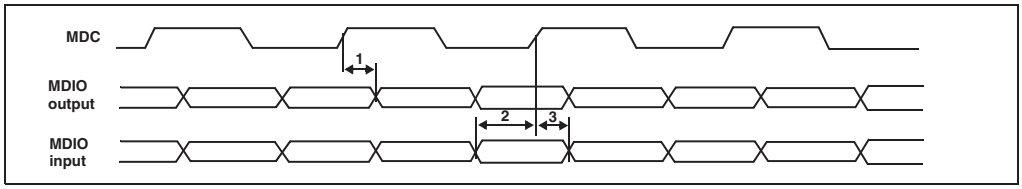
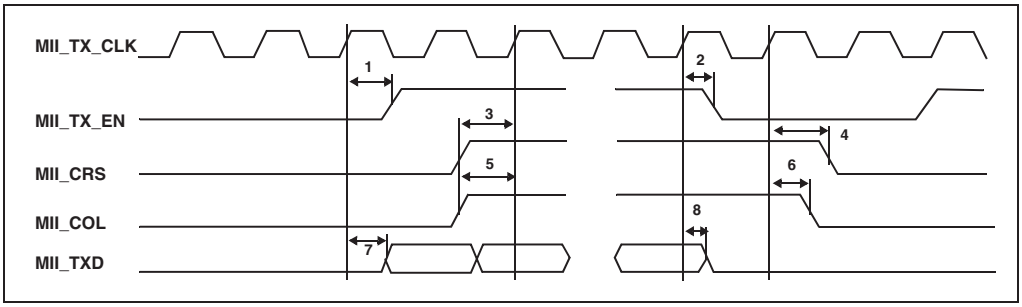


Table 42. Ethernet MII management timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	MDIO delay from rising edge of MDC	t_c(MDIO)		2.83	ns
2	MDIO setup time to rising edge of MDC	T_{su} (MDIO)	2.70		ns
3	MDIO hold time from rising edge of MDC	T_h (MDIO)	-2.03		ns

Ethernet MII transmit timings

Figure 28. Ethernet MII transmit timing diagram



7.13 ADC electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 47. General ADC electrical characteristics

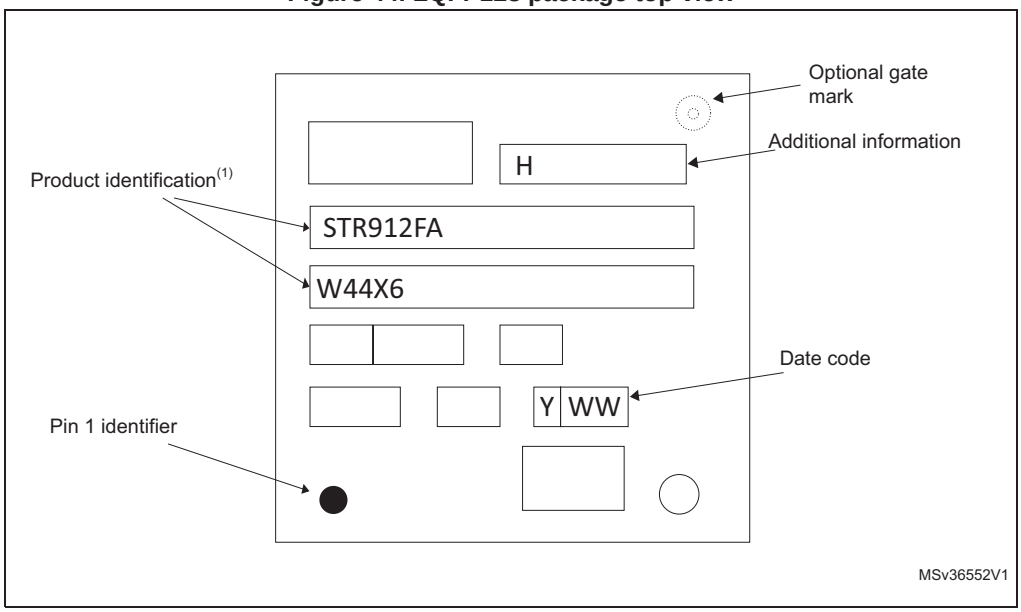
Symbol	Parameter[1]	Test conditions	Value			Unit
			Min	Typ	Max	
V_{AIN}	Input voltage range		0		AV_{REF}	V
RES	Resolution				10	Bits
N_{CH}	Number of input channels				8	N
f_{ADC}	ADC clock frequency				25	MHz
$t_{POR(ADC)}$	POR bit set to Standby mode				500	ms
$t_{ck\_off(ADC)}$	ADC clock disabled before conversion (2)				1	ms
t_{STAB}	Stabilization time				15	s
C_{IN}	Input capacitance			5		pF
E_D	Differential non-linearity	(3) (4)		1	3	LSB(5)
E_L	Integral non-linearity	(3)		3	6	LSB(5)
E_O	Offset error	(3)		3	6	LSB(5)
E_G	Gain error	(3)		0.5	2	LSB(5)
E_T	Total unadjusted error	(3)		4	6	LSB(5)
I_{ADC}	Power consumption			4.6		mA
I_{VREF}	Current on VREF input pin	(6) (7)			920	A

1. Guaranteed by design, not tested in production.
2. The ADC clock can be disabled by setting the ADC bit in the SCU_PCGR1 register or by setting the ACG bit in the SCU_GPIOANA register (for Rev H and higher)
3. Conditions: AV_{SS} = 0 V, AV_{DD} = 3.3 V f_{ADC} = 25 MHz.
4. The A/D is monotonic, there are no missing codes.
5. 1 LSB = (AV_{DD} - AV_{SS})/1024
6. Data based on characterization, not tested in production.
7. Conditions: V_{DD}=1.8 V, f_{CPU}=96 MHz , f_{ADC}=24 MHz

Marking of engineering samples for LQFP128

The following figure shows the engineering sample marking for the LQFP128 package. Only the information field containing the engineering sample marking is shown.

Figure 44. LQFP128 package top view



1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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