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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str911faw46x6

List of tables

List of figures

3.4.2 Branch cache (BC)

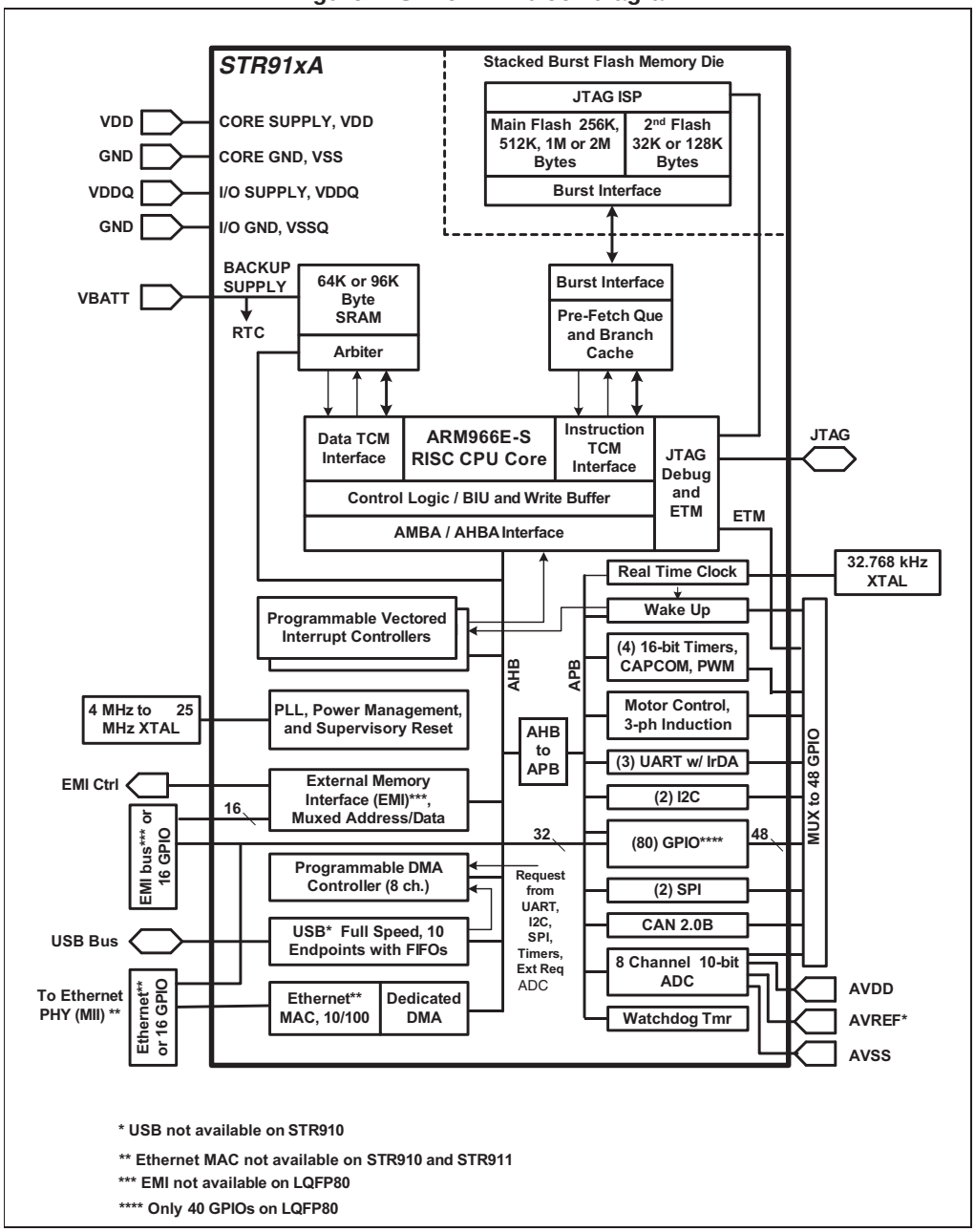
When instruction addresses are not sequential, such as a program branch situation, the PFQ would have to flush and reload which would cause the CPU to stall if no BC were present. Before reloading, the PFQ checks the BC to see if it contains the desired target branch address. The BC contains up to fifteen of the most recently taken branch addresses and the first eight instructions associated with each of these branches. This check is extremely fast, checking all fifteen BC entries simultaneously for a branch address match (cache hit). If there is a hit, the BC rapidly supplies the instruction and reduces the CPU stall. This gives the PFQ time to start pre-fetching again while the CPU consumes these eight instructions from the BC. The advantage here is that program loops (very common with embedded control applications) run very fast if the address of the loops are contained in the BC.

In addition, there is a 16th branch cache entry that is dedicated to the Vectored Interrupt Controller (VIC) to further reduce interrupt latency by eliminating the stall latency typically imposed by fetching the instruction that reads the interrupt vector address from the VIC.

3.4.3 Management of literals

Typical ARM architecture and compilers do not place literals (data constants) sequentially in Flash memory with the instructions that use them, but instead the literals are placed at some other address which looks like a program branch from the PFQ's point of view. The STR91xFA implementation of the ARM966E-S core has special circuitry to prevent flushing the PFQ when literals are encountered in program flow to keep performance at a maximum.

Figure 1. STR91xFA block diagram



3.7 Non-volatile memories

There are two independent 32-bit wide burst Flash memories enabling true read-while-write operation. The Flash memories are single-voltage erase/program with 20 year minimum data retention and 100K minimum erase cycles. The primary Flash memory is much larger than the secondary Flash.

Both Flash memories are blank when devices are shipped from ST. The CPU can boot only from Flash memory (configurable selection of which Flash bank).

Flash memories are programmed half-word (16 bits) at a time, but are erased by sector or by full array.

3.7.1 Primary Flash memory

Using the STR91xFA device configuration software tool and 3rd party Integrated Developer Environments, it is possible to specify that the primary Flash memory is the default memory from which the CPU boots at reset, or otherwise specify that the secondary Flash memory is the default boot memory. This choice of boot memory is non-volatile and stored in a location that can be programmed and changed only by JTAG In-System Programming. See *Section 6: Memory mapping*, for more detail.

The primary Flash memory has equal length 64K byte sectors. See *Table 3* for number of sectors per device type.

Table 3. Sectoring of primary Flash memory

Size of primary Flash	256 Kbytes	512 Kbytes	1 Mbyte	2 Mbytes
Number of sectors	4	8	16	32
Size of each sector	64 Kbytes		64 Kbytes	

3.7.2 Secondary Flash memory

The smaller of the two Flash memories can be used to implement a bootloader, capable of storing code to perform robust In-Application Programming (IAP) of the primary Flash memory. The CPU executes code from the secondary Flash, while updating code in the primary Flash memory. New code for the primary Flash memory can be downloaded over any of the interfaces on the STR91xFA (USB, Ethernet, CAN, UART, etc.)

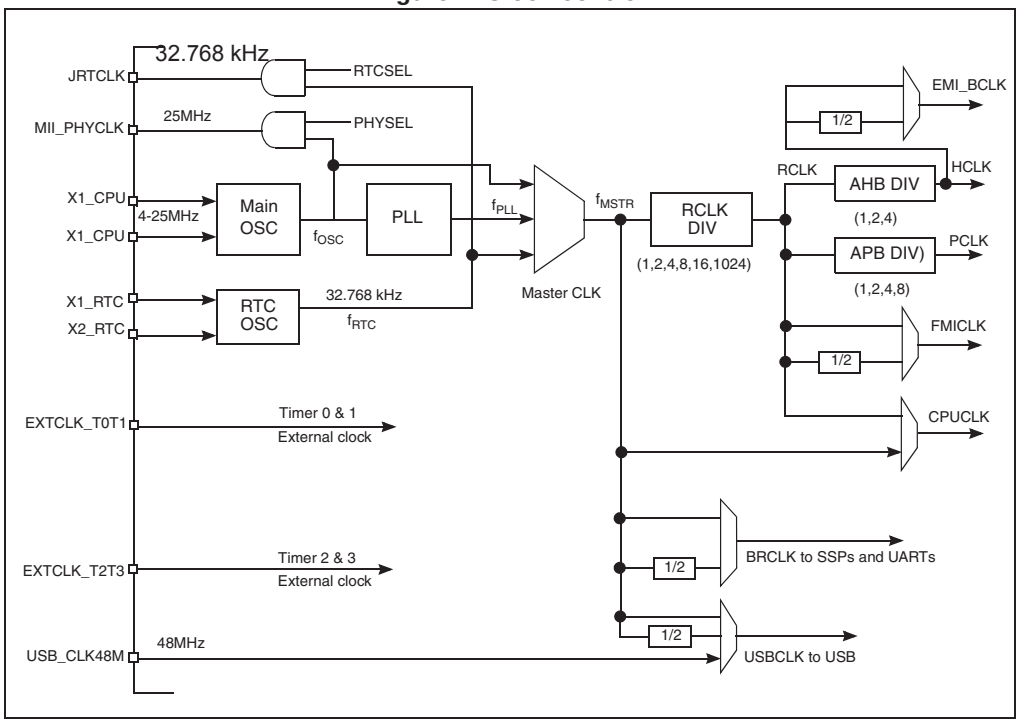
Additionally, the secondary Flash memory may also be used to store small data sets by emulating EEPROM through firmware, eliminating the need for external EEPROM memories. This raises the data security level because passcodes and other sensitive information can be securely locked inside the STR91xFA device.

The secondary Flash memory is sectored as shown in *Table 4* according to device type.

Both the primary Flash memory and the secondary Flash memory can be programmed with code and/or data using the JTAG In-System Programming (ISP) channel, totally independent of the CPU. This is excellent for iterative code development and for manufacturing.

As an option, there are a number of peripherals that do not have to receive a clock sourced from the CCU. The USB interface can receive an external clock on pin P2.7, TIM timers TIM0/ TIM1 can receive an external clock on pin P2.4, and timers TIM2/TIM3 on pin P2.5.

Figure 2. Clock control



3.10.2 Reference clock (RCLK)

The main clock (f_{MSTR}) can be divided to operate at a slower frequency reference clock (RCLK) for the ARM core and all the peripherals. The RCLK provides the divided clock for the ARM core, and feeds the dividers for the AHB, APB, External Memory Interface, and FMI units.

3.10.3 AHB clock (HCLK)

The RCLK can be divided by 1, 2 or 4 to generate the AHB clock. The AHB clock is the bus clock for the AHB bus and all bus transfers are synchronized to this clock. The maximum HCLK frequency is 96 MHz.

3.10.4 APB clock (PCLK)

The RCLK can be divided by 1, 2, 4 or 8 to generate the APB clock. The APB clock is the bus clock for the APB bus and all bus transfers are synchronized to this clock. Many of the peripherals that are connected to the AHB bus also use the PCLK as the source for external bus data transfers. The maximum PCLK frequency is 48 MHz.

3.10.5 Flash memory interface clock (FMICLK)

The FMICLK clock is an internal clock derived from RCLK, defaulting to RCLK frequency at power up. The clock can be optionally divided by 2. The FMICLK determines the bus bandwidth between the ARM core and the Flash memory. Typically, codes in the Flash memory can be fetched one word per FMICLK clock in burst mode. The maximum FMICLK frequency is 96 MHz.

3.10.6 UART and SSP clock (BRCLK)

BRCLK is an internal clock derived from f_{MSTR} that is used to drive the two SSP peripherals and to generate the Baud rate for the three on-chip UART peripherals. The frequency can be optionally divided by 2.

3.10.7 External memory interface bus clock (BCLK)

The BCLK is an internal clock that controls the EMI bus. All EMI bus signals are synchronized to the BCLK. The BCLK is derived from the HCLK and the frequency can be configured to be the same or half that of the HCLK. Refer to *Table 17 on page 66* for the maximum BCLK frequency (f_{BCLK}). The BCLK clock is available on the LFBGA package as an output pin.

3.10.8 USB interface clock

Special consideration regarding the USB interface: The clock to the USB interface must operate at 48 MHz and comes from one of three sources, selected under firmware control:

- CCU master clock output of 48 MHz.
- CCU master clock output of 96 MHz. An optional divided-by-two circuit is available to produce 48 MHz for the USB while the CPU system runs at 96MHz.
- STR91xFA pin P2.7. An external 48 MHz oscillator connected to pin P2.7 can directly source the USB while the CCU master clock can run at some frequency other than 48 or 96 MHz.

3.10.9 Ethernet MAC clock

Special consideration regarding the Ethernet MAC: The external Ethernet PHY interface device requires it's own 25 MHz clock source. This clock can come from one of two sources:

- A 25 MHz clock signal coming from a dedicated output pin (P5.2) of the STR91xFA. In this case, the STR91xFA must use a 25 MHz signal on its main oscillator input in order to pass this 25 MHz clock back out to the PHY device through pin P5.2. The advantage here is that an inexpensive 25 MHz crystal may be used to source a clock to both the STR91xFA and the external PHY device.
- An external 25 MHz oscillator connected directly to the external PHY interface device. In this case, the STR91xFA can operate independent of 25 MHz.

3.10.10 External RTC calibration clock

The RTC_CLK can be enabled as an output on the JRTCK pin. The RTC_CLK is used for RTC oscillator calibration. The RTC_CLK is active in Sleep mode and can be used as a system wake up control clock.

3.18.1 Packet buffer interface (PBI)

The PBI manages a set of buffers inside the 2 Kbyte Packet Buffer, both for transmission and reception. The PBI will choose the proper buffer according to requests coming from the USB Serial Interface Engine (SIE) and locate it in the Packet SRAM according to addresses pointed by endpoint registers. The PBI will also auto-increment the address after each exchanged byte until the end of packet, keeping track of the number of exchanged bytes and preventing buffer overrun. Special support is provided by the PBI for isochronous and bulk transfers, implementing double-buffer usage which ensures there is always an available buffer for a USB packet while the CPU uses a different buffer.

3.18.2 DMA

A programmable DMA channel may be assigned by CPU firmware to service the USB interface for fast and direct transfers between the USB bus and SRAM with little CPU involvement. This DMA channel includes the following features:

- Direct USB Packet Buffer SRAM to system SRAM transfers of receive packets, by descriptor chain for bulk or isochronous endpoints.
- Direct system SRAM to USB Packet Buffer SRAM transfers of transmit packets, by descriptor chain for bulk or isochronous endpoints.
- Linked-list descriptor chain support for multiple USB packets

3.18.3 Suspend mode

CPU firmware may place the USB interface in a low-power suspend mode when required, and the USB interface will automatically wake up asynchronously upon detecting activity on the USB pins.

3.19 CAN 2.0B interface

The STR91xFA provides a CAN interface complying with CAN protocol version 2.0 parts A and B. An external CAN transceiver device connected to pins CAN_RX and CAN_TX is required for connection to the physical CAN bus.

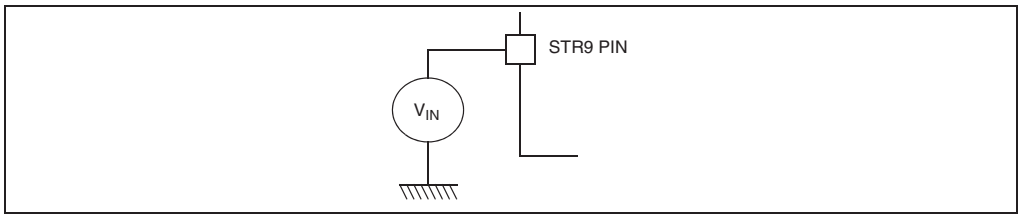
The CAN interface manages up to 32 Message Objects and Identifier Masks using a Message SRAM and a Message Handler. The Message Handler takes care of low-level CAN bus activity such as acceptance filtering, transfer of messages between the CAN bus and the Message SRAM, handling of transmission requests, and interrupt generation. The CPU has access to the Message SRAM via the Message Handler using a set of 38 control registers.

The follow features are supported by the CAN interface:

- Bit rates up to 1 Mbps
- Disable Automatic Retransmission mode for Time Triggered CAN applications
- 32 Message Objects
- Each Message Object has its own Identifier Mask
- Programmable FIFO mode
- Programmable loopback mode for self-test operation

The CAN interface is not supported by DMA.

Figure 11. Pin input voltage



7.2 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages. It is also recommended to ground any unused input pin to reduce power consumption and minimize noise.

Table 9. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
V_{DD}	Voltage on VDD pin with respect to ground V_{SS}	-0.3	2.4	V
V_{DDQ}	Voltage on VDDQ pin with respect to ground V_{SS}	-0.3	4.0	V
V_{BATT}	Voltage on VBATT pin with respect to ground V_{SS}	-0.3	4.0	V
AV_{DD}	Voltage on AVDD pin with respect to ground V_{SS} (128-pin and 144-ball packages)	-0.3	4.0	V
AV_{REF}	Voltage on AVREF pin with respect to ground V_{SS} (128-pin and 144-ball packages)	-0.3	4.0	V
AV_{REF_AVDD}	Voltage on AVREF_AVDD pin with respect to Ground V_{SS} (80-pin package)	-0.3	4.0	V
V_{IN}	Voltage on 5V tolerant pins with respect to ground V_{SS}	-0.3	5.5	V
	Voltage on any other pin with respect to ground V_{SS}	-0.3	4.0	V
T_{ST}	Storage Temperature	-55	+150	°C
T_J	Junction Temperature		+125	°C
ESD	ESD Susceptibility (Human Body Model)	2000		V

Note: Stresses exceeding above listed recommended "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN}>V_{DDQ}$ or $V_{IN}<V_{SSQ}$) the voltage on pins with respect to ground (V_{SSQ}) must not exceed the recommended values.

7.7 Clock and timing characteristics

Table 17. Internal clock frequencies

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{MSTR}	CCU Master clock		32.768		$f_{CPUCLKmax}$	kHz
f_{CPUCLK}	CPU Core frequency	Flash size ≤512 KB Executing from SRAM			96	MHz
		Flash size ≤512 KB Executing from Flash			96	MHz
		Flash size = 1 MB / 2 MB, executing from SRAM or Flash V_{DD} ≥1.77 V			96	MHz
		Flash size = 1 MB / 2 MB, executing from SRAM or Flash V_{DD} ≥ 1.65 V			85	MHz
f_{PCLK}	Peripheral clock for APB				48	MHz
f_{HCLK}	Peripheral clock for AHB				$f_{CPUCLKmax}$	MHz
f_{OSC}	Clock input		4		25	MHz
f_{FMICLK}	FMI Flash bus clock (internal clock)				$f_{CPUCLKmax}$	MHz
		Flash size = 1 MB / 2 MB, write operation to Flash memory or Flash registers			48	MHz
f_{BCLK}	External memory bus clock				$f_{CPUCLKmax}$	MHz
f_{RTC}	RTC clock		32.768			kHz
f_{EMAC}	EMAC PHY clock		25			MHz
f_{USB}	USB clock		48			MHz
$f_{TIMCLKEXT}$	Timer external clock		0		$f_{PCLKmax}/4$ = 12	MHz
f_{TIMCLK}	Timer clock when internal clock (PCLK) is selected		0		$f_{PCLKmax}$ = 48	MHz

7.8 Memory characteristics

7.8.1 SRAM characteristics

Table 23. SRAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DR}	Supply voltage for data retention(1)	T_A= 85 °C (worst case)	1.1			V

1. Guaranteed by characterization, not tested in production.

7.8.2 Flash memory characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Note: Flash read access for sequential addresses is 0 wait states at 96 MHz. Flash read access for non-sequential accesses requires 2 wait states when FMI clock is above 66 MHz. See STR91xF Flash Programming Manual for more information.

Table 24. Flash memory program/erase characteristics (Flash size ≤ 512 KB)

Parameter		Test conditions	Value			Unit
			Typ(1)	Typ after 100K W/E cycles(1)	Max	
Bank erase	Primary bank (512 Kbytes)		8	9	11.5	s
	Primary bank (256 Kbytes)		4	4.5	6	s
	Secondary bank (32 Kbytes)		700	750	950	ms
Sector erase	Of primary bank (64 Kbytes)		1300	1400	1800	ms
	Of secondary bank (8 Kbytes)		300	320	450	ms
Bank program	Primary bank (512 Kbytes)		3700	4700	5100	ms
	Primary bank (256 Kbytes)		1900	2000	2550	ms
	Secondary bank (32 Kbytes)		250	260	320	ms
Sector program	Of primary bank (64 Kbytes)		500	520	640	ms
	Of secondary bank (8 Kbytes)		60	62	80	ms
Word program		Half word (16 bits)	8	9	11	µs

1. V_{DD} = 1.8 V, V_{DDQ} = 3.3 V, T_A = 25 °C.

Mux write

Figure 20. Mux write diagram

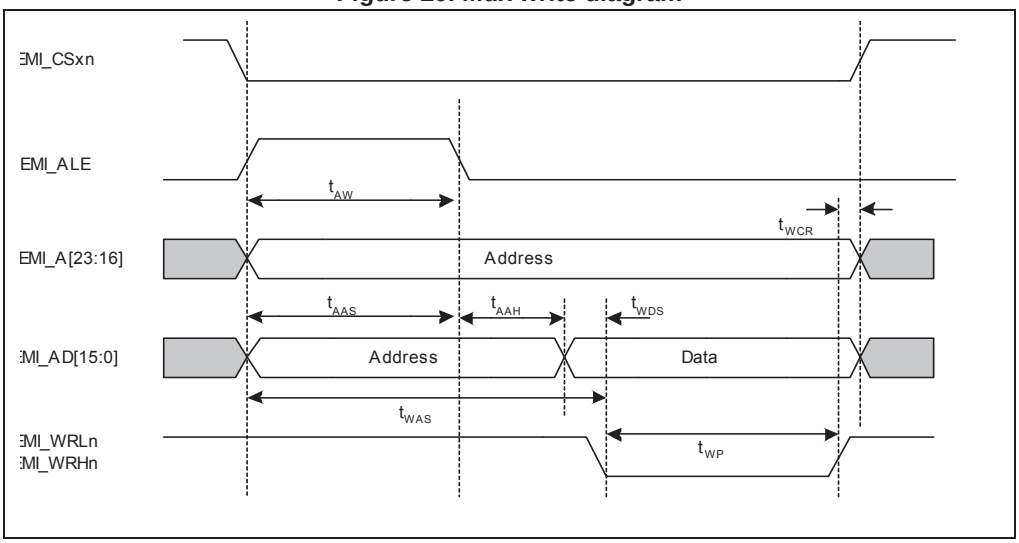


Table 35. Mux write times

Symbol	Parameter	Value	
		Min	Max
t_{WCR}	WRn to CSn inactive	(t_{BCLK}/2) - 2ns	(t_{BCLK}/2) + 2ns
t_{WAS}	Write address setup time	(WSTWEN + 1/2) x t_{BCLK} - 2.5 ns	(WSTWEN + 1/2) x t_{BCLK} + 2 ns
t_{WDS}	Write data setup time	((WSTWEN - ALE_LENGTH) x t_{BCLK}) - 2 ns	((WSTWEN - ALE_LENGTH) x t_{BCLK}) + 1 ns
t_{WP}	Write pulse width	((WSTWR-WSTWEN + 1) x t_{BCLK}) - 1 ns	((WSTWR-WSTWEN + 1) x $t_{BCLK)}$ + 1.5 ns
t_{AW}	ALE pulse width	(ALE_LENGTH x t_{BCLK})- 3.5 ns	(ALE_LENGTH x t_{BCLK})
t_{AAS}	Address to ALE setup time	(ALE_LENGTH x t_{BCLK})- 3.5 ns	(ALE_LENGTH x t_{BCLK})
t_{AAH}	Address to ALE hold time	(t_{BCLK}/2) - 1 ns	(t_{BCLK}/2) + 2 ns

7.12 Communication interface electrical characteristics

7.12.1 10/100 Ethernet MAC electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Ethernet MII interface timings

Figure 25. MII_RX_CLK and MII_TX_CLK timing diagram

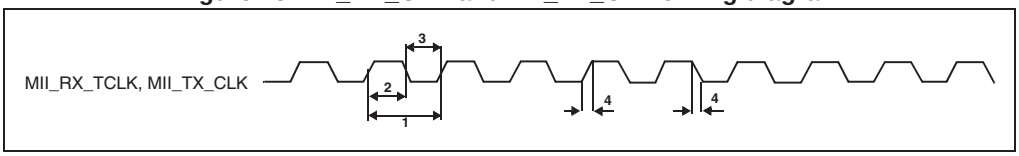


Table 40. MII_RX_CLK and MII_TX_CLK timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	Cycle time	t_c(CLK)	40		ns
2	Pulse duration high	t_{HIGH}(CLK)	40%	60%	
3	Pulse duration low	t_{LOW}(CLK)	40%	60%	
4	Transition time	t_t(CLK)		1	ns

Figure 26. MDC timing diagram

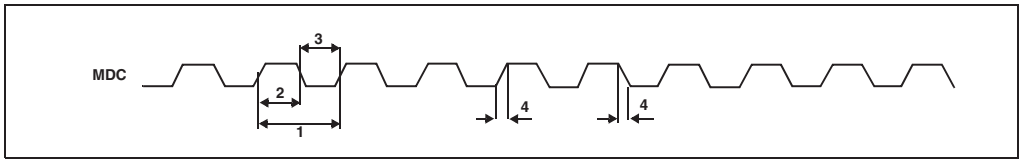


Table 41. MDC timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	Cycle time	t_c(MDC)	266		ns
2	Pulse duration high	t_{HIGH}(MDC)	40%	60%	
3	Pulse duration low	t_{LOW}(MDC)	40%	60%	
4	Transition time	t_t(MDC)		1	ns

Table 48. ADC conversion time (silicon Rev G)

Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$2*16/f_{ADC}$		$3*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	1.33		2	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			500	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev G. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained on conversions started by trigger in single mode
4. All sucessive conversions in continuous and scan modes.

Table 49. ADC conversion time (silicon Rev H and higher)

Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$1*16/f_{ADC}$		$2*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	0.66		1.33	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			750	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps
$t_{CONV(FT)}$	Fast trigger mode conversion time(5)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(FT)	Fast trigger mode throughput rate(6)	f_{ADC} = 24 MHz	100		1200	ksps

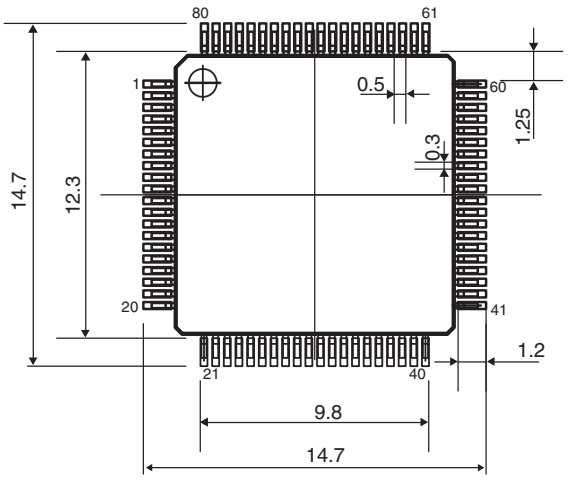
1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev H and higher. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained from conversions started by trigger in single mode
4. All successive conversions in continuous and scan modes.
5. Conversion started by trigger when automatic clock gated mode enabled. Fast trigger mode is available only in devices with silicon Rev H and higher.
6. Value obtained from conversions started by fast trigger in single mode

Table 50. LQFP80 12 x12 mm low-profile quad flat package mechanical data

Dim.	mm			inches[1]		
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	14.000	-	-	0.5512	-
D1	-	12.000	-	-	0.4724	-
D2	-	9.500	-	-	0.3740	-
E	-	14.000	-	-	0.5512	-
E1	-	12.000	-	-	0.4724	-
E3	-	9.500	-	-	0.3740	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc		0.080			0.0031	
k	0.0°	-	7.0°	0.0°	-	7.0°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. LQFP80 - 80 pin, 12 x 12 mm low-profile quad flat package footprint

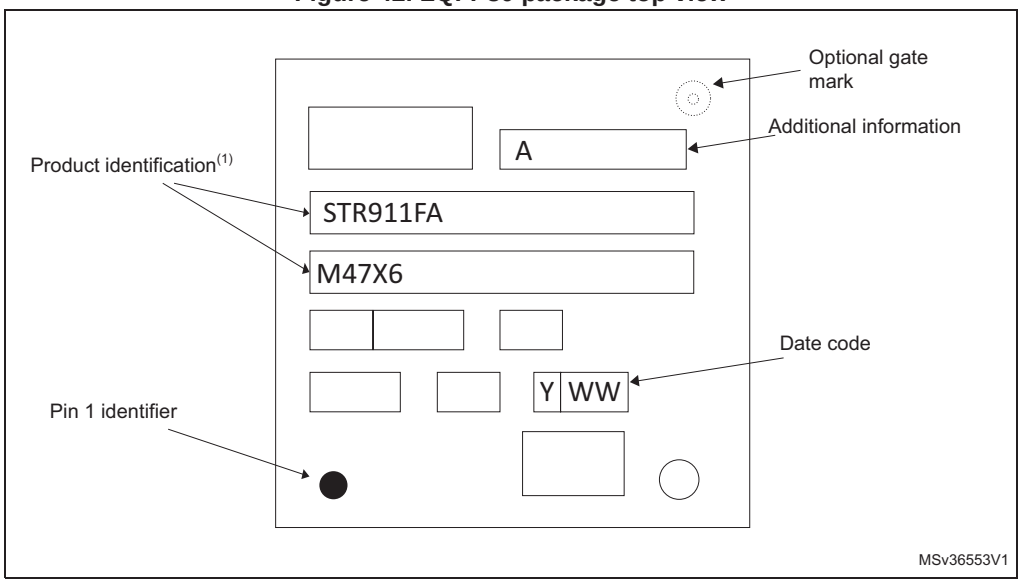


1. Dimensions are expressed in millimeters.

Marking of engineering samples for LQFP80

The following figure shows the engineering sample marking for the LQFP80 package. Only the information field containing the engineering sample marking is shown

Figure 42. LQFP80 package top view

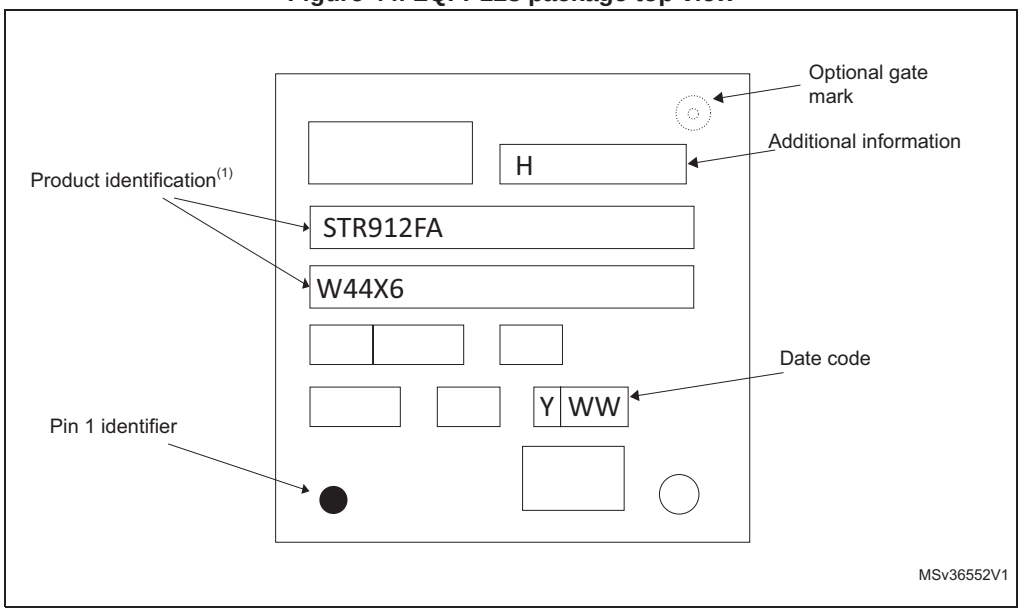


1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Marking of engineering samples for LQFP128

The following figure shows the engineering sample marking for the LQFP128 package. Only the information field containing the engineering sample marking is shown.

Figure 44. LQFP128 package top view



1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 45. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline

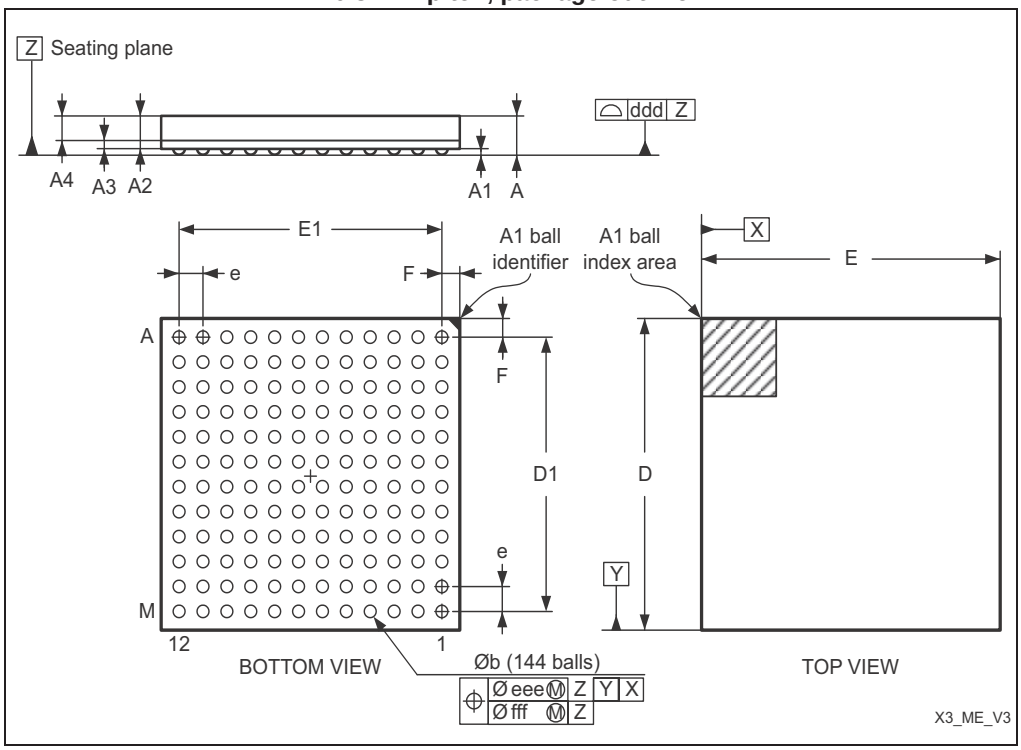


Table 52.LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A[2]	-	-	1.700			0.0669
A1	0.210	-	-	0.0083		
A2	-	1.060	-		0.0417	
A3		0.026			0.0010	
A4	-	0.800	-	-	0.0315	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	8.800	-	-	0.3465	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	0.100			0.0039		
eee	0.150			0.0059		
fff	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.

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