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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str911faw47x6

List of tables

3 Functional overview

3.1 System-in-a-package (SiP)

The STR91xFA is a SiP device, comprised of two stacked die. One die is the ARM966E-S CPU with peripheral interfaces and analog functions, and the other die is the burst Flash. The two die are connected to each other by a custom high-speed 32-bit burst memory interface and a serial JTAG test/programming interface.

3.2 Package choice

STR91xFA devices are available in 128-pin (14 x 14 mm) and 80-pin (12 x 12 mm) LQFP and LFBGA144 (10 x 10 mm) packages. Refer to *Table 2: Device summary on page 11* for a list of available peripherals for each of the package choices.

3.3 ARM966E-S CPU core

The ARM966E-S core inherently has separate instruction and data memory interfaces (Harvard architecture), allowing the CPU to simultaneously fetch an instruction, and read or write a data item through two Tightly-Coupled Memory (TCM) interfaces as shown in *Figure 1*. The result is streamlined CPU Load and Store operations and a significant reduction in cycle count per instruction. In addition to this, a 5-stage pipeline is used to increase the amount of operational parallelism, giving the most performance out of each clock cycle.

Ten DSP-enhanced instruction extensions are supported by this core, including single-cycle execution of 32x16 Multiply-Accumulate, saturating addition/subtraction, and count leading-zeros.

The ARM966E-S core is binary compatible with 32-bit ARM7 code and 16-bit Thumb® code.

3.4 Burst Flash memory interface

A burst Flash memory interface (*Figure 1*) has been integrated into the Instruction TCM (I-TCM) path of the ARM966E-S core. Also in this path is an 8-instruction Pre-Fetch Queue (PFQ) and a 15-entry Branch Cache (BC), enabling the ARM966E-S core to perform up to 96 MIPS while executing code directly from Flash memory. This architecture provides high performance levels without a costly instruction SRAM, instruction cache, or external SDRAM. Eliminating the instruction cache also means interrupt latency is reduced and code execution becomes more deterministic.

3.4.1 Pre-fetch queue (PFQ)

As the CPU core accesses sequential instructions through the I-TCM, the PFQ always looks ahead and will pre-fetch instructions, taking advantage any idle bus cycles due to variable length instructions. The PFQ will fetch 32-bits at a time from the burst Flash memory at a rate of up to 96 MHz.

3.4.2 Branch cache (BC)

When instruction addresses are not sequential, such as a program branch situation, the PFQ would have to flush and reload which would cause the CPU to stall if no BC were present. Before reloading, the PFQ checks the BC to see if it contains the desired target branch address. The BC contains up to fifteen of the most recently taken branch addresses and the first eight instructions associated with each of these branches. This check is extremely fast, checking all fifteen BC entries simultaneously for a branch address match (cache hit). If there is a hit, the BC rapidly supplies the instruction and reduces the CPU stall. This gives the PFQ time to start pre-fetching again while the CPU consumes these eight instructions from the BC. The advantage here is that program loops (very common with embedded control applications) run very fast if the address of the loops are contained in the BC.

In addition, there is a 16th branch cache entry that is dedicated to the Vectored Interrupt Controller (VIC) to further reduce interrupt latency by eliminating the stall latency typically imposed by fetching the instruction that reads the interrupt vector address from the VIC.

3.4.3 Management of literals

Typical ARM architecture and compilers do not place literals (data constants) sequentially in Flash memory with the instructions that use them, but instead the literals are placed at some other address which looks like a program branch from the PFQ's point of view. The STR91xFA implementation of the ARM966E-S core has special circuitry to prevent flushing the PFQ when literals are encountered in program flow to keep performance at a maximum.

Table 4. Sectoring of secondary Flash memory

Size of secondary Flash	32 Kbytes	128 Kbytes
Number of sectors	4	8
Size of each sector	8 Kbytes	16 Kbytes

3.8 One-time-programmable (OTP) memory

There are 32 bytes of OTP memory ideally suited for serial numbers, security keys, factory calibration constants, or other permanent data constants. These OTP data bytes can be programmed only one time through either the JTAG interface or by the CPU, and these bytes can never be altered afterwards. As an option, a “lock bit” can be set by the JTAG interface or the CPU which will block any further writing to the this OTP area. The “lock bit” itself is also OTP. If the OTP array is unlocked, it is always possible to go back and write to an OTP byte location that has not been previously written, but it is never possible to change an OTP byte location if any one bit of that particular byte has been written before. The last two OTP bytes (bytes 31 and 30) are reserved for the STR91xFA product ID and revision level.

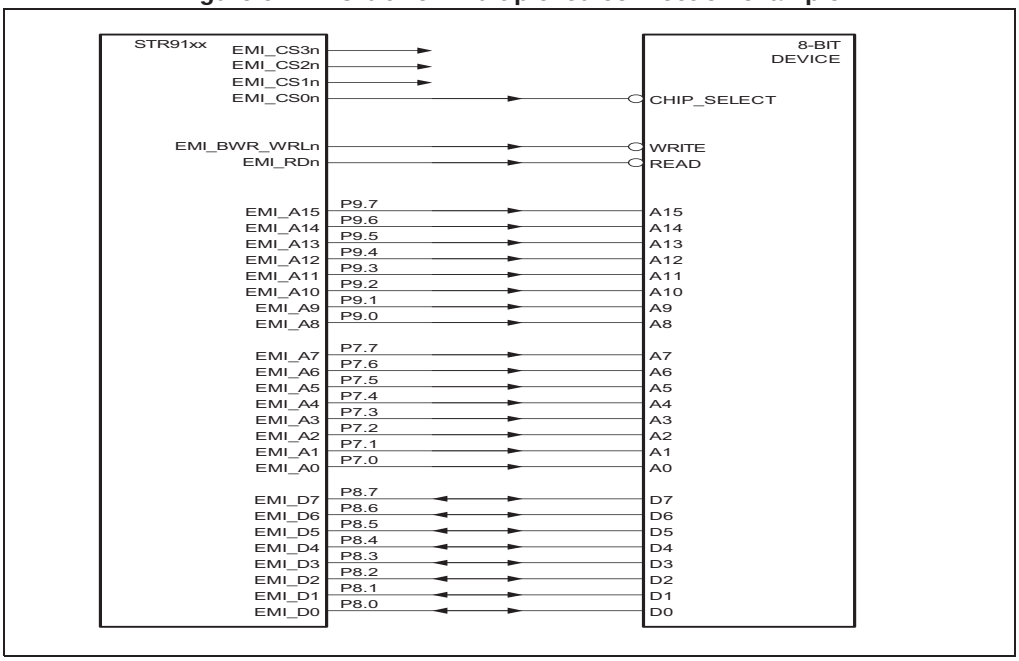
3.8.1 Product ID and revision level

OTP bytes 31 and 30 are programmed at ST factory before shipment and may be read by firmware to determine the STR91xFA product type and silicon revision so it can optionally take action based on the silicon on which it is running. In Rev H devices and 1MB/2MB Rev A devices, byte 31 contains the major family identifier of "9" (for STR9) in the high-nibble location and the minor family identifier in the low nibble location, which can be used to determine the size of primary flash memory. In all devices, byte 30 contains the silicon revision level indicator. See *Table 5* for values related to the revisions of STR9 production devices and size of primary Flash memory. See *Section 8* for details of external identification of silicon revisions.

Table 5. Product ID and revision level values

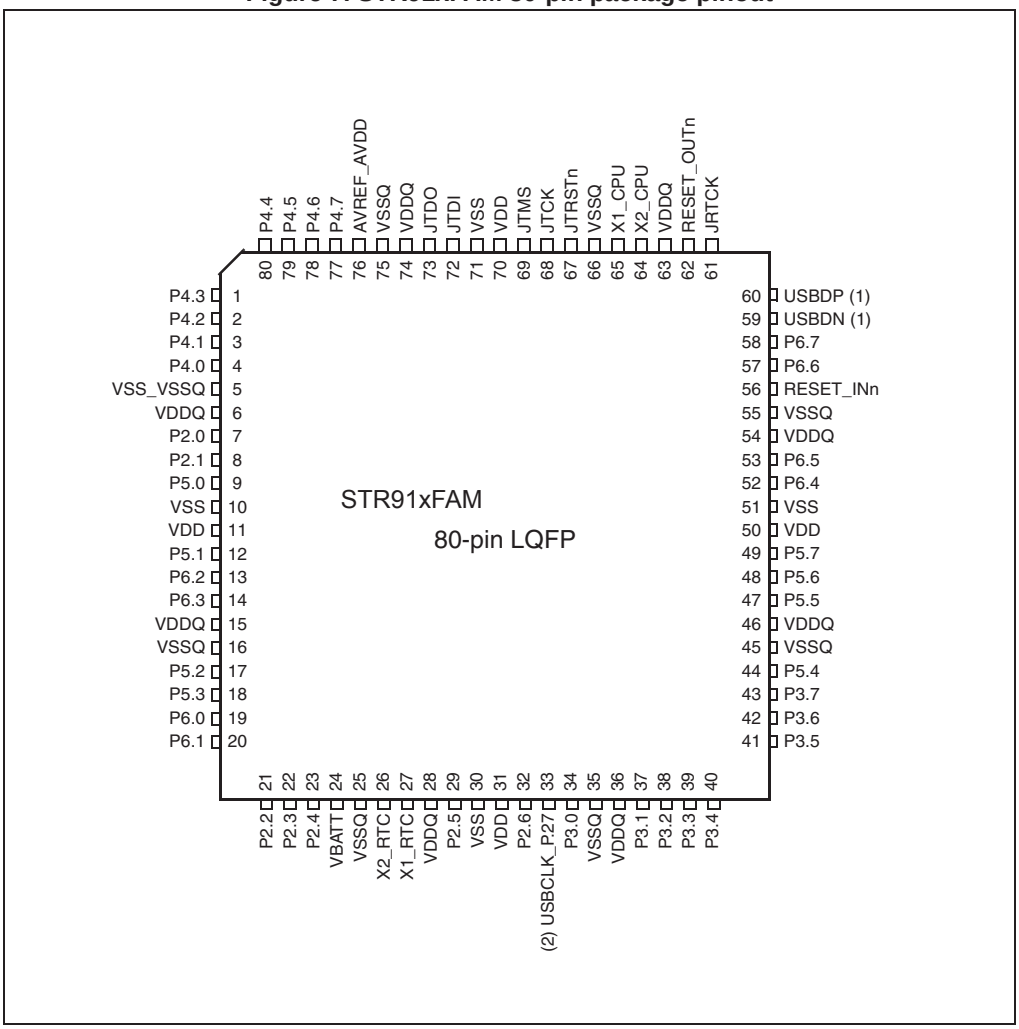
Production salestype	Silicon revision	Size of primary Flash	OTP byte 31	OTP byte 30
STR91xFAxxxxx	Rev G	256K or 512K	91h	20h
STR91xFAxxxxx	Rev H	256K	90h	21h
STR91xFAxxxxx	Rev H	512K	91h	21h
STR91xFAx46xx	Rev A	1024K	92h	21h
STR91xFAx47xx	Rev A	2048K	93h	21h

Figure 6. EMI 8-bit non-multiplexed connection example



5 Pin description

Figure 7. STR91xFAM 80-pin package pinout



1. NU (Not Used) on STR910FAM devices. Pin 59 is not connected, pin 60 must be pulled up by a 1.5Kohm resistor to VDDQ.
2. No USBCLK function on STR910FAM devices.

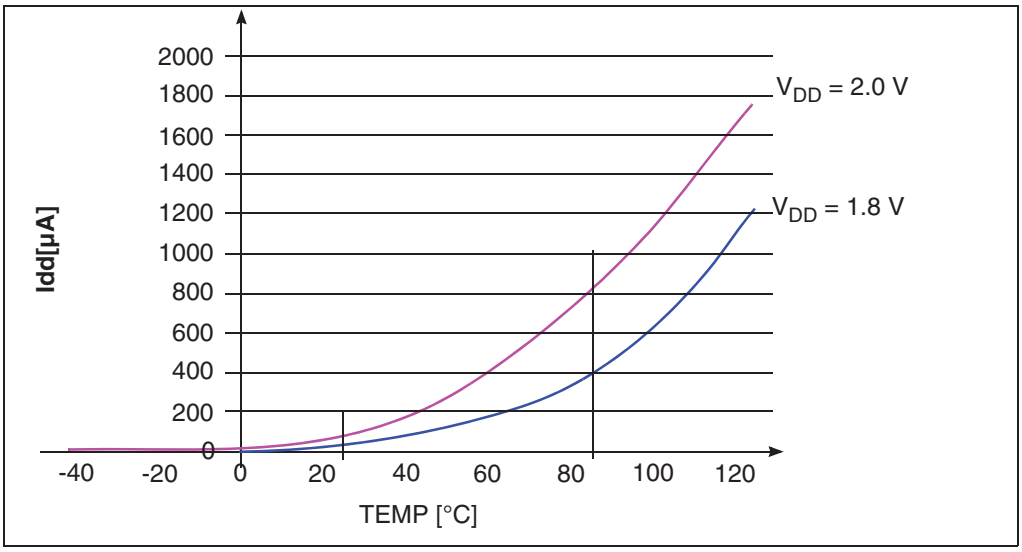
Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
29	45	J5	P2.5	I/O	GPIO_2.5, GP Input, HiZ	EXTCLK_T2T3Ext clk timer2/3	SSP0_MOSI, SSP slv dat in	GPIO_2.5, GP Output	SSP0_MOSI, SSP mstr dat out	ETM_PSTAT1, ETM pipe status
32	53	G6	P2.6	I/O	GPIO_2.6, GP Input, HiZ	-	SSP0_MISO, SSP mstr data in	GPIO_2.6, GP Output	SSP0_MISO, SSP slv data out	ETM_PSTAT2, ETM pipe status
33	54	L7	USBCLK_P2.7	I/O	GPIO_2.7, GP Input, HiZ	USB_CLK48M, 48MHz to USB	SSP0_NSS, SSP slv sel in	GPIO_2.7, GP Output	SSP0_NSS, SSP mstr sel out	ETM_TRSYNC, ETM trace sync
34	55	K7	P3.0	I/O	GPIO_3.0, GP Input, HiZ	DMA_RQST0, Ext DMA requst	UART0_RxD, UART rcv data	GPIO_3.0, GP Output	UART2_TX, UART xmit data	TIM0_OCMP1, Out comp/PWM
37	59	M10	P3.1	I/O	GPIO_3.1, GP Input, HiZ	DMA_RQST1, Ext DMA requst	UART2_RxD, UART rcv data	GPIO_3.1, GP Output	UART0_TX, UART xmit data	TIM1_OCMP1, Out comp/PWM
38	60	M11	P3.2	I/O	GPIO_3.2, GP Input, HiZ	EXINT2, External Intr	UART1_RxD, UART rcv data	GPIO_3.2, GP Output	CAN_TX, CAN Tx data	UART0_DTR, Data Trmnl Rdy
39	61	J8	P3.3	I/O	GPIO_3.3, GP Input, HiZ	EXINT3, External Intr	CAN_RX, CAN rcv data	GPIO_3.3, GP Output	UART1_TX, UART xmit data	UART0_RTS, Ready To Send
40	63	L9	P3.4	I/O	GPIO_3.4, GP Input, HiZ	EXINT4, External Intr	SSP1_SCLK, SSP slv clk in	GPIO_3.4, GP Output	SSP1_SCLK, SSP mstr clk out	UART0_TX, UART xmit data
41	65	L10	P3.5	I/O	GPIO_3.5, GP Input, HiZ	EXINT5, External Intr	SSP1_MISO, SSP mstr data in	GPIO_3.5, GP Output	SSP1_MISO, SSP slv data out	UART2_TX, UART xmit data
42	66	M12	P3.6	I/O	GPIO_3.6, GP Input, HiZ	EXINT6, External Intr	SSP1_MOSI, SSP slv dat in	GPIO_3.6, GP Output	SSP1_MOSI, SSP mstr dat out	CAN_TX, CAN Tx data
43	68	K11	P3.7	I/O	GPIO_3.7, GP Input, HiZ	EXINT7, External Intr	SSP1_NSS, SSP slv select in	GPIO_3.7, GP Output	SSP1_NSS, SSP mstr sel out	TIM1_OCMP1, Out comp/PWM
4	3	C2	P4.0	I/O	GPIO_4.0, GP Input, HiZ	ADC0, ADC input chnl	TIM0_ICAP1, Input Capture	GPIO_4.0, GP Output	TIM0_OCMP1, Out comp/PWM	ETM_PCK0, ETM Packet
3	2	B2	P4.1	I/O	GPIO_4.1, GP Input, HiZ	ADC1, ADC input chnl	TIM0_ICAP2, Input Capture	GPIO_4.1, GP Output	TIM0_OCMP2, Out comp	ETM_PCK1, ETM Packet
2	1	A1	P4.2	I/O	GPIO_4.2, GP Input, HiZ	ADC2, ADC input chnl	TIM1_ICAP1, Input Capture	GPIO_4.2, GP Output	TIM1_OCMP1, Out comp/PWM	ETM_PCK2, ETM Packet
1	128	B3	P4.3	I/O	GPIO_4.3, GP Input, HiZ	ADC3, ADC input chnl	TIM1_ICAP2, Input Capture	GPIO_4.3, GP Output	TIM1_OCMP2, Out comp	ETM_PCK3, ETM Packet
80	127	C4	P4.4	I/O	GPIO_4.4, GP Input, HiZ	ADC4, ADC input chnl	TIM2_ICAP1, Input Capture	GPIO_4.4, GP Output	TIM2_OCMP1, Out comp/PWM	ETM_PSTAT0, ETM pipe status
79	126	B4	P4.5	I/O	GPIO_4.5, GP Input, HiZ	ADC5, ADC input chnl	TIM2_ICAP2, Input Capture	GPIO_4.5, GP Output	TIM2_OCMP2, Out comp	ETM_PSTAT1, ETM pipe status
78	125	A4	P4.6	I/O	GPIO_4.6, GP Input, HiZ	ADC6, ADC input chnl	TIM3_ICAP1, Input Capture	GPIO_4.6, GP Output	TIM3_OCMP1, Out comp/PWM	ETM_PSTAT2, ETM pipe status
77	124	D5	P4.7	I/O	GPIO_4.7, GP Input, HiZ	ADC7, ADC input chnl /ADC Ext. trigger	TIM3_ICAP2, Input Capture	GPIO_4.7, GP Output	TIM3_OCMP2, Out comp	ETM_TRSYNC, ETM trace sync
9	12	E4	P5.0	I/0	GPIO_5.0, GP Input, HiZ	EXINT8, External Intr	CAN_RX, CAN rcv data	GPIO_5.0, GP Output	ETM_TRCLK, ETM trace clock	UART0_TX, UART xmit data

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	8	L2	VSSQ	G	Digital Ground for !/O and USB	N/A				
16	24	K4	VSSQ	G						
35	56	C5	VSSQ	G						
-	-	D4	VSSQ	G						
45	72	G5	VSSQ	G						
55	87	J7	VSSQ	G						
25	40	A8	VSSQ	G						
66	105	F8	VSSQ	G						
75	121	L12	VSSQ	G						
11	17	F4	VDD	V	V Source for CPU. 1.65 V - 2.0 V	N/A				
31	49	D7	VDD	V						
50	81	L6	VDD	V						
70	112	G11	VDD	V						
10	16	F3	VSS	G	Digital Ground for CPU	N/A				
30	48	H5	VSS	G						
51	82	G10	VSS	G						
71	113	E7	VSS	G						
-	-	C9	PLLV DDQ	V	V Source for PLL 2.7 to 3.6 V	N/A				
-	-	B8	PLLV SSQ	G	Digital Ground for PLL					

Figure 15. Sleep mode current vs temperature with LVD on



7.6.1 Typical power consumption for frequencies below 10 MHz

The following conditions apply to *Table 16*:

- Program is executed from Flash. The program consists of an infinite loop.
- A standard crystal source is used.
- The PLL is off.
- All clock dividers are with their default values.

Table 16. Typical current consumption at 25 °C

Symbol	Parameter		Test conditions	Typical current on V_{DD} (1.8 V)	Unit
IDDRUN	Run mode current	All peripherals ON	$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=1 MHz	2.88	mA
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=2 MHz	5.8	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=4 MHz	10.91	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=6 MHz	15.97	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=8 MHz	20.68	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=10 MHz	25.13	
		All peripherals OFF	$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=1 MHz	1.8	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=2 MHz	3.62	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=4 MHz	6.71	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=6 MHz	9.81	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=8 MHz	12.63	
			$f_{MSTR}=f_{OSC}=f_{PCLK}=f_{HCLK}$=10 MHz	15.47	

7.9 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

7.9.1 Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD}, V_{DDQ} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Table 27. EMS data

Symbol	Parameter	Conditions	Severity/ Criteria(1)	Unit
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 1.8 V, V_{DDQ} = 3.3 V, T_A = +25 °C, f_{OSC}/f_{CPUCLK} = 4 MHz/96 MHz PLL	1B	kV
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DDQ} pins to induce a functional disturbance	V_{DD}=1.8 V, V_{DDQ} = 3.3 V, T_A = +25 °C, f_{OSC}/f_{CPUCLK} = 4 MHz/96 MHz PLL conforms to IEC 1000-4-4	4A	

1. Data based on characterization results, not tested in production.

Mux write

Figure 20. Mux write diagram

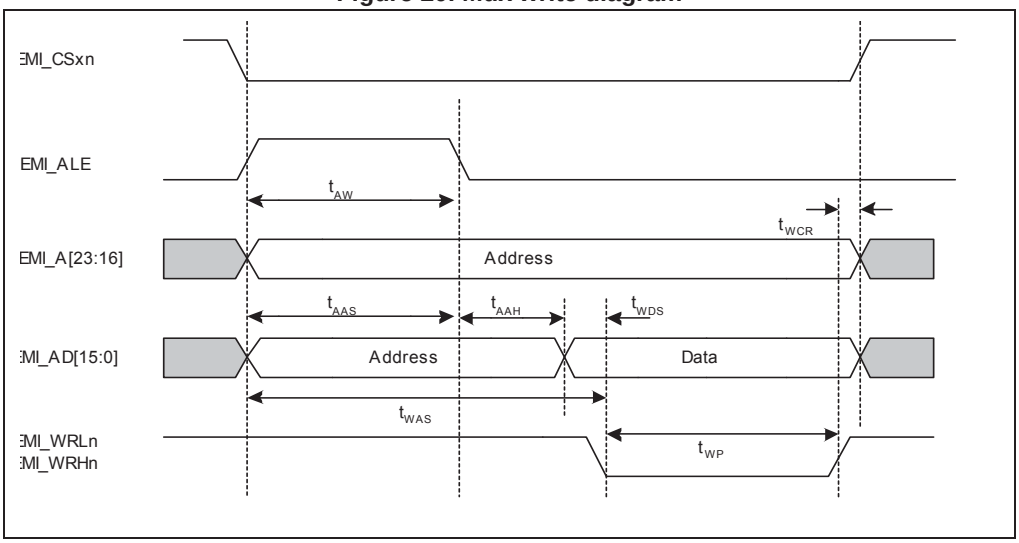


Table 35. Mux write times

Symbol	Parameter	Value	
		Min	Max
t_{WCR}	WRn to CSn inactive	(t_{BCLK}/2) - 2ns	(t_{BCLK}/2) + 2ns
t_{WAS}	Write address setup time	(WSTWEN + 1/2) x t_{BCLK} - 2.5 ns	(WSTWEN + 1/2) x t_{BCLK} + 2 ns
t_{WDS}	Write data setup time	((WSTWEN - ALE_LENGTH) x t_{BCLK}) - 2 ns	((WSTWEN - ALE_LENGTH) x t_{BCLK}) + 1 ns
t_{WP}	Write pulse width	((WSTWR-WSTWEN + 1) x t_{BCLK}) - 1 ns	((WSTWR-WSTWEN + 1) x $t_{BCLK)}$ + 1.5 ns
t_{AW}	ALE pulse width	(ALE_LENGTH x t_{BCLK})- 3.5 ns	(ALE_LENGTH x t_{BCLK})
t_{AAS}	Address to ALE setup time	(ALE_LENGTH x t_{BCLK})- 3.5 ns	(ALE_LENGTH x t_{BCLK})
t_{AAH}	Address to ALE hold time	(t_{BCLK}/2) - 1 ns	(t_{BCLK}/2) + 2 ns

7.12.4 I^2C electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 45. I^2C electrical characteristics

Symbol	Parameter	Standard I^2C		Fast I^2C		Unit
		Min	Max	Min	Max	
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		µs
$t_{HD:STA}$	Hold time START condition. After this period, the first clock pulse is generated(1)	4.0		0.6		µs
t_{LOW}	Low period of the SCL clock	4.7		1.3		µs
t_{HIGH}	High period of the SCL clock	4.0		0.6		µs
$t_{SU:STA}$	Setup time for a repeated START condition	4.7		0.6		µs
$t_{HD:DAT}$	Data hold time(2)	0		0		ns
$t_{SU:DAT}$	Data setup time	250		100		ns
t_R	Rise time of both SDA and SCL signals		1000	$20+0.1C_b$ (3)	300	ns
t_F	Fall time of both SDA and SCL signals		300	$20+0.1C_b$ (3)	300	ns
$t_{SU:STO}$	Setup time for STOP condition	4.0		0.6		µs
C_b	Capacitive load for each bus line		400		400	pF

1. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal
2. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. C_b = total capacitance of one bus line in pF

Figure 31. SPI slave timing diagram with CPHA = 1

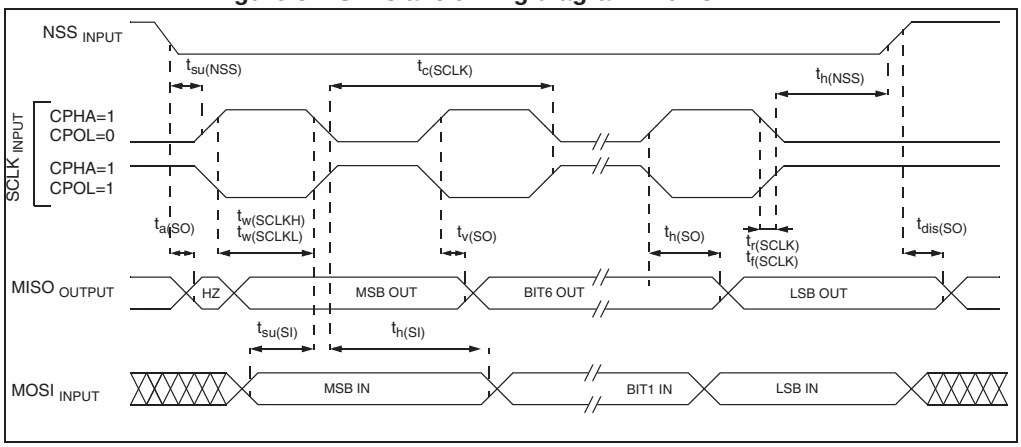


Figure 32. SPI master timing diagram

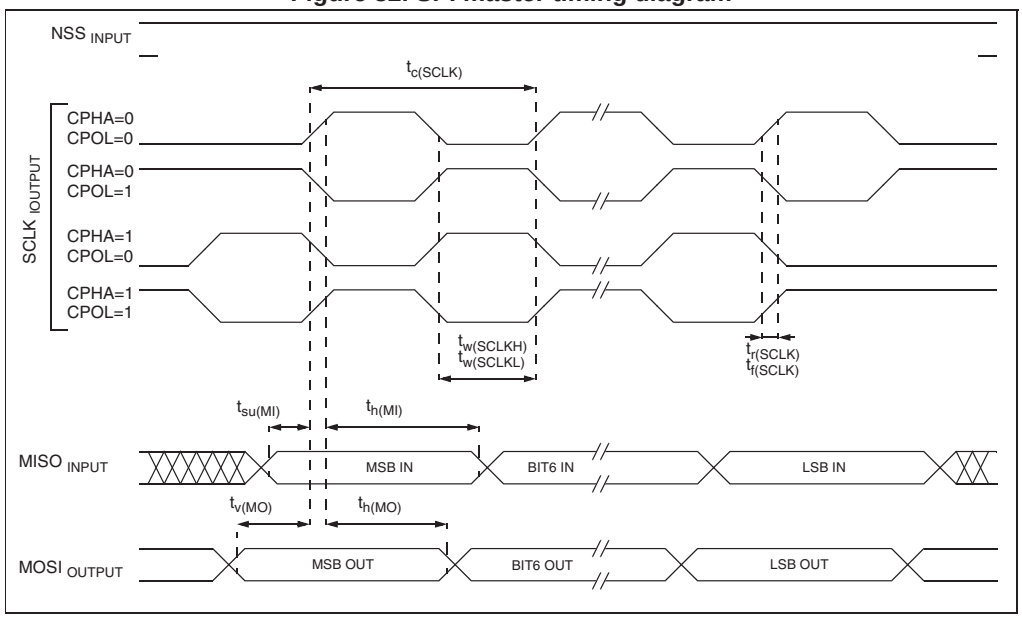


Table 48. ADC conversion time (silicon Rev G)

Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$2*16/f_{ADC}$		$3*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	1.33		2	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			500	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev G. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained on conversions started by trigger in single mode
4. All sucessive conversions in continuous and scan modes.

Table 49. ADC conversion time (silicon Rev H and higher)

Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$1*16/f_{ADC}$		$2*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	0.66		1.33	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			750	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps
$t_{CONV(FT)}$	Fast trigger mode conversion time(5)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(FT)	Fast trigger mode throughput rate(6)	f_{ADC} = 24 MHz	100		1200	ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev H and higher. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained from conversions started by trigger in single mode
4. All successive conversions in continuous and scan modes.
5. Conversion started by trigger when automatic clock gated mode enabled. Fast trigger mode is available only in devices with silicon Rev H and higher.
6. Value obtained from conversions started by fast trigger in single mode

8 Device marking

8.1 STR91xFAx32 / STR91xFAx42 / STR91xFAx44

Figure 34. Device marking for revision G LQFP80 and LQFP128 packages

Figure 35. Device marking for revision G LFBGA144 packages

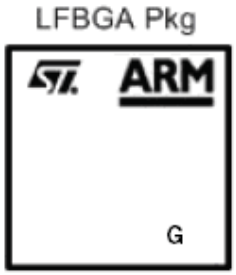


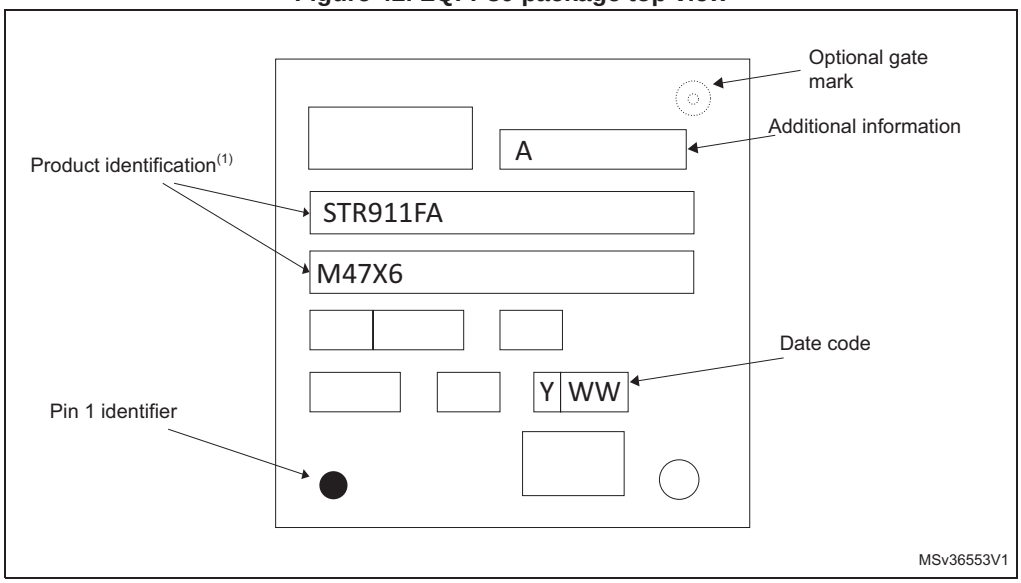
Figure 36. Device marking for revision H LQFP80 and LQFP128 packages

Figure 37. Device marking for revision H LFBGA144 packages

Marking of engineering samples for LQFP80

The following figure shows the engineering sample marking for the LQFP80 package. Only the information field containing the engineering sample marking is shown

Figure 42. LQFP80 package top view



1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 52.LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A[2]	-	-	1.700			0.0669
A1	0.210	-	-	0.0083		
A2	-	1.060	-		0.0417	
A3		0.026			0.0010	
A4	-	0.800	-	-	0.0315	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	8.800	-	-	0.3465	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	0.100			0.0039		
eee	0.150			0.0059		
fff	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.

9.1 ECOPACK

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions, and product status are available at *www.st.com*.

9.2 Thermal characteristics

The average chip-junction temperature, T_J must never exceed 125 °C.

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the power dissipation on input and output pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories. The worst case P_{INT} of the STR91xFA is 500 mW ($I_{DD} \times V_{DD}$, or 250 mA x 2.0 V).

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 53. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	***Thermal resistance junction-ambient*** LQFP 80 - 12 x 12 mm / 0.5 mm pitch	41.5	°C/W
Θ_{JA}	***Thermal resistance junction-ambient*** LQFP128 - 14 x 14 mm / 0.4 mm pitch	38	°C/W
Θ_{JA}	***Thermal resistance junction-ambient*** LFBGA 144 - 10 x 10 x 1.7 mm	36.5	°C/W

10 Ordering information

Table 54. Ordering information scheme

Example: STR9 1 2 F A W 4 4 X 6 T

Family

ARM9 microcontroller family

Series

1 = STR9 series 1

Feature set

0 = CAN, UART, IrDA, I2C, SSP
1 = USB, CAN, UART, IrDA, I2C, SSP
2 = USB, CAN, UART, IrDA, I2C, SSP, ETHERNET

Memory type

F = Flash

Revision at product level

A = Revison A

No. of pins

M = 80
W = 128
Z = 144

SRAM size

3 = 64 Kbytes
4 = 96 Kbytes

Primary memory size

2 = 256 Kbytes 6= 1024 Kbytes
4 = 512 Kbytes 7= 2048 Kbytes

Package

X = plastic LQFP
H = LFBGA

Temperature range

6 = -40 to 85 °C

Shipping option

T = Tape and reel packing

1. For a list of available options (e.g. speed, package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

11 Revision history

Table 55. Document revision history

Date	Revision	Changes
09-May-2007	1	Initial release
26-Nov-2007	2	Updated Standby current in *Table 15: Supply current characteristics on page 64* Added *Section 7.1: Parameter conditions on page 58* Added *Section 7.7.2: X1_CPU external clock source on page 67* Updated *Section 7.11: External memory bus timings on page 76* Added *Figure 14: LVD reset delay case 3 on page 63* Added *Table 48* and *Table 49* in ADC characteristics section Added min/max values for E, D, E1, D1 in *Figure 43 on page 98*
14-May-2008	3	Added 1MB and 2M devices, creating merged datasheet from seperate STR91xFAx32, 42, 44, 46 and 47 devices. Added STR912FAW32 to *Table 1: Device summary on page 1* Added paragraph on voltage supply shutdown in *Section 3.12 on page 24* Removed DMA feature for I2C in *Section 3.21 on page 33* Updated Sleep mode current in *Table 10: Current characteristics on page 60* Added *Table 16: Typical current consumption at 25 °C on page 65* Updated operating conditions for V_{DD} and f_{CPUCLK} in *Section 7.3 on page 61* and *Section 7.7: Clock and timing characteristics on page 66* Changed SPI master t_{SU} and $t_{H\ to}$ TBD in *Table 46: SPI electrical characteristics on page 88*
17-Jul-2008	4	Updated *Section 3.10.6: UART and SSP clock (BRCLK) on page 22* Updated *Table 11: Operating conditions on page 61* Updated $I_{SLEEP(IDDQ)}$ in *Table 15: Supply current characteristics on page 64* Updated *Table 17: Internal clock frequencies on page 66* Updated *Table 31: I/O characteristics on page 75*
22-Dec-2008	5	Updated *Section 7.7.3 on page 68*. Small text changes.