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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str912faw44x6

3.4.2 Branch cache (BC)

When instruction addresses are not sequential, such as a program branch situation, the PFQ would have to flush and reload which would cause the CPU to stall if no BC were present. Before reloading, the PFQ checks the BC to see if it contains the desired target branch address. The BC contains up to fifteen of the most recently taken branch addresses and the first eight instructions associated with each of these branches. This check is extremely fast, checking all fifteen BC entries simultaneously for a branch address match (cache hit). If there is a hit, the BC rapidly supplies the instruction and reduces the CPU stall. This gives the PFQ time to start pre-fetching again while the CPU consumes these eight instructions from the BC. The advantage here is that program loops (very common with embedded control applications) run very fast if the address of the loops are contained in the BC.

In addition, there is a 16th branch cache entry that is dedicated to the Vectored Interrupt Controller (VIC) to further reduce interrupt latency by eliminating the stall latency typically imposed by fetching the instruction that reads the interrupt vector address from the VIC.

3.4.3 Management of literals

Typical ARM architecture and compilers do not place literals (data constants) sequentially in Flash memory with the instructions that use them, but instead the literals are placed at some other address which looks like a program branch from the PFQ's point of view. The STR91xFA implementation of the ARM966E-S core has special circuitry to prevent flushing the PFQ when literals are encountered in program flow to keep performance at a maximum.

3.10.5 Flash memory interface clock (FMICLK)

The FMICLK clock is an internal clock derived from RCLK, defaulting to RCLK frequency at power up. The clock can be optionally divided by 2. The FMICLK determines the bus bandwidth between the ARM core and the Flash memory. Typically, codes in the Flash memory can be fetched one word per FMICLK clock in burst mode. The maximum FMICLK frequency is 96 MHz.

3.10.6 UART and SSP clock (BRCLK)

BRCLK is an internal clock derived from f_{MSTR} that is used to drive the two SSP peripherals and to generate the Baud rate for the three on-chip UART peripherals. The frequency can be optionally divided by 2.

3.10.7 External memory interface bus clock (BCLK)

The BCLK is an internal clock that controls the EMI bus. All EMI bus signals are synchronized to the BCLK. The BCLK is derived from the HCLK and the frequency can be configured to be the same or half that of the HCLK. Refer to *Table 17 on page 66* for the maximum BCLK frequency (f_{BCLK}). The BCLK clock is available on the LFBGA package as an output pin.

3.10.8 USB interface clock

Special consideration regarding the USB interface: The clock to the USB interface must operate at 48 MHz and comes from one of three sources, selected under firmware control:

- CCU master clock output of 48 MHz.
- CCU master clock output of 96 MHz. An optional divided-by-two circuit is available to produce 48 MHz for the USB while the CPU system runs at 96MHz.
- STR91xFA pin P2.7. An external 48 MHz oscillator connected to pin P2.7 can directly source the USB while the CCU master clock can run at some frequency other than 48 or 96 MHz.

3.10.9 Ethernet MAC clock

Special consideration regarding the Ethernet MAC: The external Ethernet PHY interface device requires it's own 25 MHz clock source. This clock can come from one of two sources:

- A 25 MHz clock signal coming from a dedicated output pin (P5.2) of the STR91xFA. In this case, the STR91xFA must use a 25 MHz signal on its main oscillator input in order to pass this 25 MHz clock back out to the PHY device through pin P5.2. The advantage here is that an inexpensive 25 MHz crystal may be used to source a clock to both the STR91xFA and the external PHY device.
- An external 25 MHz oscillator connected directly to the external PHY interface device. In this case, the STR91xFA can operate independent of 25 MHz.

3.10.10 External RTC calibration clock

The RTC_CLK can be enabled as an output on the JRTCK pin. The RTC_CLK is used for RTC oscillator calibration. The RTC_CLK is active in Sleep mode and can be used as a system wake up control clock.

3.10.11 Operation example

As an example of CCU operation, a 25 MHz crystal can be connected to the main oscillator input on pins X1_CPU and X2_CPU, a 32.768 kHz crystal connected to pins X1_RTC and X2_RTC, and the clock input of an external Ethernet PHY device is connected to STR91xFA output pin P5.2. In this case, the CCU can run the CPU at 96 MHz from PLL, the USB interface at 48 MHz, and the Ethernet interface at 25 MHz. The RTC is always running in the background at 32.768 kHz, and the CPU can go to very low power mode dynamically by running from 32.768 kHz and shutting off peripheral clocks and the PLL as needed.

3.11 Flexible power management

The STR91xFA offers configurable and flexible power management control that allows the user to choose the best power option to fit the application. Power consumption can be dynamically managed by firmware and hardware to match the system's requirements. Power management is provided via clock control to the CPU and individual peripherals.

Clocks to the CPU and peripherals can be individually divided and gated off as needed. In addition to individual clock divisors, the CCU master clock source going to the CPU, AHB, APB, EMI, and FMI can be divided dynamically by as much as 1024 for low power operation. Additionally, the CCU may switch its input to the 32.768 kHz RTC clock at any time for low power.

The STR91xFA supports the following three global power control modes:

- ***Run Mode*:** All clocks are on with option to gate individual clocks off via clock mask registers.
- ***Idle Mode*:** CPU and FMI clocks are off until an interrupt, reset, or wake-up occurs. Pre-configured clock mask registers selectively allow individual peripheral clocks to continue run during Idle Mode.
- ***Sleep Mode*:** All clocks off except RTC clock. Wake up unit remains powered, PLL is forced off.

A special mode is used when JTAG debug is active which never gates off any clocks even if the CPU enters Idle or Sleep mode.

3.11.1 Run mode

This is the default mode after any reset occurs. Firmware can gate off or scale any individual clock. Also available is a special Interrupt Mode which allows the CPU to automatically run full speed during an interrupt service and return back to the selected CPU clock divisor rate when the interrupt has been serviced. The advantage here is that the CPU can run at a very low frequency to conserve power until a periodic wake-up event or an asynchronous interrupt occurs at which time the CPU runs full speed immediately.

3.12.2 Battery supply

An optional stand-by voltage from a battery or other source may be connected to pin VBATT to retain the contents of SRAM in the event of a loss of the main digital supplies (V_{DD} and $V_{DDQ)}$. The SRAM will automatically switch its supply from the internal V_{DD} source to the VBATT pin when the voltage of V_{DD} drops below the LVD threshold. In order to use the battery supply, the LVD must be enabled.

The VBATT pin also supplies power to the RTC unit, allowing the RTC to function even when the main digital supplies (V_{DD} and V_{DDQ}) are switched off. By configuring the RTC register, it is possible to select whether or not to power from VBATT only the RTC unit, or power the RTC unit and the SRAM when the STR91xFA device is powered off.

3.13 System supervisor

The STR91xFA monitors several system and environmental inputs and will generate a global reset, a system reset, or an interrupt based on the nature of the input and configurable settings. A global reset clears all functions on the STR91xFA, a system reset will clear all but the Clock Control Unit (CCU) settings and the system status register. At any time, firmware may reset individual on-chip peripherals. System supervisor inputs include:

- GR: CPU voltage supply (V_{DD}) drop out or brown out
- GR: I/O voltage supply (V_{DDQ}) drop out or brown out
- GR: Power-Up condition
- SR: Watchdog timer timeout
- SR: External reset pin (RESET_INn)
- SR: JTAG debug reset command

Note: GR: means the input causes Global Reset, SR: means the input causes System Reset

The CPU may read a status register after a reset event to determine if the reset was caused by a watchdog timer timeout or a voltage supply drop out. This status register is cleared only by a power up reset.

3.13.1 Supply voltage brownout

Each operating voltage source (V_{DD} and V_{DDQ}) is monitored separately by the Low Voltage Detect (LVD) circuitry. The LVD will generate an early warning interrupt to the CPU when voltage sags on either V_{DD} or V_{DDQ} voltage inputs. This is an advantage for battery powered applications because the system can perform an orderly shutdown before the batteries become too weak. The voltage trip point to cause a brown out interrupt is typically 0.25V above the LVD dropout thresholds that cause a reset.

CPU firmware may prevent all brown-out interrupts by writing to interrupt mask registers at run-time.

3.20 UART interfaces with DMA

The STR91xFA supports three independent UART serial interfaces, designated UART0, UART1, and UART2. Each interface is very similar to the industry-standard 16C550 UART device. All three UART channels support IrDA encoding/decoding, requiring only an external LED transceiver to pins UARTx_RX and UARTx_Tx for communication. One UART channel (UART0) supports full modem control signals.

UART interfaces include the following features:

- Maximum baud rate of 1.5 Mbps
- Separate FIFOs for transmit and receive, each 16 deep, each FIFO can be disabled by firmware if desired
- Programmable FIFO trigger levels between 1/8 and 7/8
- Programmable baud rate generator based on CCU master clock, or CCU master clock divided by two
- Programmable serial data lengths of 5, 6, 7, or 8 bits with start bit and 1 or 2 stop bits
- Programmable selection of even, odd, or no-parity bit generation and detection
- False start-bit detection
- Line break generation and detection
- Support of IrDA SIR ENDEC functions for data rates of up to 115.2K bps
- IrDA bit duration selection of 3/16 or low-power (1.14 to 2.23 µsec)
- Channel UART0 supports modem control functions CTS, DCD, DSR, RTS, DTR, and RI

For your reference, only two standard 16550 UART features are not supported, 1.5 stop bits and independent receive clock.

3.20.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service channels UART0 and UART1 for fast and direct transfers between the UART bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive. Burst transfers require that UART FIFOs are enabled.

3.21 I^2C interfaces

The STR91xFA supports two independent I2C serial interfaces, designated I2C0, and I2C1. Each interface allows direct connection to an I2C bus as either a bus master or bus slave device (firmware configurable). I2C is a two-wire communication channel, having a bi-directional data signal and a single-directional clock signal based on open-drain line drivers, requiring external pull-up resistors.

Byte-wide data is transferred between a Master device and a Slave device on two wires. More than one bus Master is allowed, but only one Master may control the bus at any given time. Data is not lost when another Master requests the use of a busy bus because I2C supports collision detection and arbitration. More than one Slave device may be present on the bus, each having a unique address. The bus Master initiates all data movement and generates the clock that permits the transfer. Once a transfer is initiated by the Master, any device that is addressed is considered a Slave. Automatic clock synchronization allows I2C devices with different bit rates to communicate on the same physical bus.

A single device can play the role of Master or Slave, or a single device can be a Slave only. A Master or Slave device has the ability to suspend data transfers if the device needs more time to transmit or receive data.

Each I2C interface on the STR91xFA has the following features:

- Programmable clock supports various rates up to I2C Standard rate (100 KHz) or Fast rate (400 KHz).
- Serial I/O Engine (SIOE) takes care of serial/parallel conversion; bus arbitration; clock generation and synchronization; and handshaking
- Multi-master capability
- 7-bit or 10-bit addressing

3.22 SSP interfaces (SPI, SSI, and MICROWIRE) with DMA

The STR91xFA supports two independent Synchronous Serial Port (SSP) interfaces, designated SSP0, and SSP1. Primary use of each interface is for supporting the industry standard Serial Peripheral Interface (SPI) protocol, but also supporting the similar Synchronous Serial Interface (SSI) and MICROWIRE communication protocols.

SPI is a three or four wire synchronous serial communication channel, capable of full-duplex operation. In three-wire configuration, there is a clock signal, and two data signals (one data signal from Master to Slave, the other from Slave to Master). In four-wire configuration, an additional Slave Select signal is output from Master and received by Slave.

The SPI clock signal is a gated clock generated from the Master and regulates the flow of data bits. The Master may transmit at a variety of baud rates, up to 24 MHz

In multi-Slave operation, no more than one Slave device can transmit data at any given time. Slave selection is accomplished when a Slave's "Slave Select" input is permanently grounded or asserted active-low by a Master device. Slave devices that are not selected do not interfere with SPI activities. Slave devices ignore the clock signals and keep their data output pins in high-impedance state when not selected. The STR91xFA supports SPI multi-Master operation because it provides collision detection.

Each SSP interface on the STR91xFA has the following features:

- Full-duplex, three or four-wire synchronous transfers
- Master or Slave operation
- Programmable clock bit rate with prescaler, up to 24 MHz for Master mode and 4 MHz for Slave mode
- Separate transmit and receive FIFOs, each 16-bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Programmable clock and phase polarity
- Specifically for MICROWIRE protocol:
  - Half-duplex transfers using 8-bit control message
- Specifically for SSI protocol:
  - Full-duplex four-wire synchronous transfer
  - Transmit data pin tri-stateable when not transmitting

3.22.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service each SSP channel for fast and direct transfers between the SSP bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive. Burst transfers require that FIFOs are enabled.

3.23 General purpose I/O

There are up to 80 GPIO pins available on 10 I/O ports for 128-pin and 144-ball devices, and up to 40 GPIO pins on 5 I/O ports for 80-pin devices. Each and every GPIO pin by default (during and just after a reset condition) is in high-impedance input mode, and some GPIO pins are additionally routed to certain peripheral function inputs. CPU firmware may initialize GPIO pins to have alternate input or output functions as listed in *Table 8*. At any time, the logic state of any GPIO pin may be read by firmware as a GPIO input, regardless of its reassigned input or output function.

Bit masking is available on each port, meaning firmware may selectively read or write individual port pins, without disturbing other pins on the same port during a write.

Firmware may designate each GPIO pin to have open-drain or push-pull characteristics.

All GPIO pins are 5 V tolerant, meaning they can drive a voltage level up to VDDQ, and can be safely driven by a voltage up to 5 V.

3.24 A/D converter (ADC) with DMA

The STR91xFA provides an eight-channel, 10-bit successive approximation analog-to-digital converter. The ADC input pins are multiplexed with other functions on Port 4 as shown in *Table 8*. Following are the major ADC features:

- Fast conversion time, as low as 0.7 usec
- Accuracy. Integral and differential non-linearity are typically within 4 conversion counts.
- 0 to 3.6 V input range. External reference voltage input pin (AVREF) available on 128-pin packages for better accuracy on low-voltage inputs. See *Table 11: Operating conditions*, for restrictions to the relative voltage levels of VDDQ, AVDD, AVREF, and AVREF_AVDD.
- CPU Firmware may convert one ADC input channel at a time, or it has the option to set the ADC to automatically scan and convert all eight ADC input channels sequentially before signalling an end-of-conversion
- Automatic continuous conversion mode is available for any number of designated ADC input channels
- Analog watchdog mode provides automatic monitoring of any ADC input, comparing it against two programmable voltage threshold values. The ADC unit will set a flag or it will interrupt the CPU if the input voltage rises above the higher threshold, or drops below the lower threshold.
- The ADC unit goes to stand-by mode (very low-current consumption) after any reset event. CPU firmware may also command the ADC unit to stand-by mode at any time.
- ADC conversion can be started or triggered by software command as well as triggers from Timer/Counter (TIM), Motor Controller and input from external pin.

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	21	G4	EMI_ BWR_ WRLn	O	EMI byte write strobe (8 bit mode) or low byte write strobe (16 bit mode) Can also be configured as EMI_LBn in BGA package	N/A				
-	22	H1	EMI_ WRHn	O	EMI high byte write strobe (16-bit mode) Can also be configured as EMI_UBn in BGA package	N/A				
-	74	J10	EMI_ALE	O	EMI address latch enable (mux mode)	N/A				
-	75	J9	EMI_ RDn	O	EMI read strobe	N/A				
-	-	H8	EMI_ BAAn	O	EMI Burst address advance	N/A				
-	-	K8	EMI_ WAITn	I	EMI Wait input for burst mode device	N/A				
-	-	M8	EMI_ BCLK	O	EMI bus clock	N/A				
-	-	A12	EMI_ WEn	O	EMI write enable	N/A				
-	91	E10	TAMPER _IN	I	Tamper detection input	N/A				
-	94	D11	MII_ MDIO	I/O	MAC/PHY management data line	N/A				
59	95	D10	USBDN	I/O	USB data (-) bus connect	N/A				
60	96	C11	USBDP	I/O	USB data (+) bus connect	N/A				
56	89	C12	RESET _INn	I	External reset input	N/A				
62	100	A9	RESET _OUTn	O	Global or System reset output	N/A				
65	104	A10	X1_CPU	I	CPU oscillator or crystal input	N/A				
64	103	A11	X2_CPU	O	CPU crystal connection	N/A				

6 Memory mapping

The ARM966E-S CPU addresses a single linear address space of 4 giga-bytes (2^{32}) from address 0x0000.0000 to 0xFFFF.FFFF as shown in *Figure 9*. Upon reset the CPU boots from address 0x0000.0000, which is chip-select zero at address zero in the Flash Memory Interface (FMI).

The Instruction TCM and Data TCM enable high-speed CPU operation without incurring any performance or power penalties associated with accessing the system buses (AHB and APB). I-TCM and D-TCM address ranges are shown at the bottom of the memory map in *Figure 9*.

6.1 Buffered and non-buffered writes

The CPU makes use of write buffers on the AHB and the D-TCM to decouple the CPU from any wait states associated with a write operation. The user may choose to use write with buffers on the AHB by setting bit 3 in control register CP15 and selecting the appropriate AHB address range when writing. By default at reset, buffered writes are disabled (bit 3 of CP15 is clear) and all AHB writes are non-buffered until enabled. *Figure 9* shows that most addressable items on the AHB are aliased at two address ranges, one for buffered writes and another for non-buffered writes. A buffered write will allow the CPU to continue program execution while the write-back is performed through a FIFO to the final destination on the AHB. If the FIFO is full, the CPU is stalled until FIFO space is available. A non-buffered write will impose an immediate delay to the CPU, but results in a direct write to the final AHB destination, ensuring data coherency. Read operations from AHB locations are always direct and never buffered.

6.2 System (AHB) and peripheral (APB) buses

The CPU will access SRAM, higher-speed peripherals (USB, Ethernet, Programmable DMA), and the external bus (EMI) on the AHB at their respective base addresses indicated in *Figure 9*. Lower-speed peripherals reside on the APB and are accessed using two separate AHB-to-APB bridge units (APB0 and APB1). These bridge units are essentially address windows connecting the AHB to the APB. To access an individual APB peripheral, the CPU will place an address on the AHB bus equal to the base address of the appropriate bridge unit APB0 or APB1, plus the offset of the particular peripheral, plus the offset of the individual data location within the peripheral. *Figure 9* shows the base addresses of bridge units APB0 and APB1, and also the base address of each APB peripheral. Please consult the STR91xFA Reference manual for the address of data locations within each individual peripheral.

6.3 SRAM

The SRAM is aliased at three separate address ranges as shown in *Figure 9*. When the CPU accesses SRAM starting at 0x0400.0000, the SRAM appears on the D-TCM. When CPU access starts at 0x4000.0000, SRAM appears in the buffered AHB range. Beginning at CPU address 0x5000.0000, SRAM is in non-buffered AHB range. The SRAM size must be specified by CPU intitialization firmware writing to a control register after any reset condition. Default SRAM size is 32K bytes, with option to set to 64K bytes on STR91xFAx3x devices, and to 96K bytes on STR91xFAx4x devices.

When other AHB bus masters (such as a DMA controller) write to SRAM, their access is never buffered. Only the CPU can make use of buffered AHB writes.

6.4 Two independent Flash memories

The STR91xFA has two independent Flash memories, the larger primary Flash and the small secondary Flash. It is possible for the CPU to erase/write to one of these Flash memories while simultaneously reading from the other.

One or the other of these two Flash memories may reside at the “boot” address position of 0x0000.0000 at power-up or at reset as shown in *Figure 9*. The default configuration is that the first sector of primary Flash memory is enabled and residing at the boot position, and the secondary Flash memory is disabled. This default condition may be optionally changed as described below.

6.4.1 Default configuration

When the primary Flash resides at boot position, typical CPU initialization firmware would set the start address and size of the main Flash memory, and go on to enable the secondary Flash, define it’s start address and size. Most commonly, firmware would place the secondary Flash start address at the location just after the end of the primary Flash memory. In this case, the primary Flash is used for code storage, and the smaller secondary Flash can be used for data storage (EEPROM emulation).

6.4.2 Optional configuration

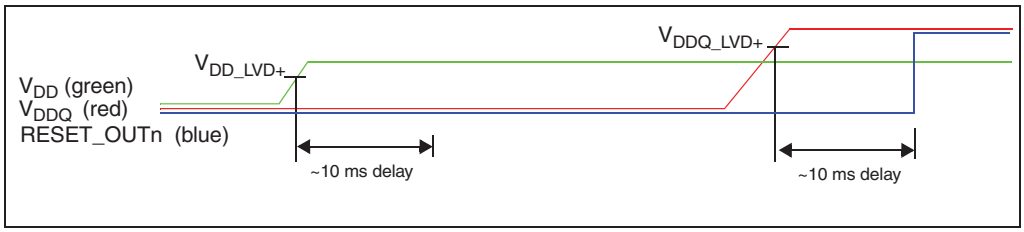
Using the STR91xFA device configuration software tool, or IDE from 3rd party, one can specify that the smaller secondary Flash memory is at the boot location at reset and the primary Flash is disabled. The selection of which Flash memory is at the boot location is programmed in a non-volatile Flash-based configuration bit during JTAG ISP. The boot selection choice will remain as the default until the bit is erased and re-written by the JTAG interface. The CPU cannot change this choice for boot Flash, only the JTAG interface has access.

In this case where the secondary Flash defaults to the boot location upon reset, CPU firmware would typically initialize the Flash memories the following way. The secondary Flash start address and size is specified, then the primary Flash is enabled and its start address and size is specified. The primary Flash start address would typically be located just after the final address location of the secondary Flash. This configuration is particularly well-suited for In-Application-Programming (IAP). The CPU would boot from the secondary Flash memory, initialize the system, then check the contents of the primary Flash memory (by checksum or other means). If the contents of primary Flash is OK, then CPU execution continues from either Flash memory.

7.5.1 LVD delay timing

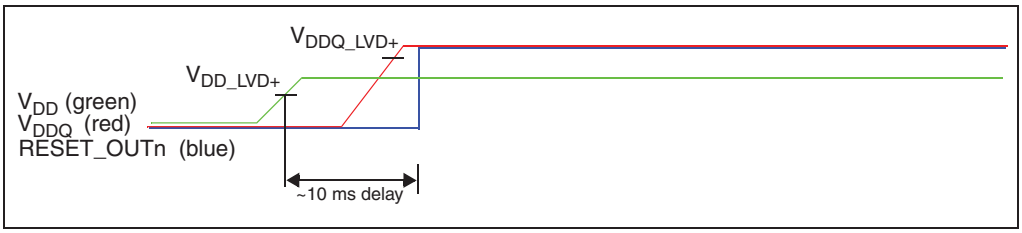
Case 1: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **after** the first ~10 ms delay (introduced by the VDD rising edge), a new ~10 ms delay starts before the release of RESET_OUTn. See *Figure 12.*

Figure 12. LVD reset delay case 1



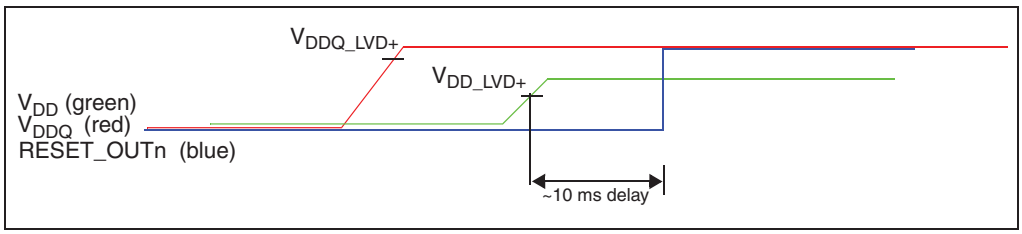
Case 2: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **before** the first ~10 ms delay (introduced by the VDD rising edge), RESET_OUTn will be released immediately at the end of the delay. No new delay is introduced in this case. See *Figure 13.*

Figure 13. LVD reset delay case 2



Case 3: When V_{DD} reaches the V_{DD_LVD+} threshold **after** the V_{DDQ} rising edge, RESET_OUTn will be released at the end of a ~10 ms delay. See *Figure 14*

Figure 14. LVD reset delay case 3



7.9.2 Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 28. EMI data

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}/f_{CPUCLK}]		Unit
				24 MHz / 48 MHz(1)	24 MHz / 96 MHz(1)	
S_{EMI}	Peak level	V_{DDQ} = 3.3 V, V_{DD}=1.8 V, T_A=+25 °C, LQFP128 package(2) conforming to SAE J 1752/3	0.1 MHz to 30 MHz	14	10	dBµV
			30 MHz to 130 MHz	18	19	
			130 MHz to 1GHz	18	22	
			SAE EMI Level	4	4	-

1. Data based on characterization results, not tested in production.
2. BGA and LQFP devices have similar EMI characteristics.

7.9.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

7.9.4 Electro-static discharge (ESD)

Electro-Static Discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 29. ESD data

Symbol	Ratings	Conditions	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A = +25°C conforming to JESD22-A114	2	+/-2000	V
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charged Device Model)	T_A = +25°C conforming to JESD22-C101	II	1000	

1. Data based on characterization results, not tested in production.

Non-mux read

Figure 19. Non-mux bus read timings

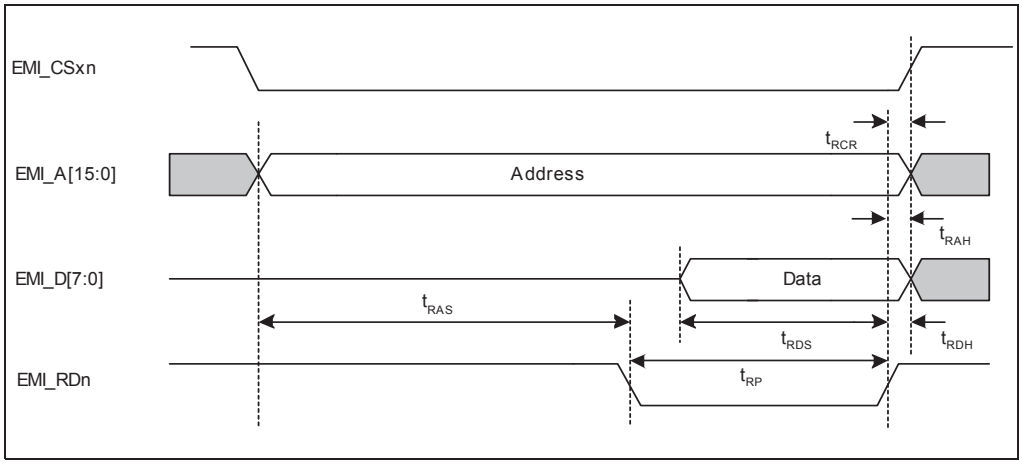


Table 34. EMI read operation

Symbol	Parameter	Value	
		Min	Max
t_{RCR}	Read to CSn inactive	0	1.5 ns
t_{RAS}	Read address setup time	((WSTOEN) x t_{BCLK})- 1.5 ns	(WSTOEN) x t_{BCLK}
t_{RDS}	Read data setup time	12.5	-
t_{RDH}	Read data hold time	0	-
t_{RP}	Read pulse width	((WSTRD-WSTOEN+1) x t_{BCLK})- 0.5 ns	((WSTRD-WSTOEN+1) x t_{BCLK})+ 2 ns

Ethernet MII management timings

Figure 27. Ethernet MII management timing diagram

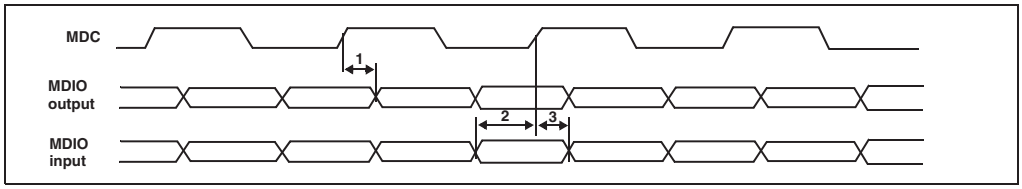
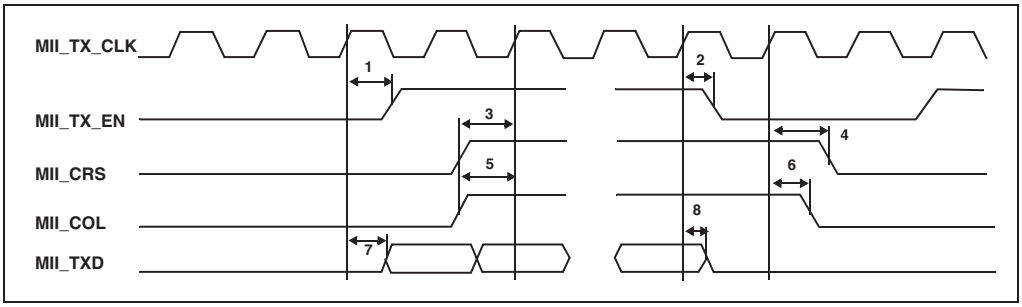


Table 42. Ethernet MII management timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	MDIO delay from rising edge of MDC	t_c(MDIO)		2.83	ns
2	MDIO setup time to rising edge of MDC	T_{su} (MDIO)	2.70		ns
3	MDIO hold time from rising edge of MDC	T_h (MDIO)	-2.03		ns

Ethernet MII transmit timings

Figure 28. Ethernet MII transmit timing diagram



8.2 STR91xFAx46 / STR91xFAx47

Figure 38. Device marking for revision A LQFP80 and LQFP128 packages

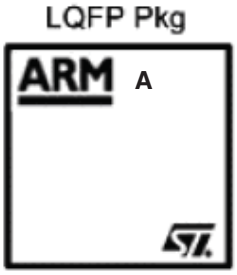
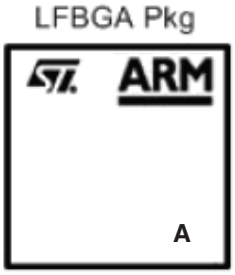
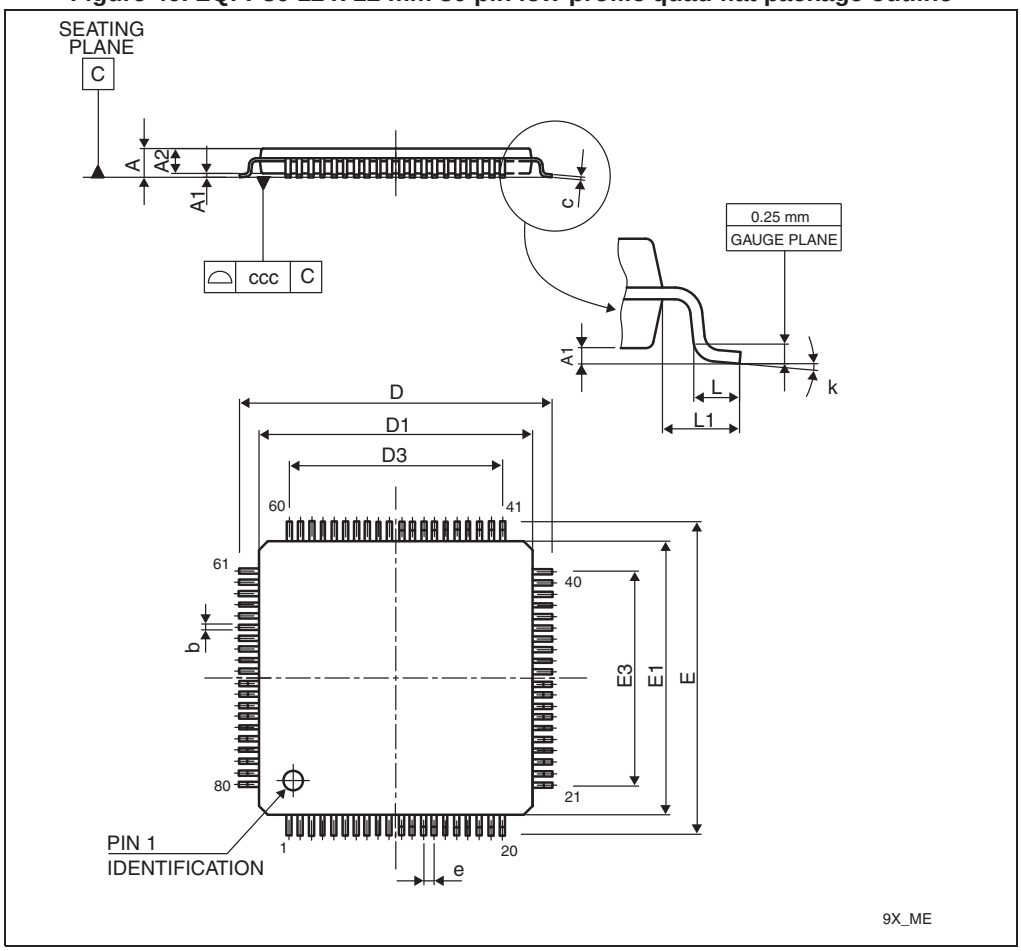


Figure 39. Device marking for revision A LFBGA144 packages



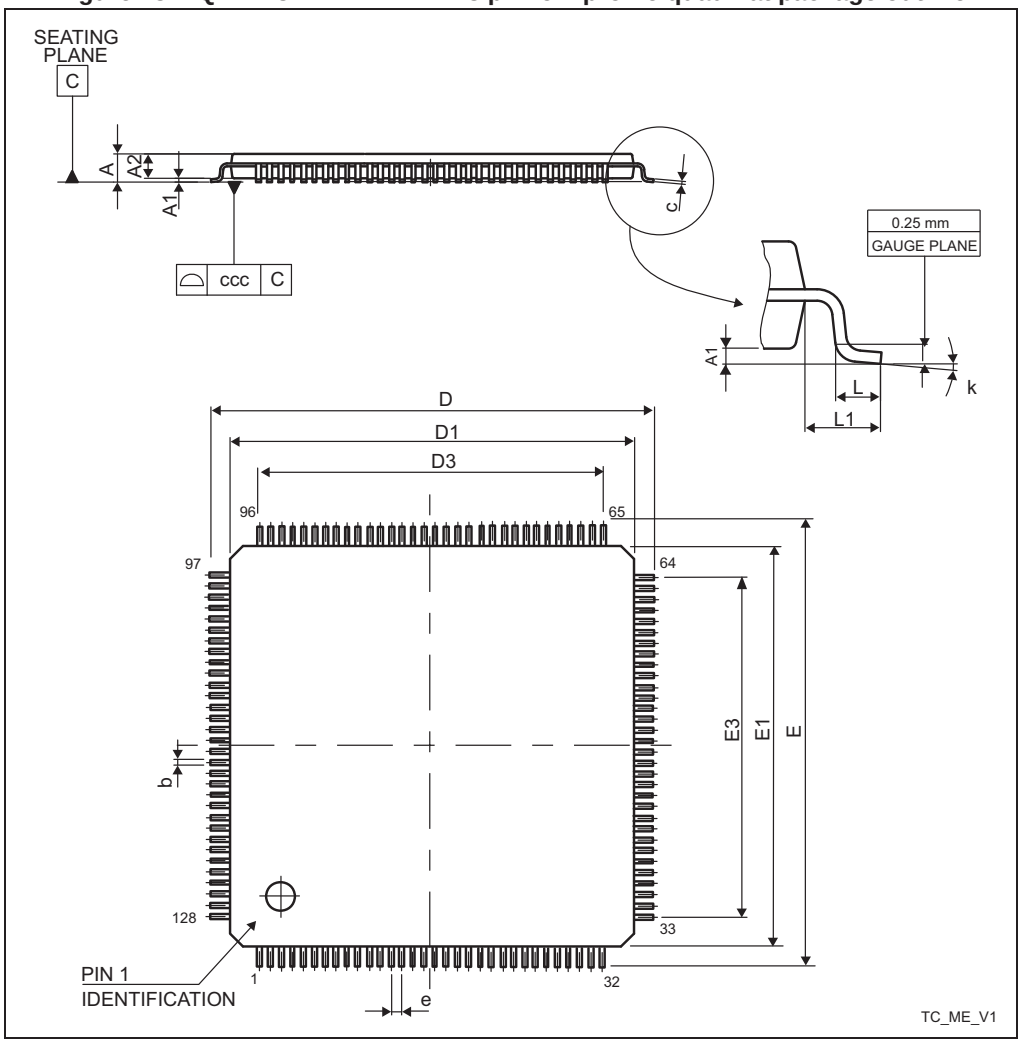
9 Package mechanical data

Figure 40. LQFP80 12 x 12 mm 80 pin low-profile quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Figure 43. LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 55. Document revision history

Date	Revision	Changes
02-Jul-2009	6	*Section 3.13.7: Tamper detection*: Removed information about “Normally Closed/Tamper Open mode”. *Table 31: I/O characteristics*: Updated V_{HYS} row.
3-Mar-2015	7	Updated *Figure 40: LQFP80 12 x 12 mm 80 pin low-profile quad flat package outline on page 95*, *Figure 43: LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline on page 98* and *Figure 45: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline on page 101* Updated *Table 50: LQFP80 12 x12 mm low-profile quad flat package mechanical data on page 96*, *Table 51: LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package mechanical data on page 99*, and *Table 52: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data on page 102* Added *Figure 42: LQFP80 package top view on page 97*, *Figure 43: LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline on page 98*, *Figure 44: LQFP128 package top view on page 100* and *Figure 45: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline on page 101*