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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str912faw47x6t

Table 4. Sectoring of secondary Flash memory

Size of secondary Flash	32 Kbytes	128 Kbytes
Number of sectors	4	8
Size of each sector	8 Kbytes	16 Kbytes

3.8 One-time-programmable (OTP) memory

There are 32 bytes of OTP memory ideally suited for serial numbers, security keys, factory calibration constants, or other permanent data constants. These OTP data bytes can be programmed only one time through either the JTAG interface or by the CPU, and these bytes can never be altered afterwards. As an option, a “lock bit” can be set by the JTAG interface or the CPU which will block any further writing to the this OTP area. The “lock bit” itself is also OTP. If the OTP array is unlocked, it is always possible to go back and write to an OTP byte location that has not been previously written, but it is never possible to change an OTP byte location if any one bit of that particular byte has been written before. The last two OTP bytes (bytes 31 and 30) are reserved for the STR91xFA product ID and revision level.

3.8.1 Product ID and revision level

OTP bytes 31 and 30 are programmed at ST factory before shipment and may be read by firmware to determine the STR91xFA product type and silicon revision so it can optionally take action based on the silicon on which it is running. In Rev H devices and 1MB/2MB Rev A devices, byte 31 contains the major family identifier of "9" (for STR9) in the high-nibble location and the minor family identifier in the low nibble location, which can be used to determine the size of primary flash memory. In all devices, byte 30 contains the silicon revision level indicator. See *Table 5* for values related to the revisions of STR9 production devices and size of primary Flash memory. See *Section 8* for details of external identification of silicon revisions.

Table 5. Product ID and revision level values

Production salestype	Silicon revision	Size of primary Flash	OTP byte 31	OTP byte 30
STR91xFAxxxxx	Rev G	256K or 512K	91h	20h
STR91xFAxxxxx	Rev H	256K	90h	21h
STR91xFAxxxxx	Rev H	512K	91h	21h
STR91xFAx46xx	Rev A	1024K	92h	21h
STR91xFAx47xx	Rev A	2048K	93h	21h

3.9 Vectored interrupt controller (VIC)

Interrupt management in the STR91xFA is implemented from daisy-chaining two standard ARM VIC units. This combined VIC has 32 prioritized interrupt request channels and generates two interrupt output signals to the CPU. The output signals are FIQ and IRQ, with FIQ having higher priority.

3.9.1 FIQ handling

FIQ (Fast Interrupt reQuest) is the only non-vectored interrupt and the CPU can execute an Interrupt Service Routine (ISR) directly without having to determine/prioritize the interrupt source, minimizing ISR latency. Typically only one interrupt source is assigned to FIQ. An FIQ interrupt has its own set of banked registers to minimize the time to make a context switch. Any of the 32 interrupt request input signals coming into the VIC can be assigned to FIQ.

3.9.2 IRQ handling

IRQ is a vectored interrupt and is the logical OR of all 32 interrupt request signals coming into the 32 IRQ channels. Priority of individual vectored interrupt requests is determined by hardware (IRQ channel Intr 0 is highest priority, IRQ channel Intr 31 is lowest).

However, inside the same VIC (primary or secondary VIC), CPU firmware may re-assign individual interrupt sources to individual hardware IRQ channels, meaning that firmware can effectively change interrupt priority levels as needed within the same VIC (from priority 0 to priority 16).

Note: VIC0 (primary VIC) interrupts always have higher priority than VIC1 (secondary VIC) interrupts

When the IRQ signal is activated by an interrupt request, VIC hardware will resolve the IRQ interrupt priority, then the ISR reads the VIC to determine both the interrupt source and the vector address to jump to the service code.

The STR91xFA has a feature to reduce ISR response time for IRQ interrupts. Typically, it requires two memory accesses to read the interrupt vector address from the VIC, but the STR91xFA reduces this to a single access by adding a 16th entry in the instruction branch cache, dedicated for interrupts. This 16th cache entry always holds the instruction that reads the interrupt vector address from the VIC, eliminating one of the memory accesses typically required in traditional ARM implementations.

3.9.3 Interrupt sources

The 32 interrupt request signals coming into the VIC on 32 IRQ channels are from various sources; 5 from a wake-up unit and the remaining 27 come from internal sources on the STR91xFA such as on-chip peripherals, see *Table 6*. Optionally, firmware may force an interrupt on any IRQ channel.

One of the 5 interrupt requests generated by the wake-up unit (IRQ25 in *Table 6*) is derived from the logical OR of all 32 inputs to the wake-up unit. Any of these 32 inputs may be used to wake up the CPU and cause an interrupt. These 32 inputs consist of 30 external interrupts on selected and enabled GPIO pins, plus the RTC interrupt, and the USB Resume interrupt.

Each of 4 remaining interrupt requests generated by the wake-up unit (IRQ26 in *Table 6*) are derived from groupings of 8 interrupt sources. One group is from GPIO pins P3.2 to P3.7 plus the RTC interrupt and the USB Resume interrupt; the next group is from pins P5.0 to P5.7; the next group is from pins P6.0 to P6.7; and last the group is from pins P7.0 to P7.7. This allows individual pins to be assigned directly to vectored IRQ interrupts or one pin assigned directly to the non-vectored FIQ interrupt.

Table 6. VIC IRQ channels

IRQ channel hardware priority	VIC input channel	Logic block	Interrupt source
0 (high priority)	VIC0.0	Watchdog	Timeout in WDT mode, Terminal Count in Counter Mode
1	VIC0.1	CPU Firmware	Firmware generated interrupt
2	VIC0.2	CPU Core	Debug Receive Command
3	VIC0.3	CPU Core	Debug Transmit Command
4	VIC0.4	TIM Timer 0	Logic OR of ICI0_0, ICI0_1, OCI0_0, OCI0_1, Timer overflow
5	VIC0.5	TIM Timer 1	Logic OR of ICI1_0, ICI1_1, OCI1_0, OCI1_1, Timer overflow
6	VIC0.6	TIM Timer 2	Logic OR of ICI2_0, ICI2_1, OCI2_0, OCI2_1, Timer overflow
7	VIC0.7	TIM Timer 3	Logic OR of ICI3_0, ICI3_1, OCI3_0, OCI3_1, Timer overflow
8	VIC0.8	USB	Logic OR of high priority USB interrupts
9	VIC0.9	USB	Logic OR of low priority USB interrupts
10	VIC0.10	CCU	Logic OR of all interrupts from Clock Control Unit
11	VIC0.11	Ethernet MAC	Logic OR of Ethernet MAC interrupts via its own dedicated DMA channel.
12	VIC0.12	DMA	Logic OR of interrupts from each of the 8 individual DMA channels
13	VIC0.13	CAN	Logic OR of all CAN interface interrupt sources
14	VIC0.14	IMC	Logic OR of 8 Induction Motor Control Unit interrupts
15	VIC0.15	ADC	End of AtoD conversion interrupt
16	VIC1.0	UART0	Logic OR of 5 interrupts from UART channel 0
17	VIC1.1	UART1	Logic OR of 5 interrupts from UART channel 1
18	VIC1.2	UART2	Logic OR of 5 interrupts from UART channel 2
19	VIC1.3	I2C0	Logic OR of transmit, receive, and error interrupts of I2C channel 0
20	VIC1.4	I2C1	Logic OR of transmit, receive, and error interrupts of I2C channel 1
21	VIC1.5	SSP0	Logic OR of all interrupts from SSP channel 0
22	VIC1.6	SSP1	Logic OR of all interrupts from SSP channel 1
23	VIC1.7	BROWNOUT	LVD warning interrupt
24	VIC1.8	RTC	Logic OR of Alarm, Tamper, or Periodic Timer interrupts

3.10.11 Operation example

As an example of CCU operation, a 25 MHz crystal can be connected to the main oscillator input on pins X1_CPU and X2_CPU, a 32.768 kHz crystal connected to pins X1_RTC and X2_RTC, and the clock input of an external Ethernet PHY device is connected to STR91xFA output pin P5.2. In this case, the CCU can run the CPU at 96 MHz from PLL, the USB interface at 48 MHz, and the Ethernet interface at 25 MHz. The RTC is always running in the background at 32.768 kHz, and the CPU can go to very low power mode dynamically by running from 32.768 kHz and shutting off peripheral clocks and the PLL as needed.

3.11 Flexible power management

The STR91xFA offers configurable and flexible power management control that allows the user to choose the best power option to fit the application. Power consumption can be dynamically managed by firmware and hardware to match the system's requirements. Power management is provided via clock control to the CPU and individual peripherals.

Clocks to the CPU and peripherals can be individually divided and gated off as needed. In addition to individual clock divisors, the CCU master clock source going to the CPU, AHB, APB, EMI, and FMI can be divided dynamically by as much as 1024 for low power operation. Additionally, the CCU may switch its input to the 32.768 kHz RTC clock at any time for low power.

The STR91xFA supports the following three global power control modes:

- ***Run Mode*:** All clocks are on with option to gate individual clocks off via clock mask registers.
- ***Idle Mode*:** CPU and FMI clocks are off until an interrupt, reset, or wake-up occurs. Pre-configured clock mask registers selectively allow individual peripheral clocks to continue run during Idle Mode.
- ***Sleep Mode*:** All clocks off except RTC clock. Wake up unit remains powered, PLL is forced off.

A special mode is used when JTAG debug is active which never gates off any clocks even if the CPU enters Idle or Sleep mode.

3.11.1 Run mode

This is the default mode after any reset occurs. Firmware can gate off or scale any individual clock. Also available is a special Interrupt Mode which allows the CPU to automatically run full speed during an interrupt service and return back to the selected CPU clock divisor rate when the interrupt has been serviced. The advantage here is that the CPU can run at a very low frequency to conserve power until a periodic wake-up event or an asynchronous interrupt occurs at which time the CPU runs full speed immediately.

3.11.2 Idle mode

In this mode the CPU suspends code execution and the CPU and FMI clocks are turned off immediately after firmware sets the Idle Bit. Various peripherals continue to run based on the settings of the mask registers that exist just prior to entering Idle Mode. There are 3 ways to exit Idle Mode and return to Run Mode:

- Any reset (external reset pin, watchdog, low-voltage, power-up, JTAG debug command)
- Any interrupt (external, internal peripheral, RTC alarm or interval)
- Input from wake-up unit on GPIO pins

Note: It is possible to remain in Idle Mode for the majority of the time and the RTC can be programmed to periodically wake up to perform a brief task or check status.

3.11.3 Sleep mode

In this mode all clock circuits except the RTC are turned off and main oscillator input pins X1_CPU and X2_CPU are disabled. The RTC clock is required for the CPU to exit Sleep Mode. The entire chip is quiescent (except for RTC and wake-up circuitry). There are three means to exit Sleep Mode and re-start the system:

- Some resets (external reset pin, low-voltage, power-up, JTAG debug command)
- RTC alarm
- Input from wake-up unit

3.12 Voltage supplies

The STR91xFA requires two separate operating voltage supplies. The CPU and memories operate from a 1.65V to 2.0V on the VDD pins, and the I/O ring operates at 2.7V to 3.6V on the VDDQ pins.

In Standby mode, both VDD and VDDQ must be shut down. Otherwise the specified maximum power consumption for Standby mode (I_{RTC_STBY} and I_{SRAM_STBY}) may be exceeded. Leakage may occur if only one of the voltage supplies is off.

3.12.1 Independent A/D converter supply and reference voltage

The ADC unit on 128-pin and 144-ball packages has an isolated analog voltage supply input at pin AVDD to accept a very clean voltage source, independent of the digital voltage supplies. Additionally, an isolated analog supply ground connection is provided on pin AVSS only on 128-pin and 144-ball packages for further ADC supply isolation. On 80-pin packages, the analog voltage supply is shared with the ADC reference voltage pin (as described next), and the analog ground is shared with the digital ground at a single point in the STR91xFA device on pin AVSS_VSSQ.

A separate external analog reference voltage input for the ADC unit is available on 128-pin and 144-ball packages at the AVREF pin for better accuracy on low voltage inputs. For 80-pin packages, the ADC reference voltage is tied internally to the ADC unit supply voltage at pin AVREF_AVDD, meaning the ADC reference voltage is fixed to the ADC unit supply voltage.

See *Table 11: Operating conditions*, for restrictions to the relative voltage levels of VDDQ, AVDD, AVREF, and AVREF_AVDD.

3.13.7 Tamper detection

On 128-pin and 144-ball STR91xFA devices only, there is a tamper detect input pin, TAMPER_IN, used to detect and record the time of a tamper event on the end product such as malicious opening of an enclosure, unwanted opening of a panel, etc. The activation mode of the tamper pin detects when a signal on the tamper input pin is driven from low-to-high, or high-to-low depending on firmware configuration. Once a tamper event occurs, the RTC time (millisecond resolution) and the date are recorded in the RTC unit. Simultaneously, the SRAM standby voltage source will be cut off to invalidate all SRAM contents. Tamper detection control and status logic are part of the RTC unit.

3.14 Real-time clock (RTC)

The RTC combines the functions of a complete time-of-day clock (millisecond resolution) with an alarm programmable up to one month, a 9999-year calender with leap-year support, periodic interrupt generation from 1 to 512 Hz, tamper detection (described in *Section 3.13.7*), and an optional clock calibration output on the JRTCK pin. The time is in 24 hour mode, and time/calendar values are stored in binary-coded decimal format.

The RTC also provides a self-isolation mode that is automatically activated during power down. This feature allows the RTC to continue operation when V_{DDQ} and V_{DD} are absent, as long as an alternate power source, such as a battery, is connected to the VBATT input pin. The current drawn by the RTC unit on the VBATT pin is very low in this standby mode, I_{RTC_STBY}.

3.15 JTAG interface

An IEEE-1149.1 JTAG interface on the STR91xFA provides In-System-Programming (ISP) of all memory, boundary scan testing of pins, and the capability to debug the CPU.

STR91xFA devices are shipped from ST with blank Flash memories. The CPU can only boot from Flash memory (selection of which Flash bank is programmable). Firmware must be initially programmed through JTAG into one of these Flash memories before the STR91xFA is used.

Six pins are used on this JTAG serial interface. The five signals JTDI, JTDO, JTMS, JTCK, and JTRSTn are all standard JTAG signals complying with the IEEE-1149.1 specification. The sixth signal, JRTCK (Return TCK), is an output from the STR91xFA and it is used to pace the JTCK clock signal coming in from the external JTAG test equipment for debugging. The frequency of the JTCK clock signal coming from the JTAG test equipment must be at least 10 times less than the ARM966E-S CPU core operating frequency (f_{CPUCLK}). To ensure this, the signal JRTCK is output from the STR91xFA and is input to the external JTAG test equipment to hold off transitions of JTCK until the CPU core is ready, meaning that the JTAG equipment cannot send the next rising edge of JTCK until the equipment receives a rising edge of JRTCK from the STR91xFA. The JTAG test equipment must be able to interpret the signal JRTCK and perform this adaptive clocking function. If it is known that the CPU clock will always be at least ten times faster than the incoming JTCK clock signal, then the JRTCK signal is not needed.

The two die inside the STR91xFA (CPU die and Flash memory die) are internally daisy-chained on the JTAG bus, see *Figure 3 on page 28*. The CPU die has two JTAG Test Access Ports (TAPs), one for boundary scan functions and one for ARM CPU debug. The Flash memory die has one TAP for program/erase of non-volatile memory. Because these

6 Memory mapping

The ARM966E-S CPU addresses a single linear address space of 4 giga-bytes (2^{32}) from address 0x0000.0000 to 0xFFFF.FFFF as shown in *Figure 9*. Upon reset the CPU boots from address 0x0000.0000, which is chip-select zero at address zero in the Flash Memory Interface (FMI).

The Instruction TCM and Data TCM enable high-speed CPU operation without incurring any performance or power penalties associated with accessing the system buses (AHB and APB). I-TCM and D-TCM address ranges are shown at the bottom of the memory map in *Figure 9*.

6.1 Buffered and non-buffered writes

The CPU makes use of write buffers on the AHB and the D-TCM to decouple the CPU from any wait states associated with a write operation. The user may choose to use write with buffers on the AHB by setting bit 3 in control register CP15 and selecting the appropriate AHB address range when writing. By default at reset, buffered writes are disabled (bit 3 of CP15 is clear) and all AHB writes are non-buffered until enabled. *Figure 9* shows that most addressable items on the AHB are aliased at two address ranges, one for buffered writes and another for non-buffered writes. A buffered write will allow the CPU to continue program execution while the write-back is performed through a FIFO to the final destination on the AHB. If the FIFO is full, the CPU is stalled until FIFO space is available. A non-buffered write will impose an immediate delay to the CPU, but results in a direct write to the final AHB destination, ensuring data coherency. Read operations from AHB locations are always direct and never buffered.

6.2 System (AHB) and peripheral (APB) buses

The CPU will access SRAM, higher-speed peripherals (USB, Ethernet, Programmable DMA), and the external bus (EMI) on the AHB at their respective base addresses indicated in *Figure 9*. Lower-speed peripherals reside on the APB and are accessed using two separate AHB-to-APB bridge units (APB0 and APB1). These bridge units are essentially address windows connecting the AHB to the APB. To access an individual APB peripheral, the CPU will place an address on the AHB bus equal to the base address of the appropriate bridge unit APB0 or APB1, plus the offset of the particular peripheral, plus the offset of the individual data location within the peripheral. *Figure 9* shows the base addresses of bridge units APB0 and APB1, and also the base address of each APB peripheral. Please consult the STR91xFA Reference manual for the address of data locations within each individual peripheral.

7.4 RESET_INn and power-on-reset characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 13. RESET_INn and power-on-reset characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min(1)	Typ	Max	
t_{RINMIN}	RESET_INn Valid Active Low		100			ns
t_{POR}	Power-On-Reset Condition duration	V_{DDQ},V_{DD} ramp time is less than 10ms: 0V to V_{DD}	10			ms
t_{RSO}	RESET_OUT Duration (Watchdog reset)		one PCLK			ns

1. Data based on bench measurements, not tested in production.

7.5 LVD electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 14. LVD electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{DD_LVD+} (1.8V)	LVD threshold during V_{DD} rise		1.43	1.50	1.58	V
V_{DD_LVD-} (1.8V)	LVD threshold during V_{DD} fall		1.33	1.40	1.47	V
V_{DD_BRN} (1.8V)	V_{DD} brown out warning threshold			1.65		V
V_{DDQ_LVD+} (3.0V)	LVD threshold during V_{DDQ} rise	(1)(2)	2.32	2.45	2.57	V
V_{DDQ_LVD-} (3.0V)	LVD threshold during V_{DDQ} fall	(1)(2)	2.23	2.35	2.46	
V_{DDQ_BRN} (3.0V)	V_{DDQ} brown out warning threshold	(1)(2)		2.65		V
V_{DDQ_LVD+} (3.3V)	LVD threshold during V_{DDQ} rise	(2)(3)	2.61	2.75	2.89	V
V_{DDQ_LVD-} (3.3V)	LVD threshold during V_{DDQ} fall	(2)(3)	2.52	2.65	2.78	
V_{DDQ_BRN} (3.3V)	V_{DDQ} brown out warning threshold	(2)(3)		2.95		V

1. For V_{DDQ} I/O voltage operating at 2.7 - 3.3V.
2. Selection of V_{DDQ} operation range is made using configuration software from ST, or IDE from 3rd parties. The default condition is V_{DDQ}=2.7V - 3.3V.
3. For V_{DDQ} I/O voltage operating at 3.0 - 3.6V.

7.7.1 Main oscillator electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 18. Main oscillator electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{STUP(OSC)}$	Oscillator Start-up Time	V_{DD} stable (1)		2	3	mS

1. Data characterized with quartz crystal, not tested in production.

7.7.2 X1_CPU external clock source

Subject to general operating conditions for V_{DD} and T_A.

Table 19. External clock characteristics

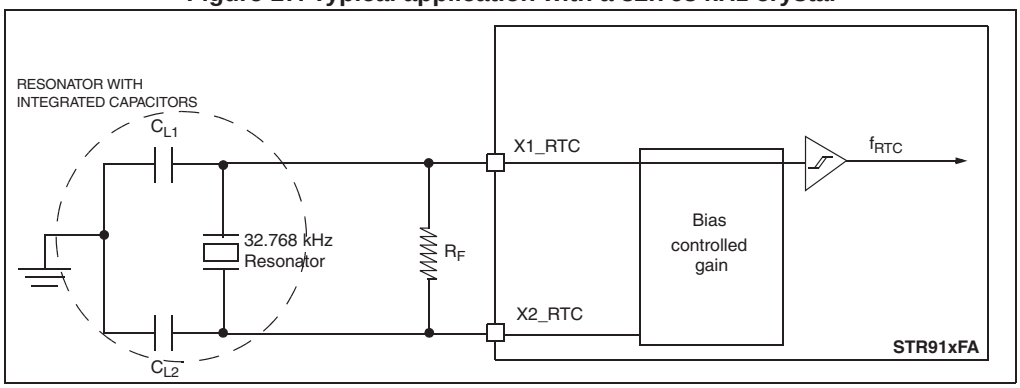
Symbol	Parameter	Test conditions(1)	Value			Unit
			Min	Typ	Max	
f_{X1}	External clock source frequency	See *Figure 16*	4		25	MHz
V_{X1H}	X1 input pin high level voltage		0.7xV_{DD}		V_{DD}	V
V_{X1L}	X1 input pin low level voltage		V_{SS}		0.3xV_{DD}	V
$t_{w(X1H)}$ $t_{w(X1L)}$	X1 high or low time(2)		6			ns
$t_{r(X1)}$ $t_{f(X1)}$	X1 rise or fall time(2)				20	ns
I_L	X1 input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
$C_{IN(X1)}$	X1 input capacitance(2)			5		pF
$DuCy_{(X1)}$	Duty cycle		45		55	%

1. Data based on typical appilcation software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Table 21. RTC crystal electrical characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			40	kΩ
C_L	Load capacitance			8	pF

Figure 17. Typical application with a 32.768 kHz crystal



7.7.4 PLL electrical characteristics

V_{DDQ} = 2.7 - 3.6V, V_{DD} = 1.65 - 2V, T_A = -40 / 85 °C unless otherwise specified.

Table 22. PLL electrical characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL}	PLL output clock	6.25		$f_{CPUCLKmax}$	MHz
f_{OSC}	Clock input	4		25	MHz
t_{LOCK}	PLL lock time		300	1500	µs
Δt_{JITTER}	PLL jitter (peak to peak)(1)		0.1	0.2	ns

1. Data based on bench measurements, not tested in production

7.10 I/O characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 31. I/O characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level	General inputs(1)	2.0		(2)	V
		RESET and TCK inputs(1)	0.8 V_{DDQ}			
		TAMPER_IN input(3) (Run mode)	V_{DDQ}/2			
		TAMPER_IN input(3) (Standby mode)	V_{BAT}/2			
V_{IL}	Input low level	General inputs(1)			0.8	
		RESET and TCK inputs(1)			0.2 V_{DDQ}	
		TAMPER_IN input(3) (Run mode)			V_{DDQ}/2	
		TAMPER_IN input(3) (Standby mode)			V_{BAT}/2	
V_{HYS}	Input hysteresis Schmitt trigger	General inputs(4)			0	V
V_{OH}	Output high level High current pins	I/O ports 3 and 6: Push-Pull, I_{OH} = 8mA	V_{DDQ}-0.7			V
	Output high level Standard current pins	I/O ports 0,1,2,4,5,7,8,9: Push-Pull, I_{OH} = 4mA	V_{DDQ}-0.7			
	Output high level JTAG JTDO pin	I_{OH}= -100 µA	V_{DDQ}-0.1			
V_{OL}	Output low level High current pins	I/O ports 3 and 6: Push-Pull, I_{OL} = 8mA			0.4	V
	Output low level Standard current pins	I/O ports 0,1,2,4,5,7,8,9: Push-Pull, I_{OL} = 4mA			0.4	
	Output low level JTAG JTDO pin	I_{OL}=100 µA			0.1	

1. Guaranteed by characterization, not tested in production.
2. Input pins are 5V tolerant, max input voltage is 5.5V
3. Guaranteed by design, not tested in production.
4. TAMPER_IN pin and STR9 general inputs have no built-in hysteresis.

Sync burst read

Figure 24. Sync burst read diagram

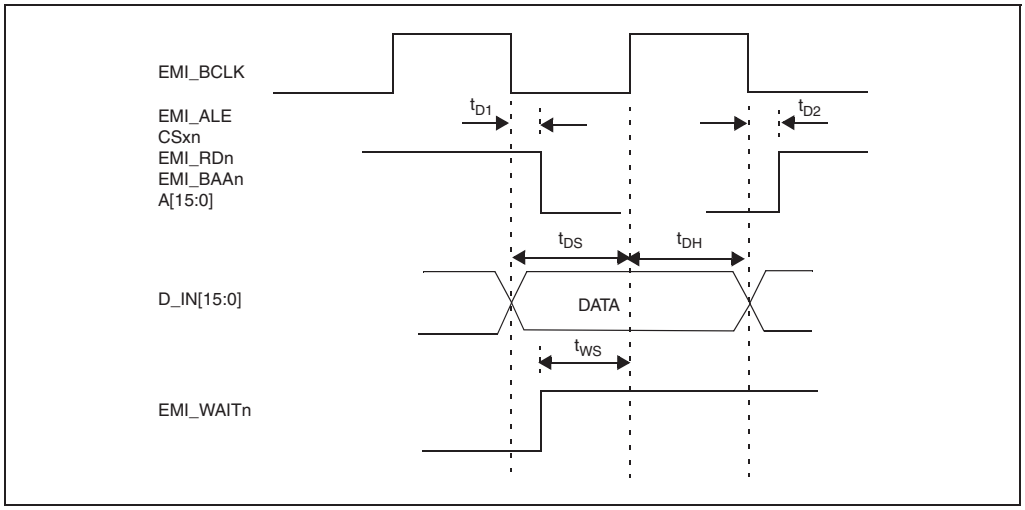


Table 39. Sync burst read times

Symbol	Parameter	Value	
		Min	Max
t_{D1BAA}	BAA t_{D1}	0 ns	2 ns
t_{D2BAA}	BAA t_{D2}	0.5ns	2.5 ns
t_{D1ALE}	ALE t_{D1}	1 ns	3.5 ns
t_{D2ALE}	ALE t_{D2}	$(t_{BCLK}/2)$+0.5 ns	$(t_{BCLK}/2)$+3 ns
t_{D1RD}	RD t_{D1}	0	2 ns
t_{D2RD}	RD t_{D2}	0.5 ns	2.5 ns
t_{D1A}	Address t_{D1}	2 ns	4 ns
t_{D2A}	Address t_{D2}	2.5 ns	3.5 ns
t_{D1CS}	CS t_{D1}	0.5 ns	3 ns
t_{D2CS}	CS t_{D2}	1 ns	3.5 ns
t_{WS}	WAIT set up time	1 ns	4 ns
t_{DS}	Data setup time	4.5 ns	-
t_{DH}	Data hold time	0	-

7.12.5 SPI electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 46. SPI electrical characteristics

Symbol	Parameter	Test conditions	Value		Unit
			Typ	Max	
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master		24	MHz
		Slave		4	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall times	50pF load	0.1		V/ns
$t_{su(SS)}$	SS setup time	Slave	1		t_{PCLK}
$t_{h(SS)}$	SS hold time	Slave	1		
$t_{w(SCLKH)}$ $t_{w(SCLKL)}$	SCLK high and low time	Master Slave	1		
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master Slave	TBD 5		
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master Slave	TBD 6		
$t_{a(SO)}$	Data output access time	Slave		6	
$t_{dis(SO)}$	Data output disable time	Slave		6	
$t_{v(SO)}$	Data output valid time	Slave (after enable edge)		6	
$t_{h(SO)}$	Data output hold time		0		
$t_{v(MO)}$	Data output valid time	Master (before capture edge)	0.25		
$t_{h(MO)}$	Data output hold time		0.25		

Figure 30. SPI slave timing diagram with CPHA = 0

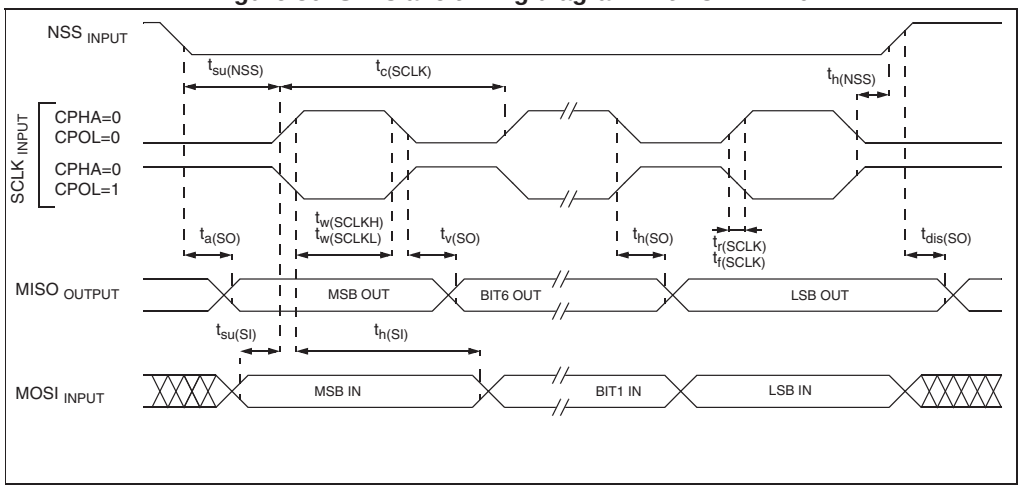


Figure 31. SPI slave timing diagram with CPHA = 1

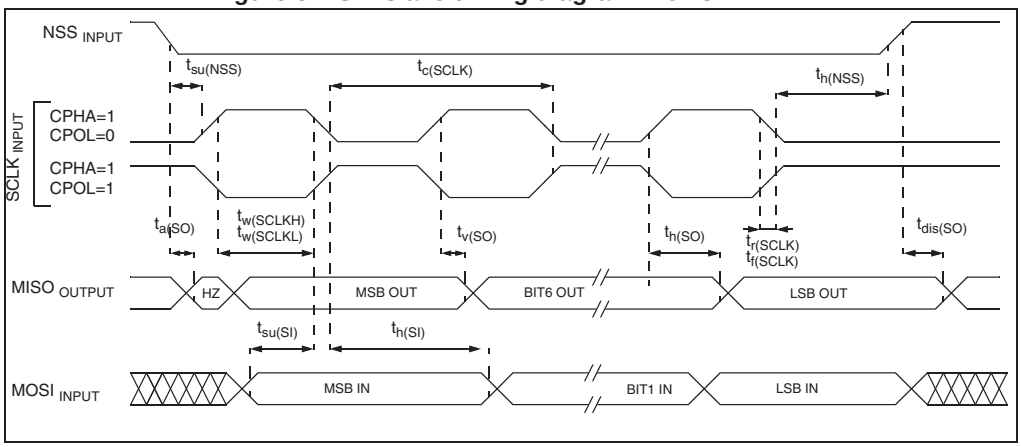


Figure 32. SPI master timing diagram

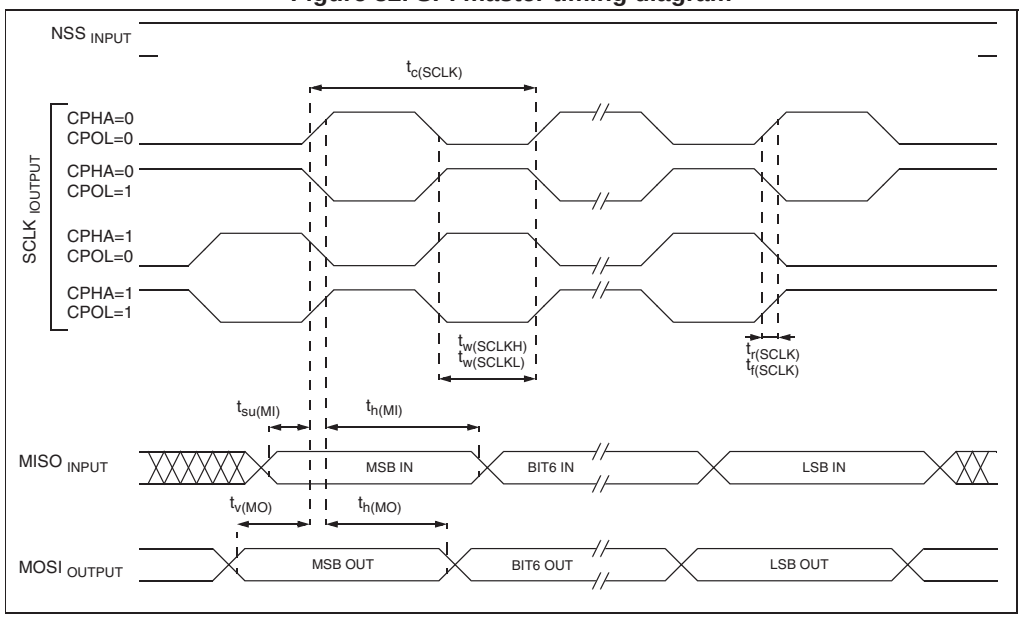
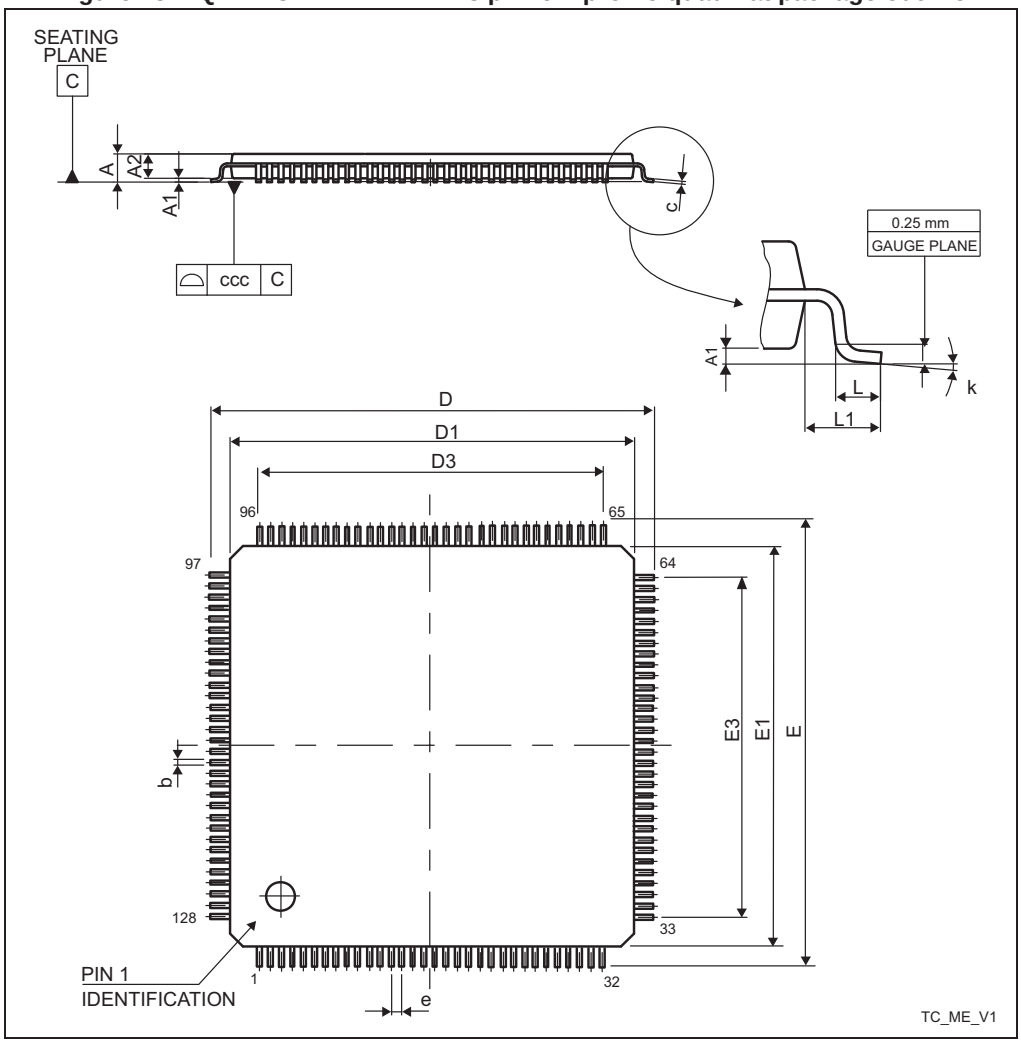


Figure 43. LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 51. LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.130	0.180	0.230	0.0051	0.0071	0.0091
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.400	-	-	0.4882	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.400	-	-	0.4882	-
e	-	0.400	-	-	0.0157	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 52.LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A[2]	-	-	1.700			0.0669
A1	0.210	-	-	0.0083		
A2	-	1.060	-		0.0417	
A3		0.026			0.0010	
A4	-	0.800	-	-	0.0315	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	8.800	-	-	0.3465	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	0.100			0.0039		
eee	0.150			0.0059		
fff	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.

Table 55. Document revision history

Date	Revision	Changes
02-Jul-2009	6	*Section 3.13.7: Tamper detection*: Removed information about “Normally Closed/Tamper Open mode”. *Table 31: I/O characteristics*: Updated V_{HYS} row.
3-Mar-2015	7	Updated *Figure 40: LQFP80 12 x 12 mm 80 pin low-profile quad flat package outline on page 95*, *Figure 43: LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline on page 98* and *Figure 45: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline on page 101* Updated *Table 50: LQFP80 12 x12 mm low-profile quad flat package mechanical data on page 96*, *Table 51: LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package mechanical data on page 99*, and *Table 52: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data on page 102* Added *Figure 42: LQFP80 package top view on page 97*, *Figure 43: LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline on page 98*, *Figure 44: LQFP128 package top view on page 100* and *Figure 45: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline on page 101*

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