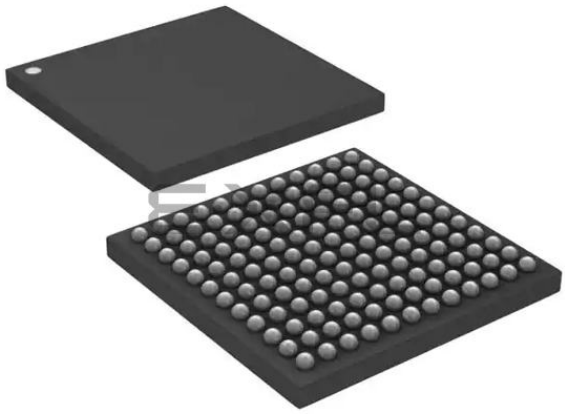

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str912faz44h6t

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2 Device summary

Table 2. Device summary

Part number	Flash KB	RAM KB	Major peripherals	Package
STR910FAM32	**256+32**	64	**CAN, 40 I/Os**	**LQFP80, 12x12 mm**
STR910FAW32	**256+32**	64	**CAN, EMI, 80 I/Os**	**LQFP128, 14x14 mm**
STR910FAZ32	**256+32**	64	**CAN, EMI, 80 I/Os**	LFBGA144 10 x 10 x 1.7
STR911FAM42	**256+32**	96	**USB, CAN, 40 I/Os**	**LQFP80, 12x12mm**
STR911FAM44	**512+32**	96		
STR911FAM46	**1024+128**	96	**USB, CAN, 40 I/Os**	**LQFP80, 12x12mm**
STR911FAM47	**2048+128**	96		
STR911FAW42	**256+32**	96	**USB, CAN, EMI, 80 I/Os**	**LQFP128, 14x14mm**
STR911FAW44	**512+32**	96		
STR911FAW46	**1024+128**	96	**USB, CAN, EMI, 80 I/Os**	**LQFP128, 14x14mm**
STR911FAW47	**2048+128**	96		
STR912FAW32	**256+32**	64	**Ethernet, USB, CAN, EMI, 80 I/Os**	**LQFP128**
STR912FAW42	**256+32**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	**LQFP128**
STR912FAW44	**512+32**	96		
STR912FAW46	**1024+128**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	**LQFP128**
STR912FAW47	**2048+128**	96		
STR912FAZ42	**256+32**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	LFBGA144 10 x 10 x 1.7
STR912FAZ44	**512+32**	96		
STR912FAZ46	**1024+128**	96	**Ethernet, USB, CAN, EMI, 80 I/Os**	LFBGA144 10 x 10 x 1.7
STR912FAZ47	**2048+128**	96		

3.10.11 Operation example

As an example of CCU operation, a 25 MHz crystal can be connected to the main oscillator input on pins X1_CPU and X2_CPU, a 32.768 kHz crystal connected to pins X1_RTC and X2_RTC, and the clock input of an external Ethernet PHY device is connected to STR91xFA output pin P5.2. In this case, the CCU can run the CPU at 96 MHz from PLL, the USB interface at 48 MHz, and the Ethernet interface at 25 MHz. The RTC is always running in the background at 32.768 kHz, and the CPU can go to very low power mode dynamically by running from 32.768 kHz and shutting off peripheral clocks and the PLL as needed.

3.11 Flexible power management

The STR91xFA offers configurable and flexible power management control that allows the user to choose the best power option to fit the application. Power consumption can be dynamically managed by firmware and hardware to match the system's requirements. Power management is provided via clock control to the CPU and individual peripherals.

Clocks to the CPU and peripherals can be individually divided and gated off as needed. In addition to individual clock divisors, the CCU master clock source going to the CPU, AHB, APB, EMI, and FMI can be divided dynamically by as much as 1024 for low power operation. Additionally, the CCU may switch its input to the 32.768 kHz RTC clock at any time for low power.

The STR91xFA supports the following three global power control modes:

- ***Run Mode*:** All clocks are on with option to gate individual clocks off via clock mask registers.
- ***Idle Mode*:** CPU and FMI clocks are off until an interrupt, reset, or wake-up occurs. Pre-configured clock mask registers selectively allow individual peripheral clocks to continue run during Idle Mode.
- ***Sleep Mode*:** All clocks off except RTC clock. Wake up unit remains powered, PLL is forced off.

A special mode is used when JTAG debug is active which never gates off any clocks even if the CPU enters Idle or Sleep mode.

3.11.1 Run mode

This is the default mode after any reset occurs. Firmware can gate off or scale any individual clock. Also available is a special Interrupt Mode which allows the CPU to automatically run full speed during an interrupt service and return back to the selected CPU clock divisor rate when the interrupt has been serviced. The advantage here is that the CPU can run at a very low frequency to conserve power until a periodic wake-up event or an asynchronous interrupt occurs at which time the CPU runs full speed immediately.

3.13.7 Tamper detection

On 128-pin and 144-ball STR91xFA devices only, there is a tamper detect input pin, TAMPER_IN, used to detect and record the time of a tamper event on the end product such as malicious opening of an enclosure, unwanted opening of a panel, etc. The activation mode of the tamper pin detects when a signal on the tamper input pin is driven from low-to-high, or high-to-low depending on firmware configuration. Once a tamper event occurs, the RTC time (millisecond resolution) and the date are recorded in the RTC unit. Simultaneously, the SRAM standby voltage source will be cut off to invalidate all SRAM contents. Tamper detection control and status logic are part of the RTC unit.

3.14 Real-time clock (RTC)

The RTC combines the functions of a complete time-of-day clock (millisecond resolution) with an alarm programmable up to one month, a 9999-year calender with leap-year support, periodic interrupt generation from 1 to 512 Hz, tamper detection (described in *Section 3.13.7*), and an optional clock calibration output on the JRTCK pin. The time is in 24 hour mode, and time/calendar values are stored in binary-coded decimal format.

The RTC also provides a self-isolation mode that is automatically activated during power down. This feature allows the RTC to continue operation when V_{DDQ} and V_{DD} are absent, as long as an alternate power source, such as a battery, is connected to the VBATT input pin. The current drawn by the RTC unit on the VBATT pin is very low in this standby mode, I_{RTC_STBY}.

3.15 JTAG interface

An IEEE-1149.1 JTAG interface on the STR91xFA provides In-System-Programming (ISP) of all memory, boundary scan testing of pins, and the capability to debug the CPU.

STR91xFA devices are shipped from ST with blank Flash memories. The CPU can only boot from Flash memory (selection of which Flash bank is programmable). Firmware must be initially programmed through JTAG into one of these Flash memories before the STR91xFA is used.

Six pins are used on this JTAG serial interface. The five signals JTDI, JTDO, JTMS, JTCK, and JTRSTn are all standard JTAG signals complying with the IEEE-1149.1 specification. The sixth signal, JRTCK (Return TCK), is an output from the STR91xFA and it is used to pace the JTCK clock signal coming in from the external JTAG test equipment for debugging. The frequency of the JTCK clock signal coming from the JTAG test equipment must be at least 10 times less than the ARM966E-S CPU core operating frequency (f_{CPUCLK}). To ensure this, the signal JRTCK is output from the STR91xFA and is input to the external JTAG test equipment to hold off transitions of JTCK until the CPU core is ready, meaning that the JTAG equipment cannot send the next rising edge of JTCK until the equipment receives a rising edge of JRTCK from the STR91xFA. The JTAG test equipment must be able to interpret the signal JRTCK and perform this adaptive clocking function. If it is known that the CPU clock will always be at least ten times faster than the incoming JTCK clock signal, then the JRTCK signal is not needed.

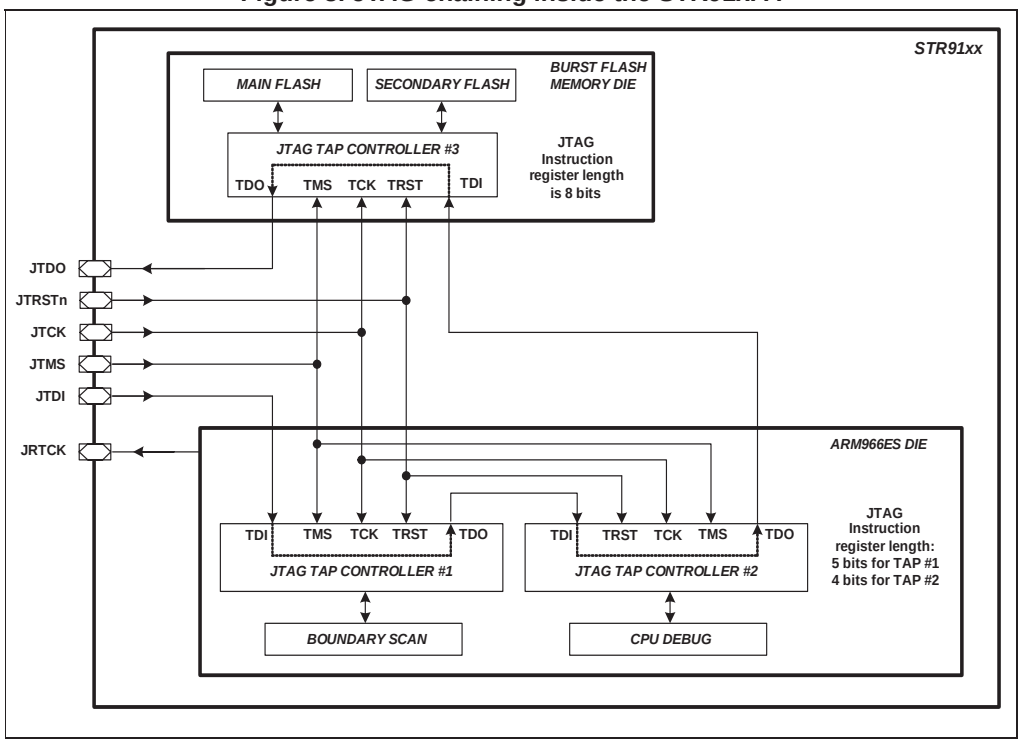
The two die inside the STR91xFA (CPU die and Flash memory die) are internally daisy-chained on the JTAG bus, see *Figure 3 on page 28*. The CPU die has two JTAG Test Access Ports (TAPs), one for boundary scan functions and one for ARM CPU debug. The Flash memory die has one TAP for program/erase of non-volatile memory. Because these

three TAPs are daisy-chained, only one TAP will converse on the JTAG bus at any given time while the other two TAPs are in BYPASS mode. The TAP positioning order within this JTAG chain is the boundary scan TAP first, followed by the ARM debug TAP, followed by the Flash TAP. All three TAP controllers are reset simultaneously by one of two methods:

- A chip-level global reset, caused only by a Power-On-Reset (POR) or a Low Voltage Detect (LVD).
- A reset command issued by the external JTAG test equipment. This can be the assertion of the JTAG JTRSTn input pin on the STR91xFA or a JTAG reset command shifted into the STR91xFA serially.

This means that chip-level system resets from watchdog time-out or the assertion of RESET_INn pin do not affect the operation of any JTAG TAP controller. Only global resets effect the TAPs.

Figure 3. JTAG chaining inside the STR91xFA



3.15.1 In-system-programming

The JTAG interface is used to program or erase all memory areas of the STR91xFA device. The pin RESET_INn must be asserted during ISP to prevent the CPU from fetching invalid instructions while the Flash memories are being programmed.

Note that the 32 bytes of OTP memory locations cannot be erased by any means once programmed by JTAG ISP or the CPU.

3.15.2 Boundary scan

Standard JTAG boundary scan testing compliant with IEEE-1149.1 is available on the majority of pins of the STR91xFA for circuit board test during manufacture of the end product. STR91xFA pins that are not serviced by boundary scan are the following:

- JTAG pins JTCK, JTMS, JTDI, JTDO, JTRSTn, JRTCK
- Oscillator input pins X1_CPU, X2_CPU, X1_RTC, X2_RTC
- Tamper detect input pin TAMPER_IN (128-pin and 144-pin packages only)

3.15.3 CPU debug

The ARM966E-S CPU core has standard ARM EmbeddedICE-RT logic, allowing the STR91xFA to be debugged through the JTAG interface. This provides advanced debugging features making it easier to develop application firmware, operating systems, and the hardware itself. Debugging requires that an external host computer, running debug software, is connected to the STR91xFA target system via hardware which converts the stream of debug data and commands from the host system's protocol (USB, Ethernet, etc.) to the JTAG EmbeddedICE-RT protocol on the STR91xFA. These protocol converters are commercially available and operate with debugging software tools.

The CPU may be forced into a Debug State by a breakpoint (code fetch), a watchpoint (data access), or an external debug request over the JTAG channel, at which time the CPU core and memory system are effectively stopped and isolated from the rest of the system. This is known as Halt Mode and allows the internal state of the CPU core, memory, and peripherals to be examined and manipulated. Typical debug functions are supported such as run, halt, and single-step. The EmbeddedICE-RT logic supports two hardware compare units. Each can be configured to be either a watchpoint or a breakpoint. Breakpoints can also be data-dependent.

Debugging (with some limitations) may also occur through the JTAG interface while the CPU is running full speed, known as Monitor Mode. In this case, a breakpoint or watchpoint will not force a Debug State and halt the CPU, but instead will cause an exception which can be tracked by the external host computer running monitor software. Data can be sent and received over the JTAG channel without affecting normal instruction execution. Time critical code, such as Interrupt Service Routines may be debugged real-time using Monitor Mode.

3.15.4 JTAG security bit

This is a non-volatile bit (Flash memory based), which when set will not allow the JTAG debugger or JTAG programmer to read the Flash memory contents.

Using JTAG ISP, this bit is typically programmed during manufacture of the end product to prevent unwanted future access to firmware intellectual property. The JTAG Security Bit can be cleared only by a JTAG "Full Chip Erase" command, making the STR91xFA device blank (except for programmed OTP bytes), and ready for programming again. The CPU can read the status of the JTAG Security Bit, but it may not change the bit value.

EMI_BWR_WRLn is the data write strobe, and the output on pin EMI_RDn is the data read strobe.

- ***8-bit non-multiplexed data mode*** (*Figure 6*): Eight bits of data are on port 8, while 16 bits of address are output on ports 7 and 9. The output signal on pin EMI_BWR_BWLn is the data write strobe and the output on pin EMI_RDn is the data read strobe.
- ***Burst Mode Support (LFBGA package only)*****:** The EMI bus supports synchronized burst read and write bus cycle in multiplexed and non-multiplexed mode. The additional EMI signals in the LFBGA package that support the burst mode are:
  - EMI_BCLK -the bus clock output. The EMI_BCLK has the same frequency or half of that of the HCLK and can be disabled by the user
  - EMI_WAITn - the not ready or wait input signal for synchronous access
  - EMI_BAAn - burst address advance or burst enable signal
  - EMI_WEn - write enable signal
  - EMI_UBn, EMI_LBn - upper byte and lower byte enable signals. These two signals share the same pins as the EMI_WRLn and EMI_WRHn and are user configurable through the EMI register.

  By defining the bus parameters such as burst length, burst type, read and write timings in the EMI control registers, the EMI bus is able to interface to standard burst memory devices. The burst timing specification and waveform will be provided in the next data sheet release

5.2 Default pin functions

During and just after reset, all pins on ports 0-9 default to high-impedance input mode until CPU firmware assigns other functions to the pins. This initial input mode routes all pins on ports 0-9 to be read as GPIO inputs as shown in the “Default Pin Function” column of *Table 8*. Simultaneously, certain port pin signals are also routed to other functional inputs as shown in the “Default Input Function” column of *Table 8*, and these pin input functions will remain until CPU firmware makes other assignments. At any time, even after the CPU assigns pins to alternate functions, the CPU may always read the state of any pin on ports 0-9 as a GPIO input. CPU firmware may assign alternate functions to port pins as shown in columns “Alternate Input 1” or “Alternate Output 1, 2, 3” of *Table 8* by writing to control registers at run-time.

5.2.1 General notes on pin usage

1 *Since there are no internal or programmable pull-up resistors on ports 0-9, it is advised to pull down to ground, or pull up to VDDQ (using max. 47 KΩ resistors), all unused pins on port 0-9. Another solution is to use the GPIO control registers to configure the unused pins on ports 0-9 as output low level. The purpose of this is to reduce noise susceptibility, noise generation, and minimize power consumption*

2 *All pins on ports 0 - 9 are 5V tolerant*

3 *Pins on ports 0,1,2,4,5,7,8,9 have 4 mA drive and 4mA sink. Ports 3 and 6 have 8 mA drive and 8 mA sink.*

4 *For 8-bit non-muxed EMI operation: Port 8 is eight bits of data, ports 7 and 9 are 16 bits of address.*

5 *For 16-bit muxed EMI operation: Ports 8 and 9 are 16 bits of muxed address and data bits, port 7 is up to eight additional bits of high-order address*

6 *Signal polarity is programmable for interrupt request inputs, EMI_ALE, timer input capture inputs and output compare/PWM outputs, motor control tach and emergency stop inputs, and motor control phase outputs.*

7 *HiZ = High Impedance, V = Voltage Source, G = Ground, I/O = Input/Output*

8 *STR910FA devices do not support USB. On these devices USBDP and USBDN signals are "Not Used" (USBDN is not connected, USBDP must be pulled up by a 1.5K ohm resistor to VDDQ), and all functions named “USB" are not available.*

9 *STR910FA 128-pin and 144-ball devices do not support Ethernet. On these devices PHYCLK and all functions named “MII*" are not available.*

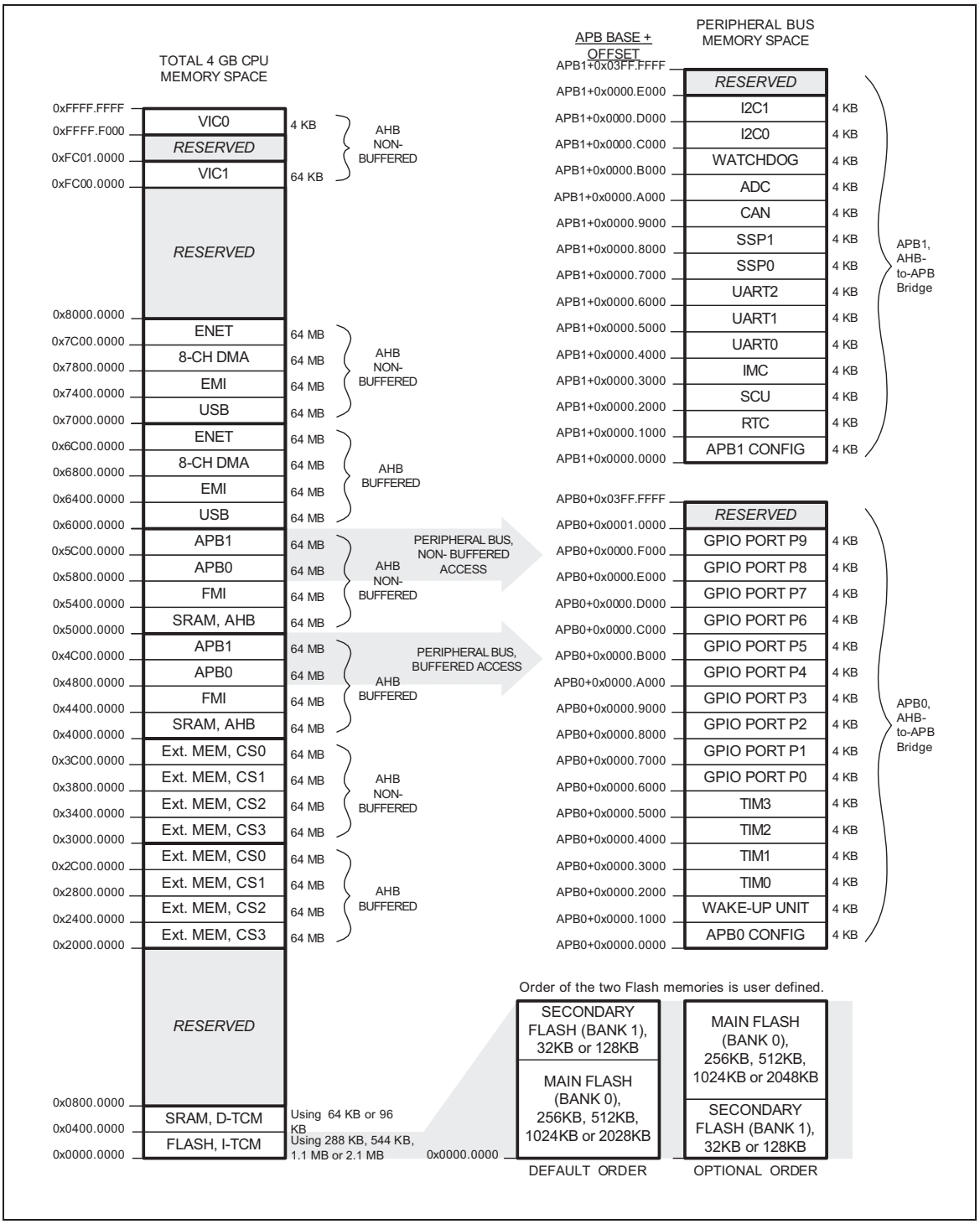
Table 8. Device pin description

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	67	L11	P0.0	I/O	GPIO_0.0, GP Input, HiZ	MII_TX_CLK, PHY Xmit clock	I2C0_CLKIN, I2C clock in	GPIO_0.0, GP Output	I2C0_CLKOUT, I2C clock out	ETM_PCK0, ETM Packet
-	69	K10	P0.1	I/O	GPIO_0.1, GP Input, HiZ	-	I2C0_DIN, I2C data in	GPIO_0.1, GP Output	I2C0_DOUT, I2C data out	ETM_PCK1, ETM Packet
-	71	J11	P0.2	I/O	GPIO_0.2, GP Input, HiZ	MII_RXD0, PHY Rx data0	I2C1_CLKIN, I2C clock in	GPIO_0.2, GP Output	I2C1_CLKOUT, I2C clock out	ETM_PCK2, ETM Packet
-	76	H12	P0.3	I/O	GPIO_0.3, GP Input, HiZ	MII_RXD1, PHY Rx data	I2C1_DIN, I2C data in	GPIO_0.3, GP Output	I2C1_DOUT, I2C data out	ETM_PCK3, ETM Packet
-	78	H10	P0.4	I/O	GPIO_0.4, GP Input, HiZ	MII_RXD2, PHY Rx data	TIM0_ICAP1, Input Capture	GPIO_0.4, GP Output	EMI_CS0n, EMI Chip Select	ETM_PSTAT0, ETM pipe status
-	85	F11	P0.5	I/O	GPIO_0.5, GP Input, HiZ	MII_RXD3, PHY Rx data	TIM0_ICAP2, Input Capture	GPIO_0.5, GP Output	EMI_CS1n, EMI Chip Select	ETM_PSTAT1, ETM pipe status
-	88	E11	P0.6	I/O	GPIO_0.6, GP Input, HiZ	MII_RX_CLK, PHY Rx clock	TIM2_ICAP1, Input Capture	GPIO_0.6, GP Output	EMI_CS2n, EMI Chip Select	ETM_PSTAT2, ETM pipe status
-	90	B12	P0.7	I/O	GPIO_0.7, GP Input, HiZ	MII_RX_DV, PHY data valid	TIM2_ICAP2, Input Capture	GPIO_0.7, GP Output	EMI_CS3n, EMI Chip Select	ETM_TRSYNC, ETM trace sync
-	98	B10	P1.0	I/O	GPIO_1.0, GP Input, HiZ	MII_RX_ER, PHY rcv error	ETM_EXTRIG, ETM ext. trigger	GPIO_1.0, GP Output	UART1_TX, UART xmit data	SSP1_SCLK, SSP mstr clk out
-	99	C10	P1.1	I/O	GPIO_1.1, GP Input, HiZ	-	UART1_RX, UART rcv data	GPIO_1.1, GP Output	MII_TXD0, MAC Tx data	SSP1_MOSI, SSP mstr dat out
-	101	B9	P1.2	I/O	GPIO_1.2, GP Input, HiZ	-	SSP1_MISO, SSP mstr data in	GPIO_1.2, GP Output	MII_TXD1, MAC Tx data	UART0_TX, UART xmit data
-	106	C8	P1.3	I/O	GPIO_1.3, GP Input, HiZ	-	UART2_RX, UART rcv data	GPIO_1.3, GP Output	MII_TXD2, MAC Tx data	SSP1_NSS, SSP mstr sel out
-	109	B7	P1.4	I/O	GPIO_1.4, GP Input, HiZ	-	I2C0_CLKIN, I2C clock in	GPIO_1.4, GP Output	MII_TXD3, MAC Tx data	I2C0_CLKOUT, I2C clock out
-	110	A7	P1.5	I/O	GPIO_1.5, GP Input, HiZ	MII_COL, PHY collision	CAN_RX, CAN rcv data	GPIO_1.5, GP Output	UART2_TX, UART xmit data	ETM_TRCLK, ETM trace clock
-	114	F7	P1.6	I/O	GPIO_1.6, GP Input, HiZ	MII_CRS, PHY carrier sns	I2C0_DIN, I2C data in	GPIO_1.6, GP Output	CAN_TX, CAN Tx data	I2C0_DOUT, I2C data out
-	116	D6	P1.7	I/O	GPIO_1.7, GP Input, HiZ	-	ETM_EXTRIG, ETM ext. trigger	GPIO_1.7, GP Output	MII_MDC, MAC mgt dat ck	ETM_TRCLK, ETM trace clock
7	10	E2	P2.0	I/O	GPIO_2.0, GP Input, HiZ	UART0_CTS, Clear To Send	I2C0_CLKIN, I2C clock in	GPIO_2.0, GP Output	I2C0_CLKOUT, I2C clock out	ETM_PCK0, ETM Packet
8	11	E3	P2.1	I/O	GPIO_2.1, GP Input, HiZ	UART0_DSR, Data Set Ready	I2C0_DIN, I2C data in	GPIO_2.1, GP Output	I2C0_DOUT, I2C data out	ETM_PCK1, ETM Packet
21	33	M1	P2.2	I/O	GPIO_2.2, GP Input, HiZ	UART0_DCD, Dat Carrier Det	I2C1_CLKIN, I2C clock in	GPIO_2.2, GP Output	I2C1_CLKOUT, I2C clock out	ETM_PCK2, ETM Packet
22	35	K3	P2.3	I/O	GPIO_2.3, GP Input, HiZ	UART0_RI, Ring Indicator	I2C1_DIN, I2C data in	GPIO_2.3, GP Output	I2C1_DOUT, I2C data out	ETM_PCK3, ETM Packet
23	37	L4	P2.4	I/O	GPIO_2.4, GP Input, HiZ	EXTCLK_T0T1E xt clk timer0/1	SSP0_SCLK, SSP slv clk in	GPIO_2.4, GP Output	SSP0_SCLK, SSP mstr clk out	ETM_PSTAT0, ETM pipe status

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	8	L2	VSSQ	G	Digital Ground for !/O and USB	N/A				
16	24	K4	VSSQ	G						
35	56	C5	VSSQ	G						
-	-	D4	VSSQ	G						
45	72	G5	VSSQ	G						
55	87	J7	VSSQ	G						
25	40	A8	VSSQ	G						
66	105	F8	VSSQ	G						
75	121	L12	VSSQ	G						
11	17	F4	VDD	V	V Source for CPU. 1.65 V - 2.0 V	N/A				
31	49	D7	VDD	V						
50	81	L6	VDD	V						
70	112	G11	VDD	V						
10	16	F3	VSS	G	Digital Ground for CPU	N/A				
30	48	H5	VSS	G						
51	82	G10	VSS	G						
71	113	E7	VSS	G						
-	-	C9	PLLV DDQ	V	V Source for PLL 2.7 to 3.6 V	N/A				
-	-	B8	PLLV SSQ	G	Digital Ground for PLL					

Figure 9. STR91xFA memory map



7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$max (given by the selected temperature range).

Data based on product characterisation, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25° C, V_{DDQ} = 3.3 V and V_{DD}=1.8 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

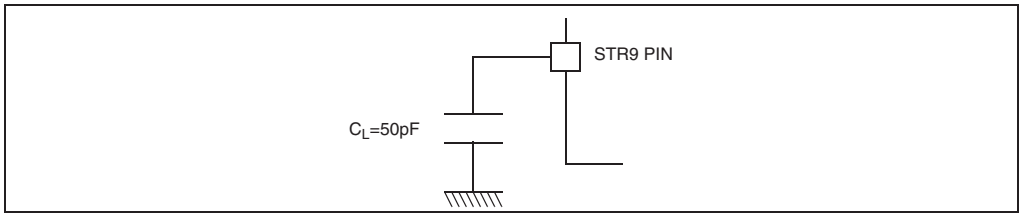
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

Figure 10. Pin loading conditions



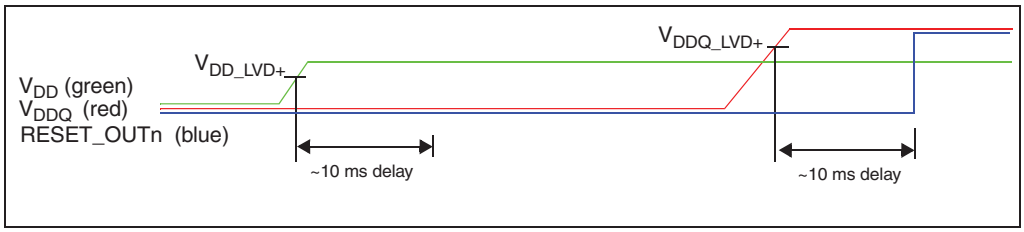
7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

7.5.1 LVD delay timing

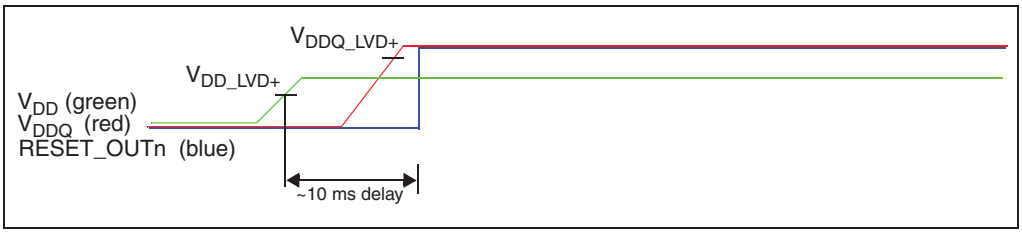
Case 1: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **after** the first ~10 ms delay (introduced by the VDD rising edge), a new ~10 ms delay starts before the release of RESET_OUTn. See *Figure 12.*

Figure 12. LVD reset delay case 1



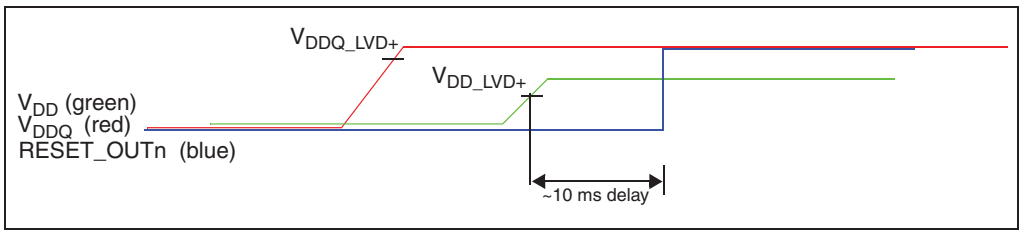
Case 2: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **before** the first ~10 ms delay (introduced by the VDD rising edge), RESET_OUTn will be released immediately at the end of the delay. No new delay is introduced in this case. See *Figure 13.*

Figure 13. LVD reset delay case 2



Case 3: When V_{DD} reaches the V_{DD_LVD+} threshold **after** the V_{DDQ} rising edge, RESET_OUTn will be released at the end of a ~10 ms delay. See *Figure 14*

Figure 14. LVD reset delay case 3



7.6 Supply current characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 15. Supply current characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
I_{DDRUN}	Run mode current	All peripherals on(1)(2)		1.7	2.3	mA/MHz
		All peripherals off(1)(2)		1.3	1.6	
I_{IDLE}	Idle mode current	All peripherals on (2)(3)		1.14	1.7	mA/MHz
		All peripherals off(2)(4)		0.45	0.75	mA/MHz
$I_{SLEEP(IDD)}$	Sleep mode current, I_{DD}	ARM core and all peripheral clocks stopped (with exception of RTC), LVD off		50	820(5)	µA
		ARM core and all peripheral clocks stopped (with exception of RTC), LVD on		55	825(5)	
$I_{SLEEP(IDDQ)}$	Sleep mode current, I_{DDQ}	LVD On (4)		7	80(5)	µA
		LVD Off (4)		7	70(5)	µA
I_{RTC_STBY}	RTC Standby current	Measured on VBATT pin		0.9	1.2	µA
I_{SRAM_STBY}	SRAM Standby current	Measured on VBATT pin		5	240	µA

1. ARM core and peripherals active with all clocks on. Power can be conserved by turning off clocks to peripherals which are not required.
2. mA/MHz data valid down to 10 MHz. Below this frequency the ratio mA/MHz increases.
3. ARM core stopped and all peripheral clocks active.
4. ARM core stopped and all peripheral clocks stopped.
5. Results based on characterization, not tested in production.

Table 25. Flash memory program/erase characteristics (Flash size = 1 MB / 2 MB)

Parameter		Test conditions	Value			Unit
			Typ(1)	Typ after 100K W/E cycles(1)	Max	
Bank erase	Primary bank (2 Mbytes)		32	36	46	s
	Primary bank (1 Mbytes)		16	18	23	s
	Secondary bank (128 Kbytes)		2.5	3	4	s
Sector erase	Of primary bank (64 Kbytes)		1300	1400	1800	ms
	Of secondary bank (16 Kbytes)		500	600	850	ms
Bank program	Primary bank (2 Mbytes)		15	20	22	s
	Primary bank (1 Mbytes)		7.5	10	11	s
	Secondary bank (128 Kbytes)		1060	1140	1380	ms
Sector program	Of primary bank (64 Kbytes)		500	520	640	ms
	Of secondary bank (16 Kbytes)		120	130	160	ms
Word program		Half word (16 bits)	8	9	11	µs

1. V_{DD} = 1.8 V, V_{DDQ} = 3.3 V, T_A = 2 5°C.

Table 26. Flash memory endurance

Parameter	Test conditions	Value			Unit
		Min	Typ	Max	
Program/erase cycles	Per word	100K			cycles
Data retention		20			years

Non-mux read

Figure 19. Non-mux bus read timings

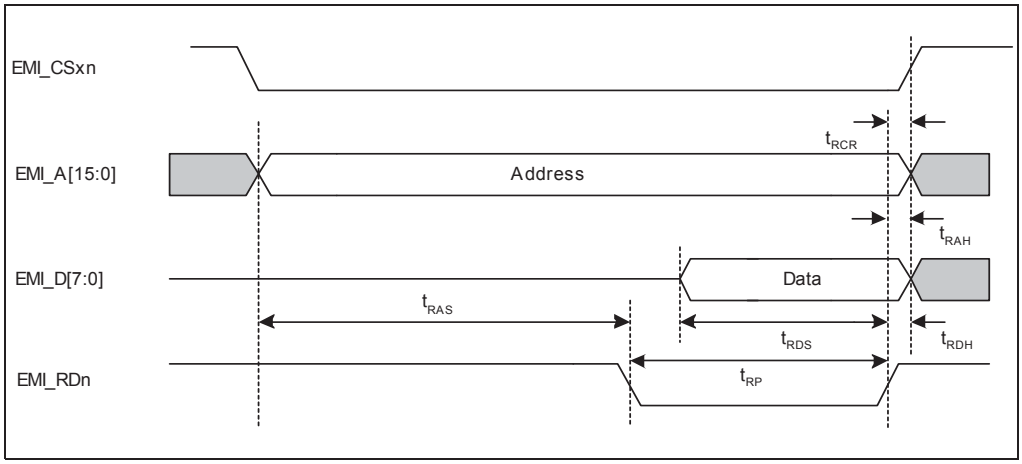


Table 34. EMI read operation

Symbol	Parameter	Value	
		Min	Max
t_{RCR}	Read to CSn inactive	0	1.5 ns
t_{RAS}	Read address setup time	((WSTOEN) x t_{BCLK})- 1.5 ns	(WSTOEN) x t_{BCLK}
t_{RDS}	Read data setup time	12.5	-
t_{RDH}	Read data hold time	0	-
t_{RP}	Read pulse width	((WSTRD-WSTOEN+1) x t_{BCLK})- 0.5 ns	((WSTRD-WSTOEN+1) x t_{BCLK})+ 2 ns

Table 48. ADC conversion time (silicon Rev G)

Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$2*16/f_{ADC}$		$3*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	1.33		2	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			500	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev G. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained on conversions started by trigger in single mode
4. All sucessive conversions in continuous and scan modes.

Table 49. ADC conversion time (silicon Rev H and higher)

Symbol	Parameter(1) (2)	Test conditions	Value			Unit
			Min	Typ	Max	
$t_{CONV(S)}$	Single mode conversion time		$1*16/f_{ADC}$		$2*16/f_{ADC}$	µs
		f_{ADC} = 24 MHz	0.66		1.33	
TR(S)	Single mode throughput rate (3)	f_{ADC} = 24 MHz			750	ksps
$t_{CONV(C)}$	Continuous mode conversion time(4)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(C)	Continuous mode throughput rate	f_{ADC} = 24 MHz		1500		ksps
$t_{CONV(FT)}$	Fast trigger mode conversion time(5)			$1*16/f_{ADC}$		µs
		f_{ADC} = 24 MHz		0.66		µs
TR(FT)	Fast trigger mode throughput rate(6)	f_{ADC} = 24 MHz	100		1200	ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev H and higher. Refer to *Table 5* for device rev identification in OTP memory and to *Section 8: Device marking*.
3. Value obtained from conversions started by trigger in single mode
4. All successive conversions in continuous and scan modes.
5. Conversion started by trigger when automatic clock gated mode enabled. Fast trigger mode is available only in devices with silicon Rev H and higher.
6. Value obtained from conversions started by fast trigger in single mode

10 Ordering information

Table 54. Ordering information scheme

Example: STR9 1 2 F A W 4 4 X 6 T

Family

ARM9 microcontroller family

Series

1 = STR9 series 1

Feature set

0 = CAN, UART, IrDA, I2C, SSP
1 = USB, CAN, UART, IrDA, I2C, SSP
2 = USB, CAN, UART, IrDA, I2C, SSP, ETHERNET

Memory type

F = Flash

Revision at product level

A = Revison A

No. of pins

M = 80
W = 128
Z = 144

SRAM size

3 = 64 Kbytes
4 = 96 Kbytes

Primary memory size

2 = 256 Kbytes 6= 1024 Kbytes
4 = 512 Kbytes 7= 2048 Kbytes

Package

X = plastic LQFP
H = LFBGA

Temperature range

6 = -40 to 85 °C

Shipping option

T = Tape and reel packing

1. For a list of available options (e.g. speed, package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.