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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str912faz46h6

Email: info@E-XFL.COM

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# 1 Description

STR91xFA is a series of ARM<sup>®</sup>-powered microcontrollers which combines a 16/32-bit ARM966E-S RISC processor core, dual-bank Flash memory, large SRAM for data or code, and a rich peripheral set to form an ideal embedded controller for a wide variety of applications such as point-of-sale terminals, industrial automation, security and surveillance, vending machines, communication gateways, serial protocol conversion, and medical equipment. The ARM966E-S core can perform single-cycle DSP instructions, good for speech processing, audio algorithms, and low-end imaging.



# 3 Functional overview

# 3.1 System-in-a-package (SiP)

The STR91xFA is a SiP device, comprised of two stacked die. One die is the ARM966E-S CPU with peripheral interfaces and analog functions, and the other die is the burst Flash. The two die are connected to each other by a custom high-speed 32-bit burst memory interface and a serial JTAG test/programming interface.

# 3.2 Package choice

STR91xFA devices are available in 128-pin (14 x 14 mm) and 80-pin (12 x 12 mm) LQFP and LFBGA144 (10 x 10 mm) packages. Refer to *Table 2: Device summary on page 11* for a list of available peripherals for each of the package choices.

# 3.3 ARM966E-S CPU core

The ARM966E-S core inherently has separate instruction and data memory interfaces (Harvard architecture), allowing the CPU to simultaneously fetch an instruction, and read or write a data item through two Tightly-Coupled Memory (TCM) interfaces as shown in *Figure 1*. The result is streamlined CPU Load and Store operations and a significant reduction in cycle count per instruction. In addition to this, a 5-stage pipeline is used to increase the amount of operational parallelism, giving the most performance out of each clock cycle.

Ten DSP-enhanced instruction extensions are supported by this core, including single-cycle execution of 32x16 Multiply-Accumulate, saturating addition/subtraction, and count leading-zeros.

The ARM966E-S core is binary compatible with 32-bit ARM7 code and 16-bit Thumb<sup>®</sup> code.

## 3.4 Burst Flash memory interface

A burst Flash memory interface (*Figure 1*) has been integrated into the Instruction TCM (I-TCM) path of the ARM966E-S core. Also in this path is an 8-instruction Pre-Fetch Queue (PFQ) and a 15-entry Branch Cache (BC), enabling the ARM966E-S core to perform up to 96 MIPS while executing code directly from Flash memory. This architecture provides high performance levels without a costly instruction SRAM, instruction cache, or external SDRAM. Eliminating the instruction cache also means interrupt latency is reduced and code execution becomes more deterministic.

## 3.4.1 Pre-fetch queue (PFQ)

As the CPU core accesses sequential instructions through the I-TCM, the PFQ always looks ahead and will pre-fetch instructions, taking advantage any idle bus cycles due to variable length instructions. The PFQ will fetch 32-bits at a time from the burst Flash memory at a rate of up to 96 MHz.



## 3.4.2 Branch cache (BC)

When instruction addresses are not sequential, such as a program branch situation, the PFQ would have to flush and reload which would cause the CPU to stall if no BC were present. Before reloading, the PFQ checks the BC to see if it contains the desired target branch address. The BC contains up to fifteen of the most recently taken branch addresses and the first eight instructions associated with each of these branches. This check is extremely fast, checking all fifteen BC entries simultaneously for a branch address match (cache hit). If there is a hit, the BC rapidly supplies the instruction and reduces the CPU stall. This gives the PFQ time to start pre-fetching again while the CPU consumes these eight instructions from the BC. The advantage here is that program loops (very common with embedded control applications) run very fast if the address of the loops are contained in the BC.

In addition, there is a 16th branch cache entry that is dedicated to the Vectored Interrupt Controller (VIC) to further reduce interrupt latency by eliminating the stall latency typically imposed by fetching the instruction that reads the interrupt vector address from the VIC.

## 3.4.3 Management of literals

Typical ARM architecture and compilers do not place literals (data constants) sequentially in Flash memory with the instructions that use them, but instead the literals are placed at some other address which looks like a program branch from the PFQ's point of view. The STR91xFA implementation of the ARM966E-S core has special circuitry to prevent flushing the PFQ when literals are encountered in program flow to keep performance at a maximum.



## **3.9** Vectored interrupt controller (VIC)

Interrupt management in the STR91xFA is implemented from daisy-chaining two standard ARM VIC units. This combined VIC has 32 prioritized interrupt request channels and generates two interrupt output signals to the CPU. The output signals are FIQ and IRQ, with FIQ having higher priority.

## 3.9.1 FIQ handling

FIQ (Fast Interrupt reQuest) is the only non-vectored interrupt and the CPU can execute an Interrupt Service Routine (ISR) directly without having to determine/prioritize the interrupt source, minimizing ISR latency. Typically only one interrupt source is assigned to FIQ. An FIQ interrupt has its own set of banked registers to minimize the time to make a context switch. Any of the 32 interrupt request input signals coming into the VIC can be assigned to FIQ.

## 3.9.2 IRQ handling

IRQ is a vectored interrupt and is the logical OR of all 32 interrupt request signals coming into the 32 IRQ channels. Priority of individual vectored interrupt requests is determined by hardware (IRQ channel Intr 0 is highest priority, IRQ channel Intr 31 is lowest).

However, inside the same VIC (primary or secondary VIC), CPU firmware may re-assign individual interrupt sources to individual hardware IRQ channels, meaning that firmware can effectively change interrupt priority levels as needed within the same VIC (from priority 0 to priority 16).

# Note: VIC0 (primary VIC) interrupts always have higher priority than VIC1 (secondary VIC) interrupts

When the IRQ signal is activated by an interrupt request, VIC hardware will resolve the IRQ interrupt priority, then the ISR reads the VIC to determine both the interrupt source and the vector address to jump to the service code.

The STR91xFA has a feature to reduce ISR response time for IRQ interrupts. Typically, it requires two memory accesses to read the interrupt vector address from the VIC, but the STR91xFA reduces this to a single access by adding a 16th entry in the instruction branch cache, dedicated for interrupts. This 16th cache entry always holds the instruction that reads the interrupt vector address from the VIC, eliminating one of the memory accesses typically required in traditional ARM implementations.

## 3.9.3 Interrupt sources

The 32 interrupt request signals coming into the VIC on 32 IRQ channels are from various sources; 5 from a wake-up unit and the remaining 27 come from internal sources on the STR91xFA such as on-chip peripherals, see *Table 6*. Optionally, firmware may force an interrupt on any IRQ channel.

One of the 5 interrupt requests generated by the wake-up unit (IRQ25 in *Table 6*) is derived from the logical OR of all 32 inputs to the wake-up unit. Any of these 32 inputs may be used to wake up the CPU and cause an interrupt. These 32 inputs consist of 30 external interrupts on selected and enabled GPIO pins, plus the RTC interrupt, and the USB Resume interrupt.



# 5.2 Default pin functions

During and just after reset, all pins on ports 0-9 default to high-impedance input mode until CPU firmware assigns other functions to the pins. This initial input mode routes all pins on ports 0-9 to be read as GPIO inputs as shown in the "Default Pin Function" column of *Table 8*. Simultaneously, certain port pin signals are also routed to other functional inputs as shown in the "Default Input Function" column of *Table 8*, and these pin input functions will remain until CPU firmware makes other assignments. At any time, even after the CPU assigns pins to alternate functions, the CPU may always read the state of any pin on ports 0-9 as a GPIO input. CPU firmware may assign alternate functions to port pins as shown in columns "Alternate Input 1" or "Alternate Output 1, 2, 3" of *Table 8* by writing to control registers at run-time.

#### 5.2.1 General notes on pin usage

- Since there are no internal or programmable pull-up resistors on ports 0-9, it is advised to pull down to ground, or pull up to VDDQ (using max. 47 KΩ resistors), all unused pins on port 0-9. Another solution is to use the GPIO control registers to configure the unused pins on ports 0-9 as output low level. The purpose of this is to reduce noise susceptibility, noise generation, and minimize power consumption
- 2 All pins on ports 0 9 are 5V tolerant
- *3* Pins on ports 0,1,2,4,5,7,8,9 have 4 mA drive and 4mA sink. Ports 3 and 6 have 8 mA drive and 8 mA sink.
- 4 For 8-bit non-muxed EMI operation: Port 8 is eight bits of data, ports 7 and 9 are 16 bits of address.
- 5 For 16-bit muxed EMI operation: Ports 8 and 9 are 16 bits of muxed address and data bits, port 7 is up to eight additional bits of high-order address
- 6 Signal polarity is programmable for interrupt request inputs, EMI\_ALE, timer input capture inputs and output compare/PWM outputs, motor control tach and emergency stop inputs, and motor control phase outputs.
- 7 HiZ = High Impedance, V = Voltage Source, G = Ground, I/O = Input/Output
- 8 STR910FA devices do not support USB. On these devices USBDP and USBDN signals are "Not Used" (USBDN is not connected, USBDP must be pulled up by a 1.5K ohm resistor to VDDQ), and all functions named "USB" are not available.
- 9 STR910FA 128-pin and 144-ball devices do not support Ethernet. On these devices PHYCLK and all functions named "MII\*" are not available.



DTURMORY SPACE         Array           0xFFFFFFFF         VC0         VC1         4 KB           0xFFFFFFFF         VC1         4 KB         Array           0xF000.0000         VC1         4 KB         Array           0xF000.0000         VC1         4 KB         Array           0xF000.0000         ENET         6 KB         Array           0xF000.0000         ENET         Array         Array			-	APB BASE +	PERIPHERAL BUS MEMORY SPACE	
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Bit PERCE         Area	0xFFFF.FFFF			APB1+0x0000.D000	I2C1	4 KB
NECON 0000         NELLYVED         6H KB         FEFREED         APB1+00000.8000         WATCHDOG         4KB           0xF000.0000         FKB         6H KB         APB1+00000.8000         SSP1         4KB           APB1+00000.0000         SSP1         4KB         APB1+00000.8000         SSP1         4KB           APB1+00000.0000         SSP1         4KB         APB1+00000.8000         SSP1         4KB           APB1+00000.0000         SSP1         4KB         APB1+00000.0000         APB1+00000.00000 </td <td>0xFFFF.F000</td> <td></td> <td>AHB</td> <td>APB1+0x0000.C000</td> <td>I2C0</td> <td>4 KB</td>	0xFFFF.F000		AHB	APB1+0x0000.C000	I2C0	4 KB
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0x6800.0000         8-CH DMA         64 MB         AHB         APB+0x0000.0000         APB+0x0000.0000         APB           0x6000.0000         USB         64 MB         PERIPHERAL BUS, AHB         APB0+0x03FF.FFF         APB0+0x0001.0000         GPIO PORT P9         4 KB           0x5000.0000         APB1         64 MB         PERIPHERAL BUS, AHB         AAB0+0x0001.6000         GPIO PORT P9         4 KB           0x5000.0000         FMI         64 MB         PERIPHERAL BUS, AHB         APB0+0x0000.6000         GPIO PORT P4         4 KB           0x5000.0000         SRAM, AHB         64 MB         PERIPHERAL BUS, AHB         PERIPHERAL BUS, APB0+0x0000.0000         GPIO PORT P4         4 KB           0x4000.0000         GPIO         FMI         64 MB         PERIPHERAL BUS, AHB         APB0+0x0000.0000         GPIO PORT P4         4 KB           0x4000.0000         FMI         64 MB         PERIPHERAL BUS, AHB         APB0+0x0000.0000         GPIO PORT P4         4 KB           0x3000.0000         Ext. MEM, CS2         64 MB         AHB         AHB         APB0+0x0000.0000         GPIO PORT P4         4 KB           0x2400.0000         Ext. MEM, CS2         64 MB         AHB         AHB         APB0+0x0000.0000         TIM2         4 KB <t< td=""><td>0x6C00.0000</td><td>ENET</td><td>64 MB</td><td>APB1+0x0000.1000</td><td>APB1 CONFIG</td><td>4 КВ</td></t<>	0x6C00.0000	ENET	64 MB	APB1+0x0000.1000	APB1 CONFIG	4 КВ
Dx84400.0000         EMI         64 M8         PERIPHERAL BUS, NON. BUFFERED         APB0+0x001.0000         RESERVED           0x5000.0000         APB0         64 M8         APB0+0x001.0000         GPIO PORT P8         4 K8           0x5000.0000         APB0         64 M8         APB0+0x000.0000         GPIO PORT P8         4 K8           0x5000.0000         APB0         64 M8         BUFFERED         APB0+0x000.0000         GPIO PORT P8         4 K8           0x4000.0000         APB0         64 M8         BUFFERED         APB0+0x0000.0000         GPIO PORT P4         4 K8           0x4000.0000         FMI         64 M8         BUFFERED         APB0+0x0000.0000         GPIO PORT P3         4 K8           0x4000.0000         FMI         64 M8         BUFFERED         APB0+0x0000.0000         GPIO PORT P1         4 K8           0x4000.0000         Ext. MEM, CS1         64 M8         AHB         APB0+0x0000.0000         GPIO PORT P1         4 K8           0x3000.0000         Ext. MEM, CS3         64 M8         AHB         APB0+0x0000.0000         TIM1         4 K8           0x3000.0000         Ext. MEM, CS3         64 M8         AHB         APB0+0x0000.0000         TIM1         4 K8               0x2000.0000             Ext. MEM, C	0x6800.0000	8-CH DMA	64 MB ( AHB	APB1+0x0000.0000		<b>J</b> ,
Oxf6000.0000         USB         64 MB         PERIPHERAL BUS, NON-BUFFERED         APB0+0x0001.0000         RESERVED         4 KB           0x5000.0000         APB0         64 MB         PERIPHERAL BUS, NON-BUFFERED         APB0+0x0000.F000         GPIO PORT PS         4 KB           0x5000.0000         FMI         64 MB         BUFFERED         APB0+0x0000.0000         GPIO PORT PF         4 KB           0x5000.0000         APB1         64 MB         BUFFERED         APB0+0x0000.0000         GPIO PORT PF         4 KB           0x5000.0000         APB1         64 MB         BUFFERED         APB0+0x0000.0000         GPIO PORT PF         4 KB           0x4000.0000         FMI         64 MB         PERIPHERAL BUS, BUFFERED         APB0+0x0000.0000         GPIO PORT PF         4 KB           0x4000.0000         FMI         64 MB         AHB         APB0+0x0000.0000         GPIO PORT PF         4 KB           0x4000.0000         Ext. MEM, CS1         64 MB         AHB         APB0+0x0000.0000         TIM2         4 KB           0x2000.0000         Ext. MEM, CS2         64 MB         AHB         APB0+0x0000.0000         TIM2         4 KB           0x2000.0000         Ext. MEM, CS2         64 MB         AHB         APB0+0x0000.0000         TIM2	0x6400.0000	EMI	64 MB	APB0+0x03FF.FFFF	-	
Ox5C00.0000         APB1         64 MB         PERIPHERAL BUS, NON-BUFFRED         APB0+0x0000_F00_0         GPIO PORT P9         4 KB           0x5600.0000         FMI         64 MB         BUFFERED         APB0+0x0000_E00_0         GPIO PORT P8         4 KB           0x5000.0000         SRAM, AHB         64 MB         PERIPHERAL BUS, BUFFERED         APB0+0x0000_E00_0         GPIO PORT P6         4 KB           0x4000.0000         APB0         64 MB         PERIPHERAL BUS, BUFFERED         APB0+0x0000_C000_0         GPIO PORT P4         4 KB           0x4000.0000         APB0         64 MB         PERIPHERAL BUS, BUFFERED         APB0+0x0000_R000_0         GPIO PORT P4         4 KB           0x4000.0000         FMI         64 MB         AHB         APB0+0x0000_R000_0         GPIO PORT P4         4 KB           0x4000.0000         EXt. MEM, CS1         64 MB         AHB         AHB         APB0+0x0000_R000_0         GPIO PORT P1         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         AHB         AHB         APB0+0x0000_R000_0         GPIO PORT P1         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         AHB         AHB         APB0+0x0000_R000_0         TIM1         4 KB           0x2000.00000         E	0x6000.0000	USB	64 MB	APB0+0x0001.0000	RESERVED	
Ox5800.0000         APB0         64 MB         ACCESS ALB         APB0+0x000.E000         GPIO PORT PB         4 KB           0x500.0000         FMI         64 MB         BUFFERED         APB0+0x000.E000         GPIO PORT P5         4 KB           0x500.0000         APB1         64 MB         PERIPHERALBUS, AHB         APB0+0x000.0000         GPIO PORT P5         4 KB           0x400.0000         APB0         64 MB         PERIPHERALBUS, AHB         APB0+0x000.0000         GPIO PORT P5         4 KB           0x400.0000         FMI         64 MB         BUFFERED         APB0+0x000.0000         GPIO PORT P2         4 KB           0x400.0000         FMI         64 MB         PERIPHERALBUS, AHB         APB0+0x0000.0000         GPIO PORT P2         4 KB           0x4400.0000         Ext. MEM, CS1         64 MB         AHB         AHB         APB0+0x0000.0000         GPIO PORT P1         4 KB           0x300.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.0000         TIM3         4 KB           0x300.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.0000         TIM4         4 KB           0x300.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.0000         TIM0 <td>0x5C00.0000</td> <td>APB1</td> <td>64 MB PERIPHERAL BUS,</td> <td>APB0+0x0000.F000</td> <td>GPIO PORT P9</td> <td>4 KB</td>	0x5C00.0000	APB1	64 MB PERIPHERAL BUS,	APB0+0x0000.F000	GPIO PORT P9	4 KB
UNAPE         OK         UNAPE         OK         <	0x5800.0000	APB0	64 MB ( AHB ACCESS	APB0+0x0000.E000	GPIO PORT P8	4 KB
October         SRAM, AHB         64 MB         PERIPHERAL BUS, BUFFERED         AFBd+0x0000_CO00         GPIO PORT P6         4 KB           0x400.0000         APB0         64 MB         PERIPHERAL BUS, BUFFERED         AFBd+0x0000_CO00         GPIO PORT P4         4 KB           0x400.0000         FMI         64 MB         BUFFERED         AFB         APBd+0x0000_CO00         GPIO PORT P4         4 KB           0x400.0000         FMI         64 MB         BUFFERED         APBd+0x0000_C000         GPIO PORT P4         4 KB           0x400.0000         Ext. MEM, CS0         64 MB         AHB         APBd+0x0000_6000         GPIO PORT P4         4 KB           0x3000.0000         Ext. MEM, CS2         64 MB         AHB         APBd+0x0000_6000         TIM2         4 KB           0x3000.0000         Ext. MEM, CS3         64 MB         AHB         APBd+0x0000_2000         TIM2         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         AHB         APBd+0x0000_2000         TIM2         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         AHB         APBd+0x0000_2000         TIM4         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         AHB         APBd+0x0000_2000         TIM0	0x5400 0000	FMI	64 MB (BUFFERED		GPIO PORT P7	4 KB
CM-CO0.0000       APB1       64 MB       PERIPHERAL BUS, BUFFRED ACCESS       APB0+0x0000.8000       GPIO PORT P5       4 KB       4 KB         CM-C00.0000       FMI       64 MB       B4 MB       BUFFRED       APB0+0x0000.8000       GPIO PORT P4       4 KB         CM-C00.0000       FMI       64 MB       B4 MB       BUFFRED       APB0+0x0000.8000       GPIO PORT P3       4 KB         CM-C00.0000       FMI       64 MB       B4 MB       BUFFRED       APB0+0x0000.8000       GPIO PORT P4       4 KB         CM-C00.0000       Ext. MEM, CS1       64 MB       AHB       APB0+0x0000.8000       GPIO PORT P4       4 KB         CM-C00.0000       Ext. MEM, CS2       64 MB       AHB       APB0+0x0000.8000       GPIO PORT P4       4 KB         CM-C00.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.8000       TIM3       4 KB         CM-C00.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.2000       TIM4       4 KB         CM-C00.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.2000       TIM0       4 KB         CM-C00.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         Dx2400.00000 </td <td>0×5000.0000</td> <td>SRAM, AHB</td> <td>64 MB</td> <td>APB0+0×0000 C000</td> <td>GPIO PORT P6</td> <td>4 KB</td>	0×5000.0000	SRAM, AHB	64 MB	APB0+0×0000 C000	GPIO PORT P6	4 KB
Ox4800.0000         APB0         64 MB         BUFFERED ACCESS         APB0+0x0000_000         GPI0 PORT P4         4 KB           0x4800.0000         FMI         64 MB         BUFFERED         APB0+0x000.000         GPI0 PORT P3         4 KB           0x400.0000         SRAM, AHB         64 MB         BUFFERED         APB0+0x000.000         GPI0 PORT P1         4 KB           0x400.0000         Ext. MEM, CS0         64 MB         AHB         APB0+0x000.000         GPI0 PORT P1         4 KB           0x300.0000         Ext. MEM, CS1         64 MB         AHB         APB0+0x000.000         GPI0 PORT P1         4 KB           0x300.0000         Ext. MEM, CS2         64 MB         AHB         APB0+0x000.000         GPI0 PORT P1         4 KB           0x3000.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x000.000         TIM3         4 KB           0x2000.0000         Ext. MEM, CS1         64 MB         AHB         APB0+0x000.0000         TIM1         4 KB           0x2000.0000         Ext. MEM, CS2         64 MB         AHB         APB0+0x000.0000         TIM1         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x000.0000         TIM1         4 KB <tr< td=""><td>0x4C00.0000</td><td>APB1</td><td>64 MB PERIPHERAL BUS.</td><td>APB0+0×0000 B000</td><td>GPIO PORT P5</td><td>4 KB</td></tr<>	0x4C00.0000	APB1	64 MB PERIPHERAL BUS.	APB0+0×0000 B000	GPIO PORT P5	4 KB
MARDON 00000         FMI         64 MB         BUFFERED         APB010000000         GPIO PORT P3         4 KB           0x44000.0000         SRAM, AHB         64 MB         AHB         APB0+0x0000.8000         GPIO PORT P2         4 KB           0x3600.0000         Ext. MEM, CS1         64 MB         AHB         APB0+0x0000.6000         GPIO PORT P1         4 KB           0x3800.0000         Ext. MEM, CS2         64 MB         AHB         APB0+0x0000.5000         GPIO PORT P0         4 KB           0x3800.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.5000         TIM3         4 KB           0x3800.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.0000         TIM2         4 KB           0x2800.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.0000         TIM1         4 KB           0x2400.0000         Ext. MEM, CS3         64 MB         AHB         AHB         APB0+0x0000.0000         TIM0         4 KB           0x2400.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.0000         TIM0         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         AHB         APB0+0x0000.0000         TIM0         4 KB	0×4800.0000	APB0	64 MB BUFFERED ACCESS	ABB0+0×0000 A000	GPIO PORT P4	4 KB
0x4400.0000       SRAM, AHB       64 MB       AHB         0x4000.0000       Ext. MEM, CS0       64 MB       AHB         0x300.0000       Ext. MEM, CS1       64 MB       AHB         0x300.0000       Ext. MEM, CS2       64 MB       AHB         0x300.0000       Ext. MEM, CS2       64 MB       AHB         0x300.0000       Ext. MEM, CS3       64 MB       AHB         0x300.0000       Ext. MEM, CS3       64 MB       AHB         0x200.0000       Ext. MEM, CS1       64 MB       AHB         0x200.0000       Ext. MEM, CS1       64 MB       AHB         0x200.0000       Ext. MEM, CS2       64 MB       AHB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB         0x2000.0000       FLASH, IARC       GHA       GHA         0x2000.0000       FLASH, IARC       GHA       GHA         0x2000.0000       SRAM, D-TCM       Using 64 KB or 96	0x4800.0000	FMI	64 MB BUFFERED		GPIO PORT P3	4 KB APB0.
0x4000.0000       Ext. MEM, CS0       64 MB       AHB       AHB       APB0+0x000.3000       GPIO PORT P1       4 KB       4 KB         0x3000.0000       Ext. MEM, CS1       64 MB       AHB       APB0+0x000.7000       GPIO PORT P1       4 KB         0x3000.0000       Ext. MEM, CS2       64 MB       AHB       BUFFERED       APB0+0x000.3000       TIM3       4 KB         0x3000.0000       Ext. MEM, CS3       64 MB       BUFFERED       AHB       APB0+0x000.3000       TIM1       4 KB         0x2000.0000       Ext. MEM, CS1       64 MB       AHB       AHB       APB0+0x000.3000       TIM1       4 KB         0x2000.0000       Ext. MEM, CS2       64 MB       AHB       AHB       APB0+0x000.0000       TIM1       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       AHB       AFB0+0x0000.0000       APB0 +0x0000.0000       AFB0+0x0000.0000       AFB0+0x0000.0000       AFB0+0x0000.0000       AFB0+0x0000.0000       AFB0+0x000.0000       AFB0+0x000.0000       AFB0+0x000.0000       AFB0+0x000.0000       AFB0+0x000.0000       AFB0+0x000.0000       AFB0+0x000.00000       AFB0+0x0000.0000	0x4400.0000	SRAM, AHB	64 MB	APB0+0x0000.9000	GPIO PORT P2	4 KB
0x3800.0000       Ext. MEM, CS1       64 MB       AHB       AHB       APB0+0x0000.6000       GPIO PORT P0       4 KB         0x3000.0000       Ext. MEM, CS2       64 MB       AHB       APB0+0x0000.6000       TIM3       4 KB         0x3000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.6000       TIM2       4 KB         0x2000.0000       Ext. MEM, CS1       64 MB       AHB       APB0+0x0000.3000       TIM1       4 KB         0x2800.0000       Ext. MEM, CS2       64 MB       AHB       APB0+0x0000.2000       TIM0       4 KB         0x2400.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       AHB       APB	0x4000.0000	Ext. MEM, CS0	64 MB	APB0+0x0000.80000	GPIO PORT P1	4 KB Bridge
0x300.0000       Ext. MEM, CS2       64 MB       APB0+0x0000.5000       TIM3       4 KB         0x300.0000       Ext. MEM, CS3       64 MB       APB0+0x0000.5000       TIM2       4 KB         0x200.0000       Ext. MEM, CS1       64 MB       APB0+0x0000.0000       TIM1       4 KB         0x200.0000       Ext. MEM, CS2       64 MB       APB0+0x0000.0000       TIM1       4 KB         0x200.0000       Ext. MEM, CS2       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2400.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2400.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       APB0+0x0000.0000       APB0 +0x0000.0000       APB0 +0x0000.	0x3000.0000	Ext. MEM, CS1	64 MB ( AHB	APB0+0x0000.7000	GPIO PORT P0	4 KB
0x3400.0000       Ext. MEM, CS3       64 MB       APB0+0x0000.0000       TIM2       4 KB         0x2000.0000       Ext. MEM, CS1       64 MB       APB0+0x0000.3000       TIM1       4 KB         0x2000.0000       Ext. MEM, CS2       64 MB       AHB       APB0+0x0000.2000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.2000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       APB0+0x0000.0000       APB0+0x0000.0000       APB0+0x0000.0000         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       AHB       APB0+0x0000.0000       AP	0x3400.0000	Ext. MEM, CS2	64 MB BUFFERED		TIM3	4 KB
0x3000.0000       Ext. MEM, CS0       64 MB       AHB       APB0+0x0000.3000       TIM1       4 KB         0x2000.0000       Ext. MEM, CS2       64 MB       AHB       APB0+0x0000.2000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       AHB       APB0+0x0000.0000       AP	0x3400.0000	Ext. MEM, CS3	64 MB	APB0+0x0000.5000	TIM2	4 KB
0x2200.0000       Ext. MEM, CS1       64 MB       AHB       AHB       AHB       APB0+0x0000.3000       TIM0       4 KB         0x2400.0000       Ext. MEM, CS2       64 MB       AHB       BUFFERED       APB0+0x0000.2000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       Gamma       APB0+0x0000.0000       TIM0       4 KB         0x2000.0000       Ext. MEM, CS3       64 MB       Order of the two Flash memories is user defined.         0x2000.0000       RESERVED       Using 64 KB or 96       SECONDARY       MAIN FLASH         0x0800.0000       SRAM, D-TCM       Using 64 KB or 96       MAIN FLASH       MAIN FLASH         0x0000.0000       FLASH, I-TCM       Using 288 KB, 544 KB,       0x0000.0000       SECONDARY         1.1 MB or 2.1 MB       0x0000.0000       DEFAULT ORDER       OPTIONAL ORDER	0x3000.0000	Ext. MEM, CS0	64 MB	APB0+0x0000.4000	TIM1	4 KB
0x2800.0000       Ext. MEM, CS2       64 MB       AHB       APB0+0x0000.2000         0x2000.0000       Ext. MEM, CS3       64 MB       BUFFERED       APB0+0x0000.1000       APB0 CONFIG         0x2000.0000       Ext. MEM, CS3       64 MB       G4 MB       G4 MB       G4 MB       APB0+0x0000.0000         0x2000.0000       Ext. MEM, CS3       G4 MB       G4 MB       G4 MB       G4 MB       G4 MB         0x2000.0000       Ext. MEM, CS3       G4 MB       G4 MB       G4 MB       G4 MB       G4 MB         0x2000.0000       Ext. MEM, CS3       G4 MB	0x2C00.0000	Ext. MEM. CS1	64 MB	APB0+0x0000.3000	TIMO	4 KB
0x2400.0000         Ext. MEM, CS3         64 MB         APB0+0x0000.1000         APB0 CONFIG         4 KB           0x2000.0000         Ext. MEM, CS3         64 MB         Order of the two Flash memories is user defined.         APB0 CONFIG         4 KB           0x0800.0000         RESERVED         Using 64 KB or 96         SECONDARY         MAIN FLASH         (BANK 0),         256KB, 512KB,         1024KB or 2048KB         1024KB or 2048KB         SECONDARY         FLASH, (BANK 1),         32KB or 128KB         SECONDARY         FLASH, (BANK 1),         SECONDARY         SECONDARY         FLASH, (BANK 1),         SECONDARY         SECONDARY         SECONDARY         SECONDARY <td>0x2800.0000</td> <td>Ext. MEM. CS2</td> <td>AHB GA MR (BUFFERED</td> <td>APB0+0x0000.2000</td> <td>WAKE-UP UNIT</td> <td>4 KB</td>	0x2800.0000	Ext. MEM. CS2	AHB GA MR (BUFFERED	APB0+0x0000.2000	WAKE-UP UNIT	4 KB
0x2000.0000         Extended with the product of the second decision of the second decis of the second decision of the second decis of the second decis	0x2400.0000	Ext MEM CS3		APB0+0x0000.1000	APB0 CONFIG	4 KB
Ox0800.0000 0x0400.0000SRAM, D-TCM FLASH, I-TCMUsing 64 KB or 96 KB Using 288 KB, 544 KB, 1.1 MB or 2.1 MBOx0000.0000 0x0000.0000Order of the two Flash memories is user defined.Dx0800.0000 Dx0400.0000SRAM, D-TCM FLASH, I-TCMUsing 64 KB or 96 KB 1.1 MB or 2.1 MBMAIN FLASH (BANK 0), 256KB, 512KB, 1024KB or 2028KBMAIN FLASH (BANK 0), 256KB, 512KB, 1024KB or 2028KBDEFAULT ORDEROPTIONAL ORDER	0x2000.0000	EXI. IVIEIVI, CSS	64 MB 🦯	APB0+0x0000.0000	AFB0 CONFIG	4 KB /
0x0800.0000     SRAM, D-TCM     Using 64 KB or 96     SECONDARY     SECONDARY       0x0000.0000     SRAM, D-TCM     Using 64 KB or 96     SECONDARY     SECONDARY       0x0000.0000     FLASH, I-TCM     Using 288 KB, 544 KB, 1.1 MB or 2.1 MB     0x0000.0000     DEFAULT ORDER     OPTIONAL ORDER				Order of the two Flock we		
RESERVED         Using 64 KB or 96 KB 0x0000.0000         Using 64 KB or 96 KB 0x0000.0000         MAIN FLASH (BANK 1), 32KB or 128KB         MAIN FLASH (BANK 0), 256KB, 512KB, 1024KB or 2028KB           0x0000.0000         SRAM, D-TCM FLASH, I-TCM         Using 64 KB or 96 KB 1.1 MB or 2.1 MB         MAIN FLASH (BANK 0), 256KB, 512KB, 1024KB or 2028KB         SECONDARY FLASH (BANK 1), 32KB or 128KB           0x0000.0000         FLASH, I-TCM         Using 288 KB, 544 KB, 1.1 MB or 2.1 MB         DEFAULT ORDER         OPTIONAL ORDER						1
0x0800.0000         SRAM, D-TCM         Using 64 KB or 96         MAIN FLASH         (BANK 0), 256KB, 512KB, 1024KB or 2048KB           0x0000.0000         FLASH, I-TCM         Using 288 KB, 544 KB, 1.1 MB or 2.1 MB         0x0000.0000         DEFAULT ORDER         OPTIONAL ORDER		RESERVED		FLASH (BANK 1),	MAIN FLASH	
0x0800.0000         SRAM, D-TCM         Using 64 KB or 96         MAIN FLASH         1024KB or 2048KB           0x0400.0000         SRAM, D-TCM         Using 288 KB, 544 KB,         256KB, 512KB,         1024KB or 2028KB           0x0000.0000         FLASH, I-TCM         Using 288 KB, 544 KB,         0x0000.0000         DEFAULT ORDER         OPTIONAL ORDER				32KB or 128KB	(BANK 0), 256KB 512KB	
0x0800.0000         SRAM, D-TCM         Using 64 KB or 96         (BANK 0), 256KB, 512KB, 1024KB or 2028KB         SECONDARY           0x0000.0000         FLASH, I-TCM         Using 288 KB, 544 KB, 1.1 MB or 2.1 MB         0x0000.0000         DEFAULT ORDER         OPTIONAL ORDER				MAIN FLASH	1024KB or 2048KB	
0x0400.0000         SRAM, D-TCM         Using 48 KB or 96 KB         256KB, 512KB, 1024KB or 2028KB         FLASH, I-TCM           0x0000.0000         FLASH, I-TCM         Using 288 KB, 544 KB, 1.1 MB or 2.1 MB         0x0000.0000         DEFAULT ORDER         FLASH (BANK 1), 32KB or 128KB           DEFAULT ORDER         OPTIONAL ORDER         OPTIONAL ORDER	0x0800.0000			(BANK 0),	SECONDARY	
0x0000.0000 FLASH, I-TCM Using 288 KB, 544 KB, 1.1 MB or 2.1 MB 0x0000.0000 DEFAULT ORDER OPTIONAL ORDER	0x0400.0000 _	SRAM, D-TCM	Using 64 KB or 96 KB	256KB, 512KB,	FLASH (BANK 1),	
DEFAULT ORDER OPTIONAL ORDER	0x0000.0000	FLASH, I-TCM	Using 288 KB, 544 KB, 1.1 MB or 2.1 MB 0x0000.0000	UZ4ND UI ZUZOND	32KB or 128KB	
				DEFAULT ORDER	OPTIONAL ORDER	

#### Figure 9. STR91xFA memory map



	Parameter	Test conditions	Typ <sup>(1)</sup>	Typ after 100K W/E cycles <sup>(1)</sup>	Max	Unit
	Primary bank (2 Mbytes)		32	36	46	S
Bank erase	Primary bank (1 Mbytes)		16	18	23	s
	Secondary bank (128 Kbytes)		2.5	3	4	s
Sector erase	Of primary bank (64 Kbytes)		1300	1400	1800	ms
	Of secondary bank (16 Kbytes)		500	600	850	ms
	Primary bank (2 Mbytes)		15	20	22	s
Bank program	Primary bank (1 Mbytes)		7.5	10	11	s
	Secondary bank (128 Kbytes)		1060	1140	1380	ms
Soctor program	Of primary bank (64 Kbytes)		500	520	640	ms
Sector program	Of secondary bank (16 Kbytes)		120	130	160	ms
Word program		Half word (16 bits)	8	9	11	μs

Table 25. Flash memory program/erase characteristics (Flash size = 1 MB / 2 MB)

1.  $V_{DD}$  = 1.8 V,  $V_{DDQ}$  = 3.3 V,  $T_A$  = 2 5°C.

#### Table 26. Flash memory endurance

Paramotor	Tost conditions	Value			Unit
Falameter	Test conditions	Min	Тур	Мах	Onit
Program/erase cycles	Per word	100K			cycles
Data retention		20			years



# 7.9 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

## 7.9.1 Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V<sub>DD</sub>, V<sub>DDQ</sub> and V<sub>SS</sub> through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Symbol	Parameter	Conditions	Severity/ Criteria <sup>(1)</sup>	Unit
V <sub>FESD</sub>	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD}$ = 1.8 V, $V_{DDQ}$ = 3.3 V, $T_A$ = +25 °C, $f_{OSC}/f_{CPUCLK}$ = 4 MHz/96 MHz PLL	1B	
V <sub>FFTB</sub>	Fast transient voltage burst limits to be applied through 100pF on $V_{DD}$ and $V_{DDQ}$ pins to induce a functional disturbance	$V_{DD}$ =1.8 V, $V_{DDQ}$ = 3.3 V, $T_A$ = +25 °C, f <sub>OSC</sub> /f <sub>CPUCLK</sub> = 4 MHz/96 MHz PLL conforms to IEC 1000-4-4	4A	kV

Table 27. EMS data

1. Data based on characterization results, not tested in production.



## 7.9.2 Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Symbol	Paramotor	Parameter Conditions	Monitored	Max vs. [fosc/fcpuclk]		Unit
Symbol	i arameter		Frequency Band	24 MHz / 48 MHz <sup>(1)</sup>	24 MHz / 96 MHz <sup>(1)</sup>	Unit
S <sub>EMI</sub> Peak le		Peak level $V_{DDQ} = 3.3 \text{ V}, V_{DD} = 1.8 \text{ V}, T_A = +25 ^{\circ}\text{C}, LQFP128 \text{ package}^{(2)} \text{ conforming to SAE J} 1752/3$	0.1 MHz to 30 MHz	14	10	
	Peak level		30 MHz to 130 MHz	18	19	dBμV
			130 MHz to 1GHz	18	22	
			SAE EMI Level	4	4	-

Table	28.	EMI	data
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1. Data based on characterization results, not tested in production.

2. BGA and LQFP devices have similar EMI characteristics.

## 7.9.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

## 7.9.4 Electro-static discharge (ESD)

Electro-Static Discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts\*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electro-static discharge voltage (Human Body Model)	$T_A = +25^{\circ}C$ conforming to JESD22-A114	2	+/-2000	V
V <sub>ESD(CDM)</sub>	Electro-static discharge voltage (Charged Device Model)	$T_A = +25^{\circ}C$ conforming to JESD22-C101	Ш	1000	v

1. Data based on characterization results, not tested in production.



#### 7.9.5 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

#### 7.9.6 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

## 7.9.7 Electrical sensitivity

#### Table 30. Static latch-up data

Symbol	Parameter	Conditions	Class <sup>(1)</sup>
LU	Static latch-up class	$T_A = +25 \ ^{\circ}C$ conforming to JESD78A	II class A

 Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).



### Mux write



#### Table 35. Mux write times

Symbol	Parameter	Value			
Cymbol	i di difictei	Min	Мах		
t <sub>WCR</sub>	WRn to CSn inactive	(t <sub>BCLK</sub> /2) - 2ns	(t <sub>BCLK</sub> /2) + 2ns		
t <sub>WAS</sub>	Write address setup time	(WSTWEN + 1/2) x t <sub>BCLK</sub> - 2.5 ns	(WSTWEN + 1/2) x t <sub>BCLK</sub> + 2 ns		
t <sub>WDS</sub>	Write data setup time	((WSTWEN - ALE_LENGTH) x t <sub>BCLK</sub> ) - 2 ns	((WSTWEN - ALE_LENGTH) x t <sub>BCLK</sub> ) + 1 ns		
t <sub>WP</sub>	Write pulse width	((WSTWR-WSTWEN + 1) x t <sub>BCLK</sub> ) - 1 ns	((WSTWR-WSTWEN + 1) x t <sub>BCLK)</sub> + 1.5 ns		
t <sub>AW</sub>	ALE pulse width	(ALE_LENGTH x t <sub>BCLK</sub> )- 3.5 ns	(ALE_LENGTH x t <sub>BCLK</sub> )		
t <sub>AAS</sub>	Address to ALE setup time	(ALE_LENGTH x t <sub>BCLK</sub> )- 3.5 ns	(ALE_LENGTH x t <sub>BCLK</sub> )		
t <sub>AAH</sub>	Address to ALE hold time	(t <sub>BCLK</sub> /2) - 1 ns	(t <sub>BCLK</sub> /2) + 2 ns		



# 7.11.2 Synchronous mode

# Sync burst write



Figure 23. Sync burst write diagram



	-		-	
Symbol	Parameter	Value		
Symbol	Falameter	Min	Мах	
t <sub>D1BAA</sub>	BAA t <sub>D1</sub>	0	2 ns	
t <sub>D2BAA</sub>	BAA t <sub>D2</sub>	0.5 ns	2.5 ns	
t <sub>D1ALE</sub>	ALE t <sub>D1</sub>	1 ns	3.5 ns	
t <sub>D2ALE</sub>	ALE t <sub>D2</sub>	(t <sub>BCLK</sub> /2) -0.5 ns	(t <sub>BCLK</sub> /2) + 3.5 ns	
t <sub>D1WR</sub>	RD t <sub>D1</sub>	0	2ns	
t <sub>D2WR</sub>	RD t <sub>D2</sub>	0.5 ns	2.5 ns	
t <sub>D1A</sub>	Address t <sub>D1</sub>	1.5 ns	4 ns	
t <sub>D2A</sub>	Address t <sub>D2</sub>	2ns	4.5 ns	
t <sub>D1CS</sub>	CS t <sub>D1</sub>	0.5ns	3 ns	
t <sub>D2CS</sub>	CS t <sub>D2</sub>	1 ns	3.5 ns	
t <sub>WS</sub>	WAIT setup time	3 ns	6 ns	
t <sub>DS</sub>	Data setup time	(t <sub>BCLK</sub> /2) -3.5 ns	(t <sub>BCLK</sub> /2)+ 0.5 ns	
t <sub>DH</sub>	Data hold time	(t <sub>BCLK</sub> /2) - 1 ns	(t <sub>BCLK</sub> /2)+3.5 ns	

Table	38	Sync	burst	write	times
lable	50.	Sync	Duisi	WIILE	umes



#### Sync burst read



Figure 24. Sync burst read diagram

Table 39. Sync burst read time	Table	39.	Sync	burst	read	times
--------------------------------	-------	-----	------	-------	------	-------

Symbol	Peremeter	Value		
Symbol	Farameter	Min	Мах	
t <sub>D1BAA</sub>	BAA t <sub>D1</sub>	0 ns	2 ns	
t <sub>D2BAA</sub>	BAA t <sub>D2</sub>	0.5ns	2.5 ns	
t <sub>D1ALE</sub>	ALE t <sub>D1</sub>	1 ns	3.5 ns	
t <sub>D2ALE</sub>	ALE t <sub>D2</sub>	(t <sub>BCLK</sub> /2)+0.5 ns	(t <sub>BCLK</sub> /2)+3 ns	
t <sub>D1RD</sub>	RD t <sub>D1</sub>	0	2 ns	
t <sub>D2RD</sub>	RD t <sub>D2</sub>	0.5 ns	2.5 ns	
t <sub>D1A</sub>	Address t <sub>D1</sub>	2 ns	4 ns	
t <sub>D2A</sub>	Address t <sub>D2</sub>	2.5 ns	3.5 ns	
t <sub>D1CS</sub>	CS t <sub>D1</sub>	0.5 ns	3 ns	
t <sub>D2CS</sub>	CS t <sub>D2</sub>	1 ns	3.5 ns	
t <sub>WS</sub>	WAIT set up time	1 ns	4 ns	
t <sub>DS</sub>	Data setup time	4.5 ns	-	
t <sub>DH</sub>	Data hold time	0	-	





Figure 31. SPI slave timing diagram with CPHA = 1







#### Marking of engineering samples for LQFP80

The following figure shows the engineering sample marking for the LQFP80 package. Only the information field containing the engineering sample marking is shown



Figure 42. LQFP80 package top view

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



# 9.1 ECOPACK

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions, and product status are available at <u>www.st.com</u>.

# 9.2 Thermal characteristics

The average chip-junction temperature,  $T_J$  must never exceed 125 °C.

The average chip-junction temperature,  $T_J$ , in degrees Celsius, may be calculated using the following equation:

$$T_{J} = T_{A} + (P_{D} \times \Theta_{JA})$$
(1)

Where:

- T<sub>A</sub> is the ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in ° C/W,
- $P_D$  is the sum of  $P_{INT}$  and  $P_{I/O} (P_D = P_{INT} + P_{I/O})$ ,
- P<sub>INT</sub> is the product of I<sub>DD</sub> and V<sub>DD</sub>, expressed in Watts. This is the Chip Internal Power.

P<sub>I/O</sub> represents the power dissipation on input and output pins;

Most of the time for the applications  $P_{I/O} < P_{INT}$  and may be neglected. On the other hand,  $P_{I/O}$  may be significant if the device is configured to drive continuously external modules and/or memories. The worst case  $P_{INT}$  of the STR91xFA is 500 mW ( $I_{DD} \times V_{DD}$ , or 250 mA x 2.0 V).

An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is given by:

$$P_{D} = K / (T_{J} + 273 \ ^{\circ}C)$$
 (2)

Therefore (solving equations 1 and 2):

$$K = P_{D} x (T_{A} + 273 °C) + \Theta_{JA} x P_{D}^{2}$$
(3)

Where:

 K is a constant for the particular part, which may be determined from equation (3) by measuring P<sub>D</sub> (at equilibrium) for a known T<sub>A</sub>. Using this value of K, the values of P<sub>D</sub> and T<sub>J</sub> may be obtained by solving equations (1) and (2) iteratively for any value of T<sub>A</sub>.

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	<i>Thermal resistance junction-ambient</i> LQFP 80 - 12 x 12 mm / 0.5 mm pitch	41.5	°C/W
$\Theta_{JA}$	<i>Thermal resistance junction-ambient</i> LQFP128 - 14 x 14 mm / 0.4 mm pitch	38	°C/W
$\Theta_{JA}$	<i>Thermal resistance junction-ambient</i> LFBGA 144 - 10 x 10 x 1.7 mm	36.5	°C/W

Table	53.	Thermal	characteristics
10010			



Date	Revision	Changes
02-Jul-2009	6	Section 3.13.7: Tamper detection: Removed information about "Normally Closed/Tamper Open mode". Table 31: I/O characteristics: Updated V <sub>HYS</sub> row.
3-Mar-2015	7	Updated Figure 40: LQFP80 12 x 12 mm 80 pin low-profile quad flat package outline on page 95, Figure 43: LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline on page 98 and Figure 45: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline on page 101 Updated Table 50: LQFP80 12 x12 mm low-profile quad flat package mechanical data on page 96, Table 51: LQFP128 - 128- pin, 14 x 14 mm low-profile quad flat package mechanical data on page 99, and Table 52: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data on page 102 Added Figure 42: LQFP80 package top view on page 97, Figure 43: LQFP128 14 x 14 mm 128 pin low-profile quad flat package outline on page 98, Figure 44: LQFP128 package top view on page 100 and Figure 45: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline on page 101

Table 55. Document revision history

