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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/str912faz47h6">https://www.e-xfl.com/product-detail/stmicroelectronics/str912faz47h6</a>

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## 3.9 Vectored interrupt controller (VIC)

Interrupt management in the STR91xFA is implemented from daisy-chaining two standard ARM VIC units. This combined VIC has 32 prioritized interrupt request channels and generates two interrupt output signals to the CPU. The output signals are FIQ and IRQ, with FIQ having higher priority.

### 3.9.1 FIQ handling

FIQ (Fast Interrupt reQuest) is the only non-vectored interrupt and the CPU can execute an Interrupt Service Routine (ISR) directly without having to determine/prioritize the interrupt source, minimizing ISR latency. Typically only one interrupt source is assigned to FIQ. An FIQ interrupt has its own set of banked registers to minimize the time to make a context switch. Any of the 32 interrupt request input signals coming into the VIC can be assigned to FIQ.

### 3.9.2 IRQ handling

IRQ is a vectored interrupt and is the logical OR of all 32 interrupt request signals coming into the 32 IRQ channels. Priority of individual vectored interrupt requests is determined by hardware (IRQ channel Intr 0 is highest priority, IRQ channel Intr 31 is lowest).

However, inside the same VIC (primary or secondary VIC), CPU firmware may re-assign individual interrupt sources to individual hardware IRQ channels, meaning that firmware can effectively change interrupt priority levels as needed within the same VIC (from priority 0 to priority 16).

*Note: VIC0 (primary VIC) interrupts always have higher priority than VIC1 (secondary VIC) interrupts*

When the IRQ signal is activated by an interrupt request, VIC hardware will resolve the IRQ interrupt priority, then the ISR reads the VIC to determine both the interrupt source and the vector address to jump to the service code.

The STR91xFA has a feature to reduce ISR response time for IRQ interrupts. Typically, it requires two memory accesses to read the interrupt vector address from the VIC, but the STR91xFA reduces this to a single access by adding a 16th entry in the instruction branch cache, dedicated for interrupts. This 16th cache entry always holds the instruction that reads the interrupt vector address from the VIC, eliminating one of the memory accesses typically required in traditional ARM implementations.

### 3.9.3 Interrupt sources

The 32 interrupt request signals coming into the VIC on 32 IRQ channels are from various sources; 5 from a wake-up unit and the remaining 27 come from internal sources on the STR91xFA such as on-chip peripherals, see [Table 6](#). Optionally, firmware may force an interrupt on any IRQ channel.

One of the 5 interrupt requests generated by the wake-up unit (IRQ25 in [Table 6](#)) is derived from the logical OR of all 32 inputs to the wake-up unit. Any of these 32 inputs may be used to wake up the CPU and cause an interrupt. These 32 inputs consist of 30 external interrupts on selected and enabled GPIO pins, plus the RTC interrupt, and the USB Resume interrupt.

### 3.10.5 Flash memory interface clock (FMICLK)

The FMICLK clock is an internal clock derived from RCLK, defaulting to RCLK frequency at power up. The clock can be optionally divided by 2. The FMICLK determines the bus bandwidth between the ARM core and the Flash memory. Typically, codes in the Flash memory can be fetched one word per FMICLK clock in burst mode. The maximum FMICLK frequency is 96 MHz.

### 3.10.6 UART and SSP clock (BRCLK)

BRCLK is an internal clock derived from  $f_{MSTR}$  that is used to drive the two SSP peripherals and to generate the Baud rate for the three on-chip UART peripherals. The frequency can be optionally divided by 2.

### 3.10.7 External memory interface bus clock (BCLK)

The BCLK is an internal clock that controls the EMI bus. All EMI bus signals are synchronized to the BCLK. The BCLK is derived from the HCLK and the frequency can be configured to be the same or half that of the HCLK. Refer to [Table 17 on page 66](#) for the maximum BCLK frequency ( $f_{BCLK}$ ). The BCLK clock is available on the LFBGA package as an output pin.

### 3.10.8 USB interface clock

Special consideration regarding the USB interface: The clock to the USB interface must operate at 48 MHz and comes from one of three sources, selected under firmware control:

- CCU master clock output of 48 MHz.
- CCU master clock output of 96 MHz. An optional divided-by-two circuit is available to produce 48 MHz for the USB while the CPU system runs at 96MHz.
- STR91xFA pin P2.7. An external 48 MHz oscillator connected to pin P2.7 can directly source the USB while the CCU master clock can run at some frequency other than 48 or 96 MHz.

### 3.10.9 Ethernet MAC clock

Special consideration regarding the Ethernet MAC: The external Ethernet PHY interface device requires it's own 25 MHz clock source. This clock can come from one of two sources:

- A 25 MHz clock signal coming from a dedicated output pin (P5.2) of the STR91xFA. In this case, the STR91xFA must use a 25 MHz signal on its main oscillator input in order to pass this 25 MHz clock back out to the PHY device through pin P5.2. The advantage here is that an inexpensive 25 MHz crystal may be used to source a clock to both the STR91xFA and the external PHY device.
- An external 25 MHz oscillator connected directly to the external PHY interface device. In this case, the STR91xFA can operate independent of 25 MHz.

### 3.10.10 External RTC calibration clock

The RTC\_CLK can be enabled as an output on the JRTCK pin. The RTC\_CLK is used for RTC oscillator calibration. The RTC\_CLK is active in Sleep mode and can be used as a system wake up control clock.

### 3.12.2 Battery supply

An optional stand-by voltage from a battery or other source may be connected to pin VBATT to retain the contents of SRAM in the event of a loss of the main digital supplies ( $V_{DD}$  and  $V_{DDQ}$ ). The SRAM will automatically switch its supply from the internal  $V_{DD}$  source to the VBATT pin when the voltage of  $V_{DD}$  drops below the LVD threshold. In order to use the battery supply, the LVD must be enabled.

The VBATT pin also supplies power to the RTC unit, allowing the RTC to function even when the main digital supplies ( $V_{DD}$  and  $V_{DDQ}$ ) are switched off. By configuring the RTC register, it is possible to select whether or not to power from VBATT only the RTC unit, or power the RTC unit and the SRAM when the STR91xFA device is powered off.

## 3.13 System supervisor

The STR91xFA monitors several system and environmental inputs and will generate a global reset, a system reset, or an interrupt based on the nature of the input and configurable settings. A global reset clears all functions on the STR91xFA, a system reset will clear all but the Clock Control Unit (CCU) settings and the system status register. At any time, firmware may reset individual on-chip peripherals. System supervisor inputs include:

- GR: CPU voltage supply ( $V_{DD}$ ) drop out or brown out
- GR: I/O voltage supply ( $V_{DDQ}$ ) drop out or brown out
- GR: Power-Up condition
- SR: Watchdog timer timeout
- SR: External reset pin (RESET\_INn)
- SR: JTAG debug reset command

*Note:* GR: means the input causes Global Reset, SR: means the input causes System Reset

The CPU may read a status register after a reset event to determine if the reset was caused by a watchdog timer timeout or a voltage supply drop out. This status register is cleared only by a power up reset.

### 3.13.1 Supply voltage brownout

Each operating voltage source ( $V_{DD}$  and  $V_{DDQ}$ ) is monitored separately by the Low Voltage Detect (LVD) circuitry. The LVD will generate an early warning interrupt to the CPU when voltage sags on either  $V_{DD}$  or  $V_{DDQ}$  voltage inputs. This is an advantage for battery powered applications because the system can perform an orderly shutdown before the batteries become too weak. The voltage trip point to cause a brown out interrupt is typically 0.25V above the LVD dropout thresholds that cause a reset.

CPU firmware may prevent all brown-out interrupts by writing to interrupt mask registers at run-time.

### 3.13.2 Supply voltage dropout

LVD circuitry will always cause a global reset if the CPU's  $V_{DD}$  source drops below its fixed threshold of 1.4 V.

However, the LVD trigger threshold to cause a global reset for the I/O ring's  $V_{DDQ}$  source is set to one of two different levels, depending if  $V_{DDQ}$  will be operated in the range of 2.7 V to 3.3 V, or 3.0V to 3.6 V. If  $V_{DDQ}$  operation is at 2.7 V to 3.3 V, the LVD dropout trigger threshold is 2.4 V. If  $V_{DDQ}$  operation is 3.0 V and 3.6 V, the LVD threshold is 2.7 V. The choice of trigger level is made by STR91xFA device configuration software from STMicroelectronics or IDE from 3rd parties, and is programmed into the STR91xFA device along with other configurable items through the JTAG interface when the Flash memory is programmed.

CPU firmware may prevent some LVD resets if desired by writing a control register at run-time. Firmware may also disable the LVD completely for lowest-power operation when an external LVD device is being used.

### 3.13.3 Watchdog timer

The STR91xFA has a 16-bit down-counter (not one of the four TIM timers) that can be used as a watchdog timer or as a general purpose free-running timer/counter. The clock source is the peripheral clock from the APB, and an 8-bit clock pre-scaler is available. When enabled by firmware as a watchdog, this timer will cause a system reset if firmware fails to periodically reload this timer before the terminal count of 0x0000 occurs, ensuring firmware sanity. The watchdog function is off by default after a reset and must be enabled by firmware.

### 3.13.4 External RESET\_INn pin

This input signal is active-low with hystereses ( $V_{HYS}$ ). Other open-drain, active-low system reset signals on the circuit board (such as closure to ground from a push-button) may be connected directly to the RESET\_INn pin, but an external pull-up resistor to  $V_{DDQ}$  must be present as there is no internal pullup on the RESET\_INn pin.

A valid active-low input signal of  $t_{RINMIN}$  duration on the RESET\_INn pin will cause a system reset within the STR91xFA. There is also a RESET\_OUTn pin on the STR91xFA that can drive other system components on the circuit board. RESET\_OUTn is active-low and has the same timing of the Power-On-Reset (POR) shown next,  $t_{POR}$ .

### 3.13.5 Power-up

The LVD circuitry will always generate a global reset when the STR91xFA powers up, meaning internal reset is active until  $V_{DDQ}$  and  $V_{DD}$  are both above the LVD thresholds. This POR condition has a duration of  $t_{POR}$ , after which the CPU will fetch its first instruction from address 0x0000.0000 in Flash memory. It is not possible for the CPU to boot from any other source other than Flash memory.

### 3.13.6 JTAG debug command

When the STR91xFA is in JTAG debug mode, an external device which controls the JTAG interface can command a system reset to the STR91xFA over the JTAG channel.

## 3.20 UART interfaces with DMA

The STR91xFA supports three independent UART serial interfaces, designated UART0, UART1, and UART2. Each interface is very similar to the industry-standard 16C550 UART device. All three UART channels support IrDA encoding/decoding, requiring only an external LED transceiver to pins UARTx\_RX and UARTx\_Tx for communication. One UART channel (UART0) supports full modem control signals.

UART interfaces include the following features:

- Maximum baud rate of 1.5 Mbps
- Separate FIFOs for transmit and receive, each 16 deep, each FIFO can be disabled by firmware if desired
- Programmable FIFO trigger levels between 1/8 and 7/8
- Programmable baud rate generator based on CCU master clock, or CCU master clock divided by two
- Programmable serial data lengths of 5, 6, 7, or 8 bits with start bit and 1 or 2 stop bits
- Programmable selection of even, odd, or no-parity bit generation and detection
- False start-bit detection
- Line break generation and detection
- Support of IrDA SIR ENDEC functions for data rates of up to 115.2K bps
- IrDA bit duration selection of 3/16 or low-power (1.14 to 2.23  $\mu$ sec)
- Channel UART0 supports modem control functions CTS, DCD, DSR, RTS, DTR, and RI

For your reference, only two standard 16550 UART features are not supported, 1.5 stop bits and independent receive clock.

### 3.20.1 DMA

A programmable DMA channel may be assigned by CPU firmware to service channels UART0 and UART1 for fast and direct transfers between the UART bus and SRAM with little CPU involvement. Both DMA single-transfers and DMA burst-transfers are supported for transmit and receive. Burst transfers require that UART FIFOs are enabled.

## 3.21 I<sup>2</sup>C interfaces

The STR91xFA supports two independent I2C serial interfaces, designated I2C0, and I2C1. Each interface allows direct connection to an I2C bus as either a bus master or bus slave device (firmware configurable). I2C is a two-wire communication channel, having a bi-directional data signal and a single-directional clock signal based on open-drain line drivers, requiring external pull-up resistors.

Byte-wide data is transferred between a Master device and a Slave device on two wires. More than one bus Master is allowed, but only one Master may control the bus at any given time. Data is not lost when another Master requests the use of a busy bus because I2C supports collision detection and arbitration. More than one Slave device may be present on the bus, each having a unique address. The bus Master initiates all data movement and generates the clock that permits the transfer. Once a transfer is initiated by the Master, any device that is addressed is considered a Slave. Automatic clock synchronization allows I2C devices with different bit rates to communicate on the same physical bus.



## 5.2 Default pin functions

During and just after reset, all pins on ports 0-9 default to high-impedance input mode until CPU firmware assigns other functions to the pins. This initial input mode routes all pins on ports 0-9 to be read as GPIO inputs as shown in the “Default Pin Function” column of [Table 8](#). Simultaneously, certain port pin signals are also routed to other functional inputs as shown in the “Default Input Function” column of [Table 8](#), and these pin input functions will remain until CPU firmware makes other assignments. At any time, even after the CPU assigns pins to alternate functions, the CPU may always read the state of any pin on ports 0-9 as a GPIO input. CPU firmware may assign alternate functions to port pins as shown in columns “Alternate Input 1” or “Alternate Output 1, 2, 3” of [Table 8](#) by writing to control registers at run-time.

### 5.2.1 General notes on pin usage

- 1 *Since there are no internal or programmable pull-up resistors on ports 0-9, it is advised to pull down to ground, or pull up to VDDQ (using max. 47 K $\Omega$  resistors), all unused pins on port 0-9. Another solution is to use the GPIO control registers to configure the unused pins on ports 0-9 as output low level. The purpose of this is to reduce noise susceptibility, noise generation, and minimize power consumption*
- 2 *All pins on ports 0 - 9 are 5V tolerant*
- 3 *Pins on ports 0,1,2,4,5,7,8,9 have 4 mA drive and 4mA sink. Ports 3 and 6 have 8 mA drive and 8 mA sink.*
- 4 *For 8-bit non-muxed EMI operation: Port 8 is eight bits of data, ports 7 and 9 are 16 bits of address.*
- 5 *For 16-bit muxed EMI operation: Ports 8 and 9 are 16 bits of muxed address and data bits, port 7 is up to eight additional bits of high-order address*
- 6 *Signal polarity is programmable for interrupt request inputs, EMI\_ALE, timer input capture inputs and output compare/PWM outputs, motor control tach and emergency stop inputs, and motor control phase outputs.*
- 7 *HiZ = High Impedance, V = Voltage Source, G = Ground, I/O = Input/Output*
- 8 *STR910FA devices do not support USB. On these devices USBDP and USBDN signals are "Not Used" (USBDN is not connected, USBDP must be pulled up by a 1.5K ohm resistor to VDDQ), and all functions named "USB" are not available.*
- 9 *STR910FA 128-pin and 144-ball devices do not support Ethernet. On these devices PHYCLK and all functions named "MII\*" are not available.*

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
12	18	F6	P5.1	I/O	GPIO_5.1, GP Input, HiZ	EXINT9, External Intr	UART0_RxD, UART rcv data	GPIO_5.1, GP Output	CAN_TX, CAN Tx data	UART2_TX, UART xmit data
17	25	K1	PHYCLK_P5.2	I/O	GPIO_5.2, GP Input, HiZ	EXINT10, External Intr	UART2_RxD, UART rcv data	GPIO_5.2, GP Output	MII_PHYCLK, 25Mhz to PHY	TIM3_OCMP1, Out comp/PWM
18	27	H2	P5.3	I/O	GPIO_5.3, GP Input, HiZ	EXINT11, External Intr	ETM_EXTRIG, ETM ext. trigger	GPIO_5.3, GP Output	MII_TX_EN, MAC xmit enbl	TIM2_OCMP1, Out comp/PWM
44	70	J12	P5.4	I/O	GPIO_5.4, GP Input, HiZ	EXINT12, External Intr	SSP0_SCLK, SSP slv clk in	GPIO_5.4, GP Output	SSP0_SCLK, SSP mstr clk out	EMI_CS0n, EMI Chip Select
47	77	H11	P5.5	I/O	GPIO_5.5, GP Input, HiZ	EXINT13, External Intr	SSP0_MOSI, SSP slv dat in	GPIO_5.5, GP Output	SSP0_MOSI, SSP mstr dat out	EMI_CS1n, EMI Chip Select
48	79	H9	P5.6	I/O	GPIO_5.6, GP Input, HiZ	EXINT14, External Intr	SSP0_MISO, SSP mstr dat in	GPIO_5.6, GP Output	SSP0_MISO, SSP slv data out	EMI_CS2n, EMI Chip Select
49	80	G12	P5.7	I/O	GPIO_5.7, GP Input, HiZ	EXINT15, External Intr	SSP0_NSS, SSP slv select in	GPIO_5.7, GP Output	SSP0_NSS, SSP mstr sel out	EMI_CS3n, EMI Chip Select
19	29	H4	P6.0	I/O	GPIO_6.0, GP Input, HiZ	EXINT16, External Intr	TIM0_ICAP1, Input Capture	GPIO_6.0, GP Output	TIM0_OCMP1, Out comp/PWM	MC_UH, IMC phase U hi
20	31	J3	P6.1	I/O	GPIO_6.1, GP Input, HiZ	EXINT17, External Intr	TIM0_ICAP2, Input Capture	GPIO_6.1, GP Output	TIM0_OCMP2, Out comp	MC_UL, IMC phase U lo
13	19	G2	P6.2	I/O	GPIO_6.2, GP Input, HiZ	EXINT18, External Intr	TIM1_ICAP1, Input Capture	GPIO_6.2, GP Output	TIM1_OCMP1, Out comp/PWM	MC_VH, IMC phase V hi
14	20	G3	P6.3	I/O	GPIO_6.3, GP Input, HiZ	EXINT19, External Intr	TIM1_ICAP2, Input Capture	GPIO_6.3, GP Output	TIM1_OCMP2, Out comp	MC_VL, IMC phase V lo
52	83	G8	P6.4	I/O	GPIO_6.4, GP Input, HiZ	EXINT20, External Intr	TIM2_ICAP1, Input Capture	GPIO_6.4, GP Output	TIM2_OCMP1, Out comp/PWM	MC_WH, IMC phase W hi
53	84	G7	P6.5	I/O	GPIO_6.5, GP Input, HiZ	EXINT21, External Intr	TIM2_ICAP2, Input Capture	GPIO_6.5, GP Output	TIM2_OCMP2, Out comp	MC_WL, IMC phase W lo
57	92	E9	P6.6	I/O	GPIO_6.6, GP Input, HiZ	EXINT22_TRIG, Ext Intr & Tach	UART0_RxD, UART rcv data	GPIO_6.6, GP Output	TIM3_OCMP1, Out comp/PWM	ETM_TRCLK, ETM trace clock
58	93	D12	P6.7	I/O	GPIO_6.7, GP Input, HiZ	EXINT23_STOP, Ext Intr & Estop	ETM_EXTRIG, ETM ext. trigger	GPIO_6.7, GP Output	TIM3_OCMP2, Out comp	UART0_TX, UART xmit data
-	5	D1	P7.0	I/O	GPIO_7.0, GP Input, HiZ	EXINT24, External Intr	TIM0_ICAP1, Input Capture	GPIO_7.0, GP Output	8b) EMI_A0, 16b) EMI_A16	ETM_PCK0, ETM Packet
-	6	D2	P7.1	I/O	GPIO_7.1, GP Input, HiZ	EXINT25, External Intr	TIM0_ICAP2, Input Capture	GPIO_7.1, GP Output	8b) EMI_A1, 16b) EMI_A17	ETM_PCK1, ETM Packet
-	7	B1	P7.2	I/O	GPIO_7.2, GP Input, HiZ	EXINT26, External Intr	TIM2_ICAP1, Input Capture	GPIO_7.2, GP Output	8b) EMI_A2, 16b) EMI_A18	ETM_PCK2, ETM Packet
-	13	F1	P7.3	I/O	GPIO_7.3, GP Input, HiZ	EXINT27, External Intr	TIM2_ICAP2, Input Capture	GPIO_7.3, GP Output	8b) EMI_A3, 16b) EMI_A19	ETM_PCK3, ETM Packet
-	14	G1	P7.4	I/O	GPIO_7.4, GP Input, HiZ	EXINT28, External Intr	UART0_RxD, UART rcv data	GPIO_7.4, GP Output	8b) EMI_A4, 16b) EMI_A20	EMI_CS3n, EMI Chip Select
-	15	E5	P7.5	I/O	GPIO_7.5, GP Input, HiZ	EXINT29, External Intr	ETM_EXTRIG, ETM ext. trigger	GPIO_7.5, GP Output	8b) EMI_A5, 16b) EMI_A21	EMI_CS2n, EMI Chip Select

## 6 Memory mapping

The ARM966E-S CPU addresses a single linear address space of 4 giga-bytes ( $2^{32}$ ) from address 0x0000.0000 to 0xFFFF.FFFF as shown in [Figure 9](#). Upon reset the CPU boots from address 0x0000.0000, which is chip-select zero at address zero in the Flash Memory Interface (FMI).

The Instruction TCM and Data TCM enable high-speed CPU operation without incurring any performance or power penalties associated with accessing the system buses (AHB and APB). I-TCM and D-TCM address ranges are shown at the bottom of the memory map in [Figure 9](#).

### 6.1 Buffered and non-buffered writes

The CPU makes use of write buffers on the AHB and the D-TCM to decouple the CPU from any wait states associated with a write operation. The user may choose to use write with buffers on the AHB by setting bit 3 in control register CP15 and selecting the appropriate AHB address range when writing. By default at reset, buffered writes are disabled (bit 3 of CP15 is clear) and all AHB writes are non-buffered until enabled. [Figure 9](#) shows that most addressable items on the AHB are aliased at two address ranges, one for buffered writes and another for non-buffered writes. A buffered write will allow the CPU to continue program execution while the write-back is performed through a FIFO to the final destination on the AHB. If the FIFO is full, the CPU is stalled until FIFO space is available. A non-buffered write will impose an immediate delay to the CPU, but results in a direct write to the final AHB destination, ensuring data coherency. Read operations from AHB locations are always direct and never buffered.

### 6.2 System (AHB) and peripheral (APB) buses

The CPU will access SRAM, higher-speed peripherals (USB, Ethernet, Programmable DMA), and the external bus (EMI) on the AHB at their respective base addresses indicated in [Figure 9](#). Lower-speed peripherals reside on the APB and are accessed using two separate AHB-to-APB bridge units (APB0 and APB1). These bridge units are essentially address windows connecting the AHB to the APB. To access an individual APB peripheral, the CPU will place an address on the AHB bus equal to the base address of the appropriate bridge unit APB0 or APB1, plus the offset of the particular peripheral, plus the offset of the individual data location within the peripheral. [Figure 9](#) shows the base addresses of bridge units APB0 and APB1, and also the base address of each APB peripheral. Please consult the STR91xFA Reference manual for the address of data locations within each individual peripheral.

## 7.3 Operating conditions

Table 11. Operating conditions

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
V <sub>DD</sub>	Digital CPU supply voltage	Flash size ≤12 KB	1.65	2.0	V
		Flash size = 1 MB / 2 MB, f <sub>CPUCCLK</sub> ≤85 MHz <sup>(1)</sup>	1.65	2.0	V
		Flash size = 1 MB / 2 MB, f <sub>CPUCCLK</sub> ≤96 MHz <sup>(2)</sup>	1.77	2.0	V
V <sub>DDQ</sub>	Digital I/O supply voltage		2.7	3.6	V
V <sub>BATT</sub> <sup>(3)</sup>	SRAM backup and RTC supply voltage		2.5	3.6	V
AV <sub>DD</sub>	Analog ADC supply voltage (128-pin and 144-ball packages)		2.7	V <sub>DDQ</sub>	V
AV <sub>REF</sub>	Analog ADC reference voltage (128-pin and 144-ball packages)		2.65	AV <sub>DD</sub> <sup>(4)</sup>	V
AV <sub>REF_AVDD</sub>	Combined analog ADC reference and ADC supply voltage (80-pin package)		2.7	V <sub>DDQ</sub>	V
T <sub>A</sub>	Ambient temperature under bias		-40	+85	C

1. f<sub>FMICLK</sub> ≤48 MHz during Flash write and 85 MHz during all other operations.

2. f<sub>FMICLK</sub> ≤48 MHz during Flash write and 96 MHz during all other operations.

3. The V<sub>BATT</sub> pin should be connected to V<sub>DDQ</sub> if no battery is installed

4. AV<sub>REF</sub> must never exceed V<sub>DDQ</sub>

### 7.3.1 Operating conditions at power-up / power-down

Subject to general operating conditions for T<sub>A</sub>.

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Min <sup>(1)</sup>	Max <sup>(1)</sup>	Unit
t <sub>VDD</sub>	V <sub>DD</sub> rise time rate	10		μs/V
			10	ms/V

1. Data guaranteed by characterization, not tested in production.

Table 25. Flash memory program/erase characteristics (Flash size = 1 MB / 2 MB)

Parameter		Test conditions	Value			Unit
			Typ <sup>(1)</sup>	Typ after 100K W/E cycles <sup>(1)</sup>	Max	
Bank erase	Primary bank (2 Mbytes)		32	36	46	s
	Primary bank (1 Mbytes)		16	18	23	s
	Secondary bank (128 Kbytes)		2.5	3	4	s
Sector erase	Of primary bank (64 Kbytes)		1300	1400	1800	ms
	Of secondary bank (16 Kbytes)		500	600	850	ms
Bank program	Primary bank (2 Mbytes)		15	20	22	s
	Primary bank (1 Mbytes)		7.5	10	11	s
	Secondary bank (128 Kbytes)		1060	1140	1380	ms
Sector program	Of primary bank (64 Kbytes)		500	520	640	ms
	Of secondary bank (16 Kbytes)		120	130	160	ms
Word program		Half word (16 bits)	8	9	11	µs

1.  $V_{DD} = 1.8\text{ V}$ ,  $V_{DDQ} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

Table 26. Flash memory endurance

Parameter	Test conditions	Value			Unit
		Min	Typ	Max	
Program/erase cycles	Per word	100K			cycles
Data retention		20			years

### 7.9.5 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

### 7.9.6 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### 7.9.7 Electrical sensitivity

**Table 30. Static latch-up data**

Symbol	Parameter	Conditions	Class <sup>(1)</sup>
LU	Static latch-up class	T <sub>A</sub> = +25 °C conforming to JESD78A	II class A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

## 7.12 Communication interface electrical characteristics

### 7.12.1 10/100 Ethernet MAC electrical characteristics

$V_{DDQ} = 2.7 - 3.6 \text{ V}$ ,  $V_{DD} = 1.65 - 2 \text{ V}$ ,  $T_A = -40 / 85 \text{ }^{\circ}\text{C}$  unless otherwise specified.

#### Ethernet MII interface timings

Figure 25. MII\_RX\_CLK and MII\_TX\_CLK timing diagram

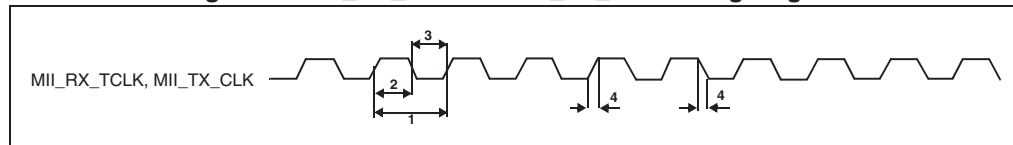


Table 40. MII\_RX\_CLK and MII\_TX\_CLK timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	Cycle time	$t_c(\text{CLK})$	40		ns
2	Pulse duration high	$t_{\text{HIGH}}(\text{CLK})$	40%	60%	
3	Pulse duration low	$t_{\text{LOW}}(\text{CLK})$	40%	60%	
4	Transition time	$t_t(\text{CLK})$		1	ns

Figure 26. MDC timing diagram

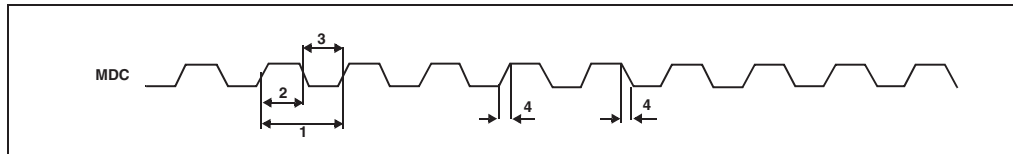


Table 41. MDC timing table

Symbol	Parameter	Symbol	Value		Unit
			Min	Max	
1	Cycle time	$t_c(\text{MDC})$	266		ns
2	Pulse duration high	$t_{\text{HIGH}}(\text{MDC})$	40%	60%	
3	Pulse duration low	$t_{\text{LOW}}(\text{MDC})$	40%	60%	
4	Transition time	$t_t(\text{MDC})$		1	ns

Table 48. ADC conversion time (silicon Rev G)

Symbol	Parameter <sup>(1) (2)</sup>	Test conditions	Value			Unit
			Min	Typ	Max	
t <sub>CONV(S)</sub>	Single mode conversion time		2*16/f <sub>ADC</sub>		3*16/f <sub>ADC</sub>	μs
		f <sub>ADC</sub> = 24 MHz	1.33		2	
TR(S)	Single mode throughput rate <sup>(3)</sup>	f <sub>ADC</sub> = 24 MHz			500	ksps
t <sub>CONV(C)</sub>	Continuous mode conversion time <sup>(4)</sup>			1*16/f <sub>ADC</sub>		μs
		f <sub>ADC</sub> = 24 MHz		0.66		μs
TR(C)	Continuous mode throughput rate	f <sub>ADC</sub> = 24 MHz		1500		ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev G. Refer to [Table 5](#) for device rev identification in OTP memory and to [Section 8: Device marking](#).
3. Value obtained on conversions started by trigger in single mode
4. All successive conversions in continuous and scan modes.

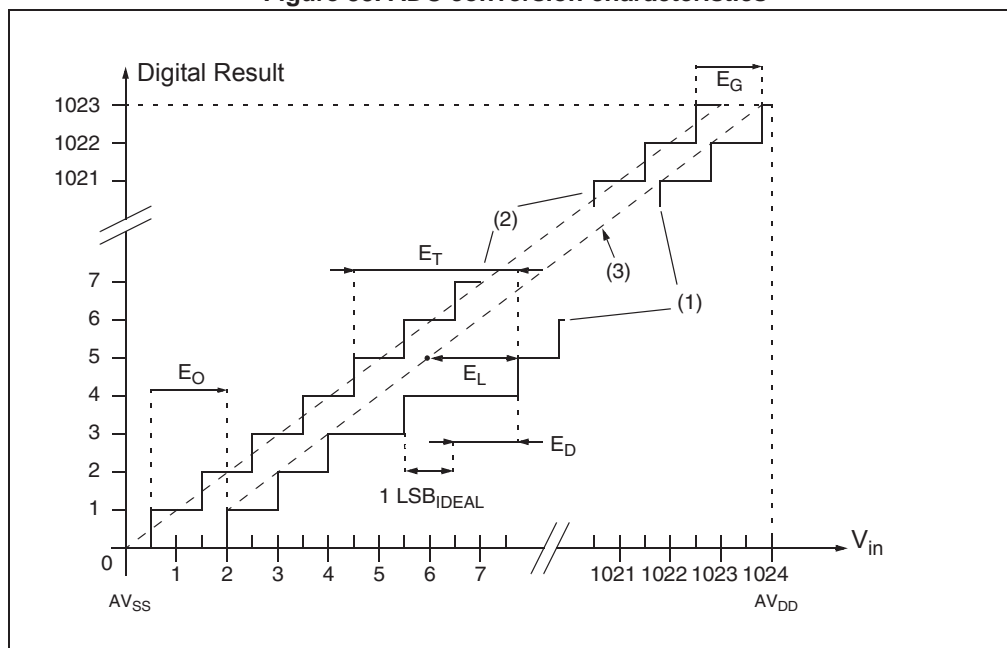
Table 49. ADC conversion time (silicon Rev H and higher)

Symbol	Parameter <sup>(1) (2)</sup>	Test conditions	Value			Unit
			Min	Typ	Max	
t <sub>CONV(S)</sub>	Single mode conversion time		1*16/f <sub>ADC</sub>		2*16/f <sub>ADC</sub>	μs
		f <sub>ADC</sub> = 24 MHz	0.66		1.33	
TR(S)	Single mode throughput rate <sup>(3)</sup>	f <sub>ADC</sub> = 24 MHz			750	ksps
t <sub>CONV(C)</sub>	Continuous mode conversion time <sup>(4)</sup>			1*16/f <sub>ADC</sub>		μs
		f <sub>ADC</sub> = 24 MHz		0.66		μs
TR(C)	Continuous mode throughput rate	f <sub>ADC</sub> = 24 MHz		1500		ksps
t <sub>CONV(FT)</sub>	Fast trigger mode conversion time <sup>(5)</sup>			1*16/f <sub>ADC</sub>		μs
		f <sub>ADC</sub> = 24 MHz		0.66		μs
TR(FT)	Fast trigger mode throughput rate <sup>(6)</sup>	f <sub>ADC</sub> = 24 MHz	100		1200	ksps

1. Guaranteed by design, not tested in production.
2. Parameters in this table apply to devices with silicon Rev H and higher. Refer to [Table 5](#) for device rev identification in OTP memory and to [Section 8: Device marking](#).
3. Value obtained from conversions started by trigger in single mode
4. All successive conversions in continuous and scan modes.
5. Conversion started by trigger when automatic clock gated mode enabled. Fast trigger mode is available only in devices with silicon Rev H and higher.
6. Value obtained from conversions started by fast trigger in single mode



Figure 33. ADC conversion characteristics



## 1. Legend:

(1) Example of an actual transfer curve

(2) The ideal transfer curve

(3) End point correlation line

 $E_T$  = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves. $E_O$  = Offset Error: deviation between the first actual transition and the first ideal one. $E_G$  = Gain Error: deviation between the last ideal transition and the last actual one. $E_D$  = Differential Linearity Error: maximum deviation between actual steps and the ideal one. $E_L$  = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

## Equation 1

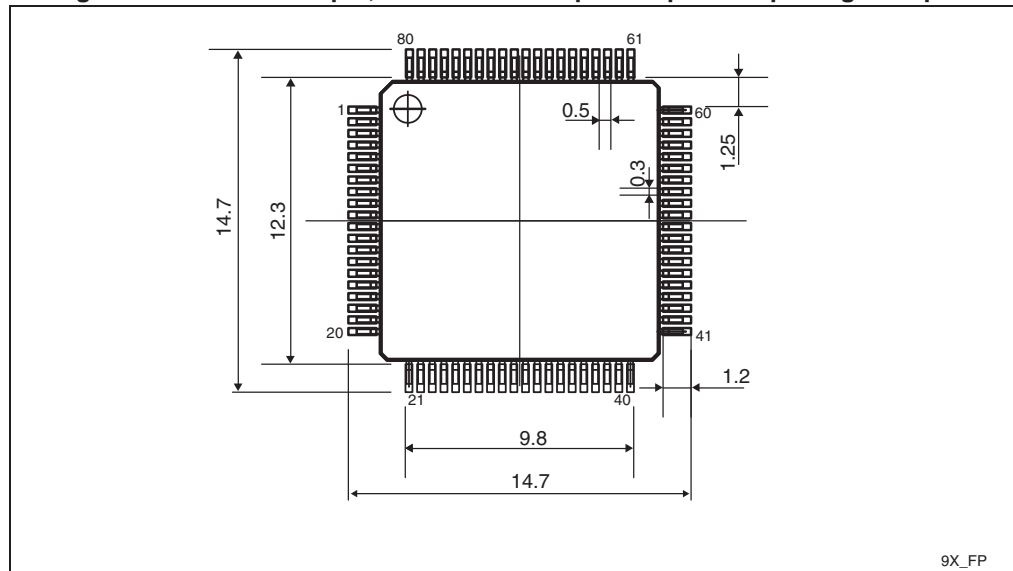
$$1\text{LSB}_{\text{IDEAL}} = \frac{V_{\text{DDA}} - V_{\text{SSA}}}{1024}$$

**Table 50. LQFP80 12 x12 mm low-profile quad flat package mechanical data**

Dim.	mm			inches <sup>(1)</sup>		
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	14.000	-	-	0.5512	-
D1	-	12.000	-	-	0.4724	-
D2	-	9.500	-	-	0.3740	-
E	-	14.000	-	-	0.5512	-
E1	-	12.000	-	-	0.4724	-
E3	-	9.500	-	-	0.3740	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	0.080			0.0031		
k	0.0°	-	7.0°	0.0°	-	7.0°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 41. LQFP80 - 80 pin, 12 x 12 mm low-profile quad flat package footprint**



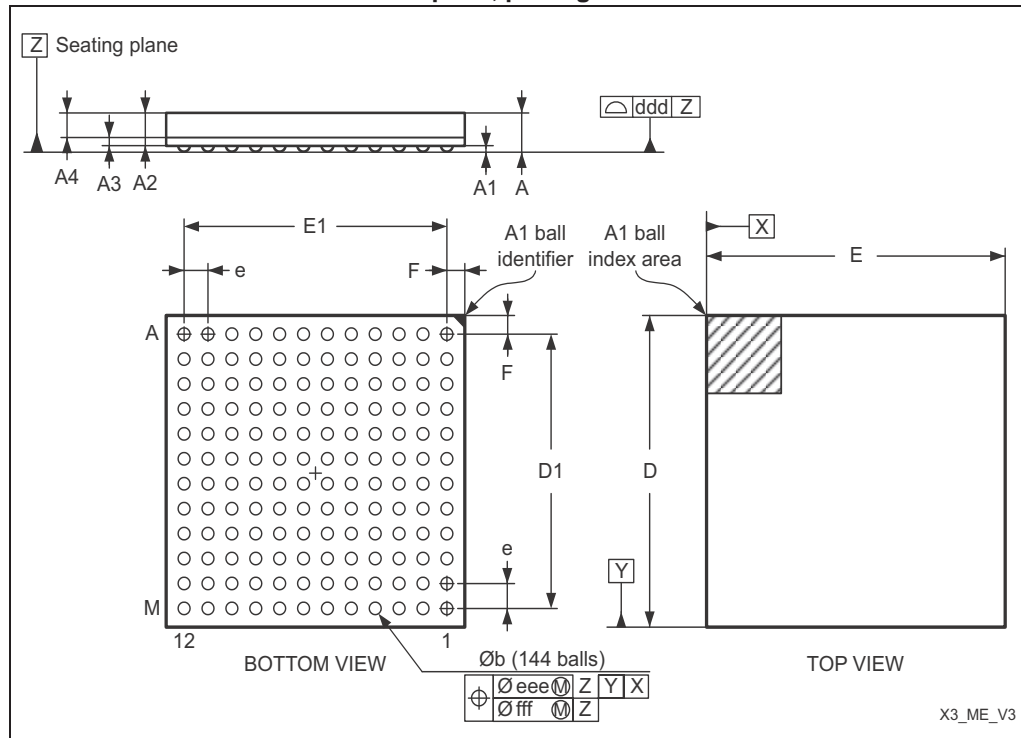
1. Dimensions are expressed in millimeters.

**Table 51. LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.130	0.180	0.230	0.0051	0.0071	0.0091
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.400	-	-	0.4882	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.400	-	-	0.4882	-
e	-	0.400	-	-	0.0157	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 45. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline**



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