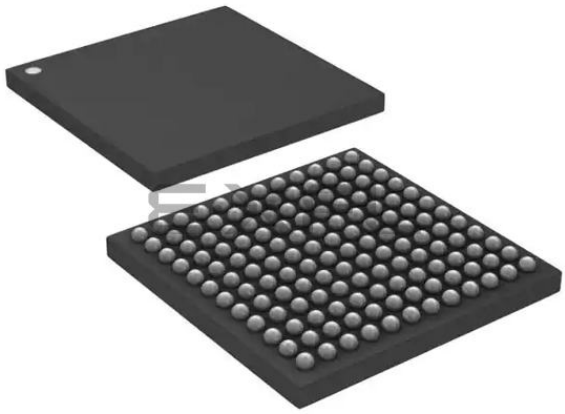

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	96MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str912faz47h6t

List of figures

1 Description

STR91xFA is a series of ARM®-powered microcontrollers which combines a 16/32-bit ARM966E-S RISC processor core, dual-bank Flash memory, large SRAM for data or code, and a rich peripheral set to form an ideal embedded controller for a wide variety of applications such as point-of-sale terminals, industrial automation, security and surveillance, vending machines, communication gateways, serial protocol conversion, and medical equipment. The ARM966E-S core can perform single-cycle DSP instructions, good for speech processing, audio algorithms, and low-end imaging.

Table 6. VIC IRQ channels (continued)

IRQ channel hardware priority	VIC input channel	Logic block	Interrupt source
25	VIC1.9	Wake-Up (all)	Logic OR of all 32 inputs of Wake-Up unit (30 pins, RTC, and USB Resume)
26	VIC1.10	Wake-up Group 0	Logic OR of 8 interrupt sources: RTC, USB Resume, pins P3.2 to P3.7
27	VIC1.11	Wake-up Group 1	Logic OR of 8 interrupts from pins P5.0 to P5.7
28	VIC1.12	Wake-up Group 2	Logic OR of 8 interrupts from pins P6.0 to P6.7
29	VIC1.13	Wake-up Group 3	Logic OR of 8 interrupts from pins P7.0 to P7.7
30	VIC1.14	USB	USB Bus Resume Wake-up (also input to wake-up unit)
31 (low priority)	VIC1.15	PFQ-BC	Special use of interrupts from Prefetch Queue and Branch Cache

3.10 Clock control unit (CCU)

The CCU generates a master clock of frequency f_{MSTR}. From this master clock the CCU also generates individually scaled and gated clock sources to each of the following functional blocks within the STR91xFA.

- CPU, f_{CPUCLK}
- Advanced High-performance Bus (AHB), f_{HCLK}
- Advanced Peripheral Bus (APB), f_{PCLK}
- Flash Memory Interface (FMI), f_{FMICLK}
- External Memory Interface (EMI), f_{BCLK}
- UART Baud Rate Generators, f_{BAUD}
- USB, f_{USB}

3.10.1 Master clock sources

The master clock in the CCU (f_{MSTR}) is derived from one of three clock input sources. Under firmware control, the CPU can switch between the three CCU inputs without introducing any glitches on the master clock output. Inputs to the CCU are:

- Main Oscillator (f_{OSC}). The source for the main oscillator input is a 4 to 25 MHz external crystal connected to STR91xFA pins X1_CPU and X2_CPU, or an external oscillator device connected to pin X1_CPU.
- PLL (f_{PLL}). The PLL takes the 4 to 25 MHz oscillator clock as input and generates a master clock output up to 96 MHz (programmable). By default, at power-up the master clock is sourced from the main oscillator until the PLL is ready (locked) and then the CPU may switch to the PLL source under firmware control. The CPU can switch back to the main oscillator source at any time and turn off the PLL for low-power operation. The PLL is always turned off in Sleep mode.
- RTC (f_{RTC}). A 32.768 kHz external crystal can be connected to pins X1_RTC and X2_RTC, or an external oscillator connected to pin X1_RTC to constantly run the real-time clock unit. This 32.768 kHz clock source can also be used as an input to the CCU to run the CPU in slow clock mode for reduced power.

3.10.5 Flash memory interface clock (FMICLK)

The FMICLK clock is an internal clock derived from RCLK, defaulting to RCLK frequency at power up. The clock can be optionally divided by 2. The FMICLK determines the bus bandwidth between the ARM core and the Flash memory. Typically, codes in the Flash memory can be fetched one word per FMICLK clock in burst mode. The maximum FMICLK frequency is 96 MHz.

3.10.6 UART and SSP clock (BRCLK)

BRCLK is an internal clock derived from f_{MSTR} that is used to drive the two SSP peripherals and to generate the Baud rate for the three on-chip UART peripherals. The frequency can be optionally divided by 2.

3.10.7 External memory interface bus clock (BCLK)

The BCLK is an internal clock that controls the EMI bus. All EMI bus signals are synchronized to the BCLK. The BCLK is derived from the HCLK and the frequency can be configured to be the same or half that of the HCLK. Refer to *Table 17 on page 66* for the maximum BCLK frequency (f_{BCLK}). The BCLK clock is available on the LFBGA package as an output pin.

3.10.8 USB interface clock

Special consideration regarding the USB interface: The clock to the USB interface must operate at 48 MHz and comes from one of three sources, selected under firmware control:

- CCU master clock output of 48 MHz.
- CCU master clock output of 96 MHz. An optional divided-by-two circuit is available to produce 48 MHz for the USB while the CPU system runs at 96MHz.
- STR91xFA pin P2.7. An external 48 MHz oscillator connected to pin P2.7 can directly source the USB while the CCU master clock can run at some frequency other than 48 or 96 MHz.

3.10.9 Ethernet MAC clock

Special consideration regarding the Ethernet MAC: The external Ethernet PHY interface device requires it's own 25 MHz clock source. This clock can come from one of two sources:

- A 25 MHz clock signal coming from a dedicated output pin (P5.2) of the STR91xFA. In this case, the STR91xFA must use a 25 MHz signal on its main oscillator input in order to pass this 25 MHz clock back out to the PHY device through pin P5.2. The advantage here is that an inexpensive 25 MHz crystal may be used to source a clock to both the STR91xFA and the external PHY device.
- An external 25 MHz oscillator connected directly to the external PHY interface device. In this case, the STR91xFA can operate independent of 25 MHz.

3.10.10 External RTC calibration clock

The RTC_CLK can be enabled as an output on the JRTCK pin. The RTC_CLK is used for RTC oscillator calibration. The RTC_CLK is active in Sleep mode and can be used as a system wake up control clock.

3.11.2 Idle mode

In this mode the CPU suspends code execution and the CPU and FMI clocks are turned off immediately after firmware sets the Idle Bit. Various peripherals continue to run based on the settings of the mask registers that exist just prior to entering Idle Mode. There are 3 ways to exit Idle Mode and return to Run Mode:

- Any reset (external reset pin, watchdog, low-voltage, power-up, JTAG debug command)
- Any interrupt (external, internal peripheral, RTC alarm or interval)
- Input from wake-up unit on GPIO pins

Note: It is possible to remain in Idle Mode for the majority of the time and the RTC can be programmed to periodically wake up to perform a brief task or check status.

3.11.3 Sleep mode

In this mode all clock circuits except the RTC are turned off and main oscillator input pins X1_CPU and X2_CPU are disabled. The RTC clock is required for the CPU to exit Sleep Mode. The entire chip is quiescent (except for RTC and wake-up circuitry). There are three means to exit Sleep Mode and re-start the system:

- Some resets (external reset pin, low-voltage, power-up, JTAG debug command)
- RTC alarm
- Input from wake-up unit

3.12 Voltage supplies

The STR91xFA requires two separate operating voltage supplies. The CPU and memories operate from a 1.65V to 2.0V on the VDD pins, and the I/O ring operates at 2.7V to 3.6V on the VDDQ pins.

In Standby mode, both VDD and VDDQ must be shut down. Otherwise the specified maximum power consumption for Standby mode (I_{RTC_STBY} and I_{SRAM_STBY}) may be exceeded. Leakage may occur if only one of the voltage supplies is off.

3.12.1 Independent A/D converter supply and reference voltage

The ADC unit on 128-pin and 144-ball packages has an isolated analog voltage supply input at pin AVDD to accept a very clean voltage source, independent of the digital voltage supplies. Additionally, an isolated analog supply ground connection is provided on pin AVSS only on 128-pin and 144-ball packages for further ADC supply isolation. On 80-pin packages, the analog voltage supply is shared with the ADC reference voltage pin (as described next), and the analog ground is shared with the digital ground at a single point in the STR91xFA device on pin AVSS_VSSQ.

A separate external analog reference voltage input for the ADC unit is available on 128-pin and 144-ball packages at the AVREF pin for better accuracy on low voltage inputs. For 80-pin packages, the ADC reference voltage is tied internally to the ADC unit supply voltage at pin AVREF_AVDD, meaning the ADC reference voltage is fixed to the ADC unit supply voltage.

See *Table 11: Operating conditions*, for restrictions to the relative voltage levels of VDDQ, AVDD, AVREF, and AVREF_AVDD.

3.13.2 Supply voltage dropout

LVD circuitry will always cause a global reset if the CPU's V_{DD} source drops below it's fixed threshold of 1.4 V.

However, the LVD trigger threshold to cause a global reset for the I/O ring's V_{DDQ} source is set to one of two different levels, depending if V_{DDQ} will be operated in the range of 2.7 V to 3.3 V, or 3.0V to 3.6 V. If V_{DDQ} operation is at 2.7 V to 3.3 V, the LVD dropout trigger threshold is 2.4 V. If V_{DDQ} operation is 3.0 V and 3.6 V, the LVD threshold is 2.7 V. The choice of trigger level is made by STR91xFA device configuration software from STMicroelectronics or IDE from 3rd parties, and is programmed into the STR91xFA device along with other configurable items through the JTAG interface when the Flash memory is programmed.

CPU firmware may prevent some LVD resets if desired by writing a control register at run-time. Firmware may also disable the LVD completely for lowest-power operation when an external LVD device is being used.

3.13.3 Watchdog timer

The STR91xFA has a 16-bit down-counter (not one of the four TIM timers) that can be used as a watchdog timer or as a general purpose free-running timer/counter. The clock source is the peripheral clock from the APB, and an 8-bit clock pre-scaler is available. When enabled by firmware as a watchdog, this timer will cause a system reset if firmware fails to periodically reload this timer before the terminal count of 0x0000 occurs, ensuring firmware sanity. The watchdog function is off by default after a reset and must be enabled by firmware.

3.13.4 External RESET_INn pin

This input signal is active-low with hystereses (V_{HYS}). Other open-drain, active-low system reset signals on the circuit board (such as closure to ground from a push-button) may be connected directly to the RESET_INn pin, but an external pull-up resistor to V_{DDQ} must be present as there is no internal pullup on the RESET_INn pin.

A valid active-low input signal of t_{RINMIN} duration on the RESET_INn pin will cause a system reset within the STR91xFA. There is also a RESET_OUTn pin on the STR91xFA that can drive other system components on the circuit board. RESET_OUTn is active-low and has the same timing of the Power-On-Reset (POR) shown next, t_{POR}.

3.13.5 Power-up

The LVD circuitry will always generate a global reset when the STR91xFA powers up, meaning internal reset is active until V_{DDQ} and V_{DD} are both above the LVD thresholds. This POR condition has a duration of t_{POR}, after which the CPU will fetch its first instruction from address 0x0000.0000 in Flash memory. It is not possible for the CPU to boot from any other source other than Flash memory.

3.13.6 JTAG debug command

When the STR91xFA is in JTAG debug mode, an external device which controls the JTAG interface can command a system reset to the STR91xFA over the JTAG channel.

Figure 6. EMI 8-bit non-multiplexed connection example

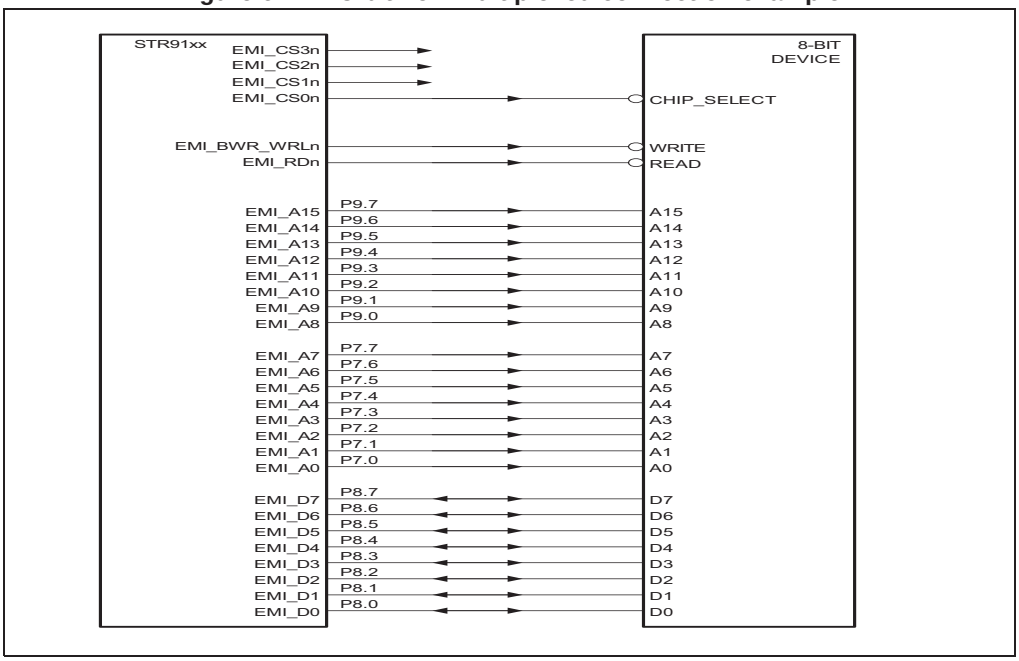


Table 8. Device pin description

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
-	67	L11	P0.0	I/O	GPIO_0.0, GP Input, HiZ	MII_TX_CLK, PHY Xmit clock	I2C0_CLKIN, I2C clock in	GPIO_0.0, GP Output	I2C0_CLKOUT, I2C clock out	ETM_PCK0, ETM Packet
-	69	K10	P0.1	I/O	GPIO_0.1, GP Input, HiZ	-	I2C0_DIN, I2C data in	GPIO_0.1, GP Output	I2C0_DOUT, I2C data out	ETM_PCK1, ETM Packet
-	71	J11	P0.2	I/O	GPIO_0.2, GP Input, HiZ	MII_RXD0, PHY Rx data0	I2C1_CLKIN, I2C clock in	GPIO_0.2, GP Output	I2C1_CLKOUT, I2C clock out	ETM_PCK2, ETM Packet
-	76	H12	P0.3	I/O	GPIO_0.3, GP Input, HiZ	MII_RXD1, PHY Rx data	I2C1_DIN, I2C data in	GPIO_0.3, GP Output	I2C1_DOUT, I2C data out	ETM_PCK3, ETM Packet
-	78	H10	P0.4	I/O	GPIO_0.4, GP Input, HiZ	MII_RXD2, PHY Rx data	TIM0_ICAP1, Input Capture	GPIO_0.4, GP Output	EMI_CS0n, EMI Chip Select	ETM_PSTAT0, ETM pipe status
-	85	F11	P0.5	I/O	GPIO_0.5, GP Input, HiZ	MII_RXD3, PHY Rx data	TIM0_ICAP2, Input Capture	GPIO_0.5, GP Output	EMI_CS1n, EMI Chip Select	ETM_PSTAT1, ETM pipe status
-	88	E11	P0.6	I/O	GPIO_0.6, GP Input, HiZ	MII_RX_CLK, PHY Rx clock	TIM2_ICAP1, Input Capture	GPIO_0.6, GP Output	EMI_CS2n, EMI Chip Select	ETM_PSTAT2, ETM pipe status
-	90	B12	P0.7	I/O	GPIO_0.7, GP Input, HiZ	MII_RX_DV, PHY data valid	TIM2_ICAP2, Input Capture	GPIO_0.7, GP Output	EMI_CS3n, EMI Chip Select	ETM_TRSYNC, ETM trace sync
-	98	B10	P1.0	I/O	GPIO_1.0, GP Input, HiZ	MII_RX_ER, PHY rcv error	ETM_EXTRIG, ETM ext. trigger	GPIO_1.0, GP Output	UART1_TX, UART xmit data	SSP1_SCLK, SSP mstr clk out
-	99	C10	P1.1	I/O	GPIO_1.1, GP Input, HiZ	-	UART1_RX, UART rcv data	GPIO_1.1, GP Output	MII_TXD0, MAC Tx data	SSP1_MOSI, SSP mstr dat out
-	101	B9	P1.2	I/O	GPIO_1.2, GP Input, HiZ	-	SSP1_MISO, SSP mstr data in	GPIO_1.2, GP Output	MII_TXD1, MAC Tx data	UART0_TX, UART xmit data
-	106	C8	P1.3	I/O	GPIO_1.3, GP Input, HiZ	-	UART2_RX, UART rcv data	GPIO_1.3, GP Output	MII_TXD2, MAC Tx data	SSP1_NSS, SSP mstr sel out
-	109	B7	P1.4	I/O	GPIO_1.4, GP Input, HiZ	-	I2C0_CLKIN, I2C clock in	GPIO_1.4, GP Output	MII_TXD3, MAC Tx data	I2C0_CLKOUT, I2C clock out
-	110	A7	P1.5	I/O	GPIO_1.5, GP Input, HiZ	MII_COL, PHY collision	CAN_RX, CAN rcv data	GPIO_1.5, GP Output	UART2_TX, UART xmit data	ETM_TRCLK, ETM trace clock
-	114	F7	P1.6	I/O	GPIO_1.6, GP Input, HiZ	MII_CRS, PHY carrier sns	I2C0_DIN, I2C data in	GPIO_1.6, GP Output	CAN_TX, CAN Tx data	I2C0_DOUT, I2C data out
-	116	D6	P1.7	I/O	GPIO_1.7, GP Input, HiZ	-	ETM_EXTRIG, ETM ext. trigger	GPIO_1.7, GP Output	MII_MDC, MAC mgt dat ck	ETM_TRCLK, ETM trace clock
7	10	E2	P2.0	I/O	GPIO_2.0, GP Input, HiZ	UART0_CTS, Clear To Send	I2C0_CLKIN, I2C clock in	GPIO_2.0, GP Output	I2C0_CLKOUT, I2C clock out	ETM_PCK0, ETM Packet
8	11	E3	P2.1	I/O	GPIO_2.1, GP Input, HiZ	UART0_DSR, Data Set Ready	I2C0_DIN, I2C data in	GPIO_2.1, GP Output	I2C0_DOUT, I2C data out	ETM_PCK1, ETM Packet
21	33	M1	P2.2	I/O	GPIO_2.2, GP Input, HiZ	UART0_DCD, Dat Carrier Det	I2C1_CLKIN, I2C clock in	GPIO_2.2, GP Output	I2C1_CLKOUT, I2C clock out	ETM_PCK2, ETM Packet
22	35	K3	P2.3	I/O	GPIO_2.3, GP Input, HiZ	UART0_RI, Ring Indicator	I2C1_DIN, I2C data in	GPIO_2.3, GP Output	I2C1_DOUT, I2C data out	ETM_PCK3, ETM Packet
23	37	L4	P2.4	I/O	GPIO_2.4, GP Input, HiZ	EXTCLK_T0T1E xt clk timer0/1	SSP0_SCLK, SSP slv clk in	GPIO_2.4, GP Output	SSP0_SCLK, SSP mstr clk out	ETM_PSTAT0, ETM pipe status

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
29	45	J5	P2.5	I/O	GPIO_2.5, GP Input, HiZ	EXTCLK_T2T3Ext clk timer2/3	SSP0_MOSI, SSP slv dat in	GPIO_2.5, GP Output	SSP0_MOSI, SSP mstr dat out	ETM_PSTAT1, ETM pipe status
32	53	G6	P2.6	I/O	GPIO_2.6, GP Input, HiZ	-	SSP0_MISO, SSP mstr data in	GPIO_2.6, GP Output	SSP0_MISO, SSP slv data out	ETM_PSTAT2, ETM pipe status
33	54	L7	USBCLK_P2.7	I/O	GPIO_2.7, GP Input, HiZ	USB_CLK48M, 48MHz to USB	SSP0_NSS, SSP slv sel in	GPIO_2.7, GP Output	SSP0_NSS, SSP mstr sel out	ETM_TRSYNC, ETM trace sync
34	55	K7	P3.0	I/O	GPIO_3.0, GP Input, HiZ	DMA_RQST0, Ext DMA requst	UART0_RxD, UART rcv data	GPIO_3.0, GP Output	UART2_TX, UART xmit data	TIM0_OCMP1, Out comp/PWM
37	59	M10	P3.1	I/O	GPIO_3.1, GP Input, HiZ	DMA_RQST1, Ext DMA requst	UART2_RxD, UART rcv data	GPIO_3.1, GP Output	UART0_TX, UART xmit data	TIM1_OCMP1, Out comp/PWM
38	60	M11	P3.2	I/O	GPIO_3.2, GP Input, HiZ	EXINT2, External Intr	UART1_RxD, UART rcv data	GPIO_3.2, GP Output	CAN_TX, CAN Tx data	UART0_DTR, Data Trmnl Rdy
39	61	J8	P3.3	I/O	GPIO_3.3, GP Input, HiZ	EXINT3, External Intr	CAN_RX, CAN rcv data	GPIO_3.3, GP Output	UART1_TX, UART xmit data	UART0_RTS, Ready To Send
40	63	L9	P3.4	I/O	GPIO_3.4, GP Input, HiZ	EXINT4, External Intr	SSP1_SCLK, SSP slv clk in	GPIO_3.4, GP Output	SSP1_SCLK, SSP mstr clk out	UART0_TX, UART xmit data
41	65	L10	P3.5	I/O	GPIO_3.5, GP Input, HiZ	EXINT5, External Intr	SSP1_MISO, SSP mstr data in	GPIO_3.5, GP Output	SSP1_MISO, SSP slv data out	UART2_TX, UART xmit data
42	66	M12	P3.6	I/O	GPIO_3.6, GP Input, HiZ	EXINT6, External Intr	SSP1_MOSI, SSP slv dat in	GPIO_3.6, GP Output	SSP1_MOSI, SSP mstr dat out	CAN_TX, CAN Tx data
43	68	K11	P3.7	I/O	GPIO_3.7, GP Input, HiZ	EXINT7, External Intr	SSP1_NSS, SSP slv select in	GPIO_3.7, GP Output	SSP1_NSS, SSP mstr sel out	TIM1_OCMP1, Out comp/PWM
4	3	C2	P4.0	I/O	GPIO_4.0, GP Input, HiZ	ADC0, ADC input chnl	TIM0_ICAP1, Input Capture	GPIO_4.0, GP Output	TIM0_OCMP1, Out comp/PWM	ETM_PCK0, ETM Packet
3	2	B2	P4.1	I/O	GPIO_4.1, GP Input, HiZ	ADC1, ADC input chnl	TIM0_ICAP2, Input Capture	GPIO_4.1, GP Output	TIM0_OCMP2, Out comp	ETM_PCK1, ETM Packet
2	1	A1	P4.2	I/O	GPIO_4.2, GP Input, HiZ	ADC2, ADC input chnl	TIM1_ICAP1, Input Capture	GPIO_4.2, GP Output	TIM1_OCMP1, Out comp/PWM	ETM_PCK2, ETM Packet
1	128	B3	P4.3	I/O	GPIO_4.3, GP Input, HiZ	ADC3, ADC input chnl	TIM1_ICAP2, Input Capture	GPIO_4.3, GP Output	TIM1_OCMP2, Out comp	ETM_PCK3, ETM Packet
80	127	C4	P4.4	I/O	GPIO_4.4, GP Input, HiZ	ADC4, ADC input chnl	TIM2_ICAP1, Input Capture	GPIO_4.4, GP Output	TIM2_OCMP1, Out comp/PWM	ETM_PSTAT0, ETM pipe status
79	126	B4	P4.5	I/O	GPIO_4.5, GP Input, HiZ	ADC5, ADC input chnl	TIM2_ICAP2, Input Capture	GPIO_4.5, GP Output	TIM2_OCMP2, Out comp	ETM_PSTAT1, ETM pipe status
78	125	A4	P4.6	I/O	GPIO_4.6, GP Input, HiZ	ADC6, ADC input chnl	TIM3_ICAP1, Input Capture	GPIO_4.6, GP Output	TIM3_OCMP1, Out comp/PWM	ETM_PSTAT2, ETM pipe status
77	124	D5	P4.7	I/O	GPIO_4.7, GP Input, HiZ	ADC7, ADC input chnl /ADC Ext. trigger	TIM3_ICAP2, Input Capture	GPIO_4.7, GP Output	TIM3_OCMP2, Out comp	ETM_TRSYNC, ETM trace sync
9	12	E4	P5.0	I/0	GPIO_5.0, GP Input, HiZ	EXINT8, External Intr	CAN_RX, CAN rcv data	GPIO_5.0, GP Output	ETM_TRCLK, ETM trace clock	UART0_TX, UART xmit data

Table 8. Device pin description (continued)

Package			Pin name	Signal type	Default pin function	Default input function	Alternate functions			
LQFP80	LQFP128	LFBGA144					Alternate input 1	Alternate output 1	Alternate output 2	Alternate output 3
27	42	M5	X1_RTC	I	RTC oscillator or crystal input (32.768 kHz)	N/A				
26	41	M4	X2_RTC	O	RTC crystal connection	N/A				
61	97	B11	JRTCK	O	JTAG return clock or RTC clock	N/A				
67	107	D8	JTRSTn	I	JTAG TAP controller reset	N/A				
68	108	E8	JTCK	I	JTAG clock	N/A				
69	111	A6	JTMS	I	JTAG mode select	N/A				
72	115	C6	JTDI	I	JTAG data in	N/A				
73	117	B6	JTDO	O	JTAG data out	N/A				
-	122	A3	AVDD	V	ADC analog voltage source, 2.7 V - 3.6 V	N/A				
-	4	C3	AVSS	G	ADC analog ground	N/A				
5	-	-	AVSS_ VSSQ	G	Common ground point for digital I/O & analog ADC	N/A				
-	123	A2	AVREF	V	ADC reference voltage input	N/A				
76	-	-	AVREF_ AVDD	V	Combined ADC ref voltage and ADC analog voltage source, 2.7 V - 3.6 V	N/A				
24	39	M3	VBATT	V	Standby voltage input for RTC and SRAM backup	N/A				
6	9	E1	VDDQ	V	V Source for I/O and USB. 2.7 V to 3.6 V	N/A				
15	23	J1	VDDQ	V						
36	57	-	VDDQ	V						
46	73	K12	VDDQ	V						
54	86	B5	VDDQ	V						
28	43	L5	VDDQ	V						
63	102	H7	VDDQ	V						
74	120	D9	VDDQ	V						
-	-	F9	VDDQ	V						

6 Memory mapping

The ARM966E-S CPU addresses a single linear address space of 4 giga-bytes (2^{32}) from address 0x0000.0000 to 0xFFFF.FFFF as shown in *Figure 9*. Upon reset the CPU boots from address 0x0000.0000, which is chip-select zero at address zero in the Flash Memory Interface (FMI).

The Instruction TCM and Data TCM enable high-speed CPU operation without incurring any performance or power penalties associated with accessing the system buses (AHB and APB). I-TCM and D-TCM address ranges are shown at the bottom of the memory map in *Figure 9*.

6.1 Buffered and non-buffered writes

The CPU makes use of write buffers on the AHB and the D-TCM to decouple the CPU from any wait states associated with a write operation. The user may choose to use write with buffers on the AHB by setting bit 3 in control register CP15 and selecting the appropriate AHB address range when writing. By default at reset, buffered writes are disabled (bit 3 of CP15 is clear) and all AHB writes are non-buffered until enabled. *Figure 9* shows that most addressable items on the AHB are aliased at two address ranges, one for buffered writes and another for non-buffered writes. A buffered write will allow the CPU to continue program execution while the write-back is performed through a FIFO to the final destination on the AHB. If the FIFO is full, the CPU is stalled until FIFO space is available. A non-buffered write will impose an immediate delay to the CPU, but results in a direct write to the final AHB destination, ensuring data coherency. Read operations from AHB locations are always direct and never buffered.

6.2 System (AHB) and peripheral (APB) buses

The CPU will access SRAM, higher-speed peripherals (USB, Ethernet, Programmable DMA), and the external bus (EMI) on the AHB at their respective base addresses indicated in *Figure 9*. Lower-speed peripherals reside on the APB and are accessed using two separate AHB-to-APB bridge units (APB0 and APB1). These bridge units are essentially address windows connecting the AHB to the APB. To access an individual APB peripheral, the CPU will place an address on the AHB bus equal to the base address of the appropriate bridge unit APB0 or APB1, plus the offset of the particular peripheral, plus the offset of the individual data location within the peripheral. *Figure 9* shows the base addresses of bridge units APB0 and APB1, and also the base address of each APB peripheral. Please consult the STR91xFA Reference manual for the address of data locations within each individual peripheral.

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$max (given by the selected temperature range).

Data based on product characterisation, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25° C, V_{DDQ} = 3.3 V and V_{DD}=1.8 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

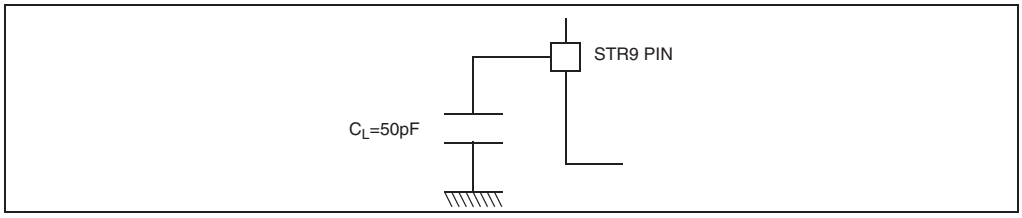
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

Figure 10. Pin loading conditions



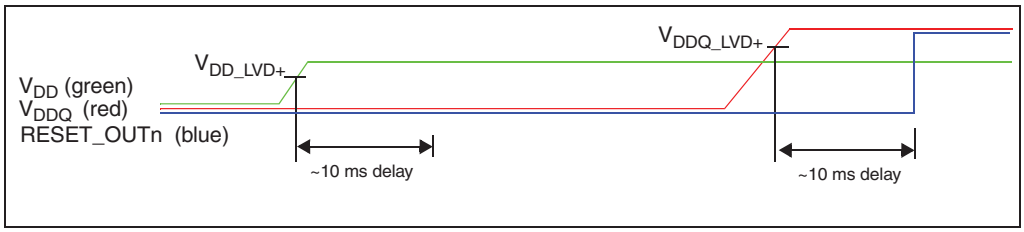
7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

7.5.1 LVD delay timing

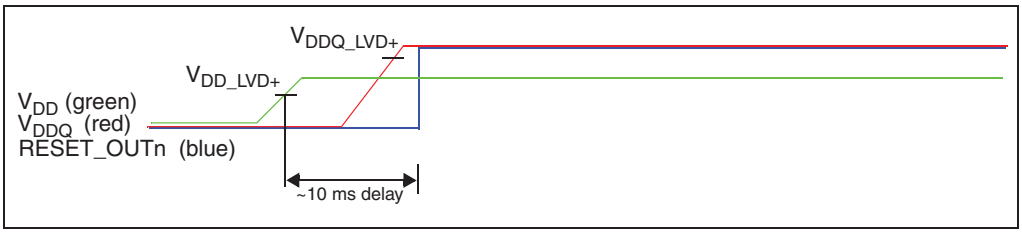
Case 1: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **after** the first ~10 ms delay (introduced by the VDD rising edge), a new ~10 ms delay starts before the release of RESET_OUTn. See *Figure 12.*

Figure 12. LVD reset delay case 1



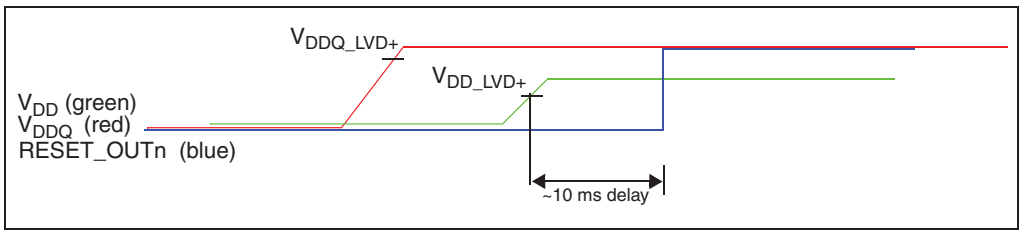
Case 2: When V_{DDQ} reaches the V_{DDQ_LVD+} threshold **before** the first ~10 ms delay (introduced by the VDD rising edge), RESET_OUTn will be released immediately at the end of the delay. No new delay is introduced in this case. See *Figure 13.*

Figure 13. LVD reset delay case 2



Case 3: When V_{DD} reaches the V_{DD_LVD+} threshold **after** the V_{DDQ} rising edge, RESET_OUTn will be released at the end of a ~10 ms delay. See *Figure 14*

Figure 14. LVD reset delay case 3



7.6 Supply current characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 15. Supply current characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
I_{DDRUN}	Run mode current	All peripherals on(1)(2)		1.7	2.3	mA/MHz
		All peripherals off(1)(2)		1.3	1.6	
I_{IDLE}	Idle mode current	All peripherals on (2)(3)		1.14	1.7	mA/MHz
		All peripherals off(2)(4)		0.45	0.75	mA/MHz
$I_{SLEEP(IDD)}$	Sleep mode current, I_{DD}	ARM core and all peripheral clocks stopped (with exception of RTC), LVD off		50	820(5)	µA
		ARM core and all peripheral clocks stopped (with exception of RTC), LVD on		55	825(5)	
$I_{SLEEP(IDDQ)}$	Sleep mode current, I_{DDQ}	LVD On (4)		7	80(5)	µA
		LVD Off (4)		7	70(5)	µA
I_{RTC_STBY}	RTC Standby current	Measured on VBATT pin		0.9	1.2	µA
I_{SRAM_STBY}	SRAM Standby current	Measured on VBATT pin		5	240	µA

1. ARM core and peripherals active with all clocks on. Power can be conserved by turning off clocks to peripherals which are not required.
2. mA/MHz data valid down to 10 MHz. Below this frequency the ratio mA/MHz increases.
3. ARM core stopped and all peripheral clocks active.
4. ARM core stopped and all peripheral clocks stopped.
5. Results based on characterization, not tested in production.

Page mode read

Figure 22. Page mode read diagram

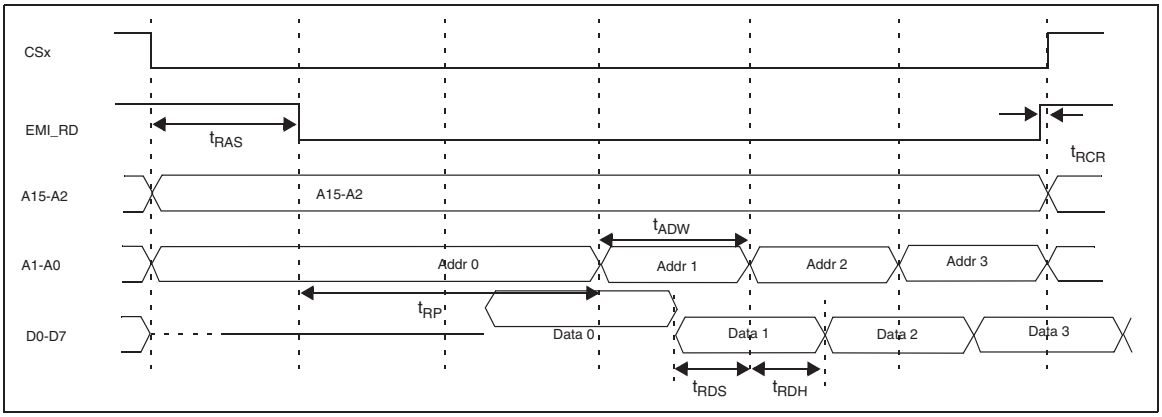


Table 37. Page mode read times

Symbol	Parameter	Value	
		Min	Max
t_{RDH}	Read data hold time	0	
t_{RDS}	Read data setup time	12 ns	-
t_{ADW}	ALE pulse width	(t_{BCLK}) - 1.5 ns	(t_{BCLK})+ 0.5 ns
t_{RAS}	Read address setup time	((WSTOEN) x t_{BCLK})	((WSTOEN) x t_{BCLK}) + 2.5 ns
t_{RP}	Read pulse width	((WSTRD-WSTOEN+1) x t_{BCLK})	((WSTRD-WSTOEN+1) x t_{BCLK}) + 2 ns
t_{RCR}	Read to CSn inactive	0	1 ns

Sync burst read

Figure 24. Sync burst read diagram

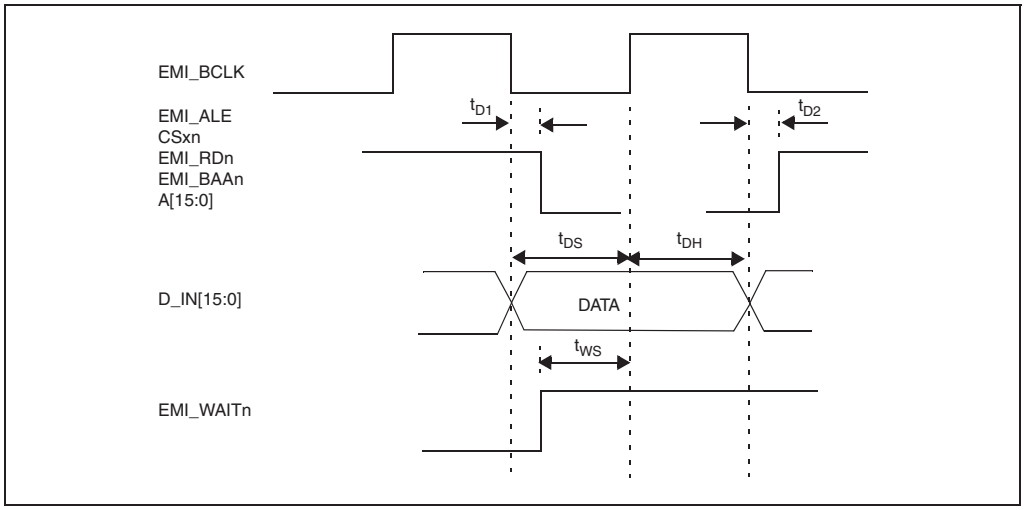


Table 39. Sync burst read times

Symbol	Parameter	Value	
		Min	Max
t_{D1BAA}	BAA t_{D1}	0 ns	2 ns
t_{D2BAA}	BAA t_{D2}	0.5ns	2.5 ns
t_{D1ALE}	ALE t_{D1}	1 ns	3.5 ns
t_{D2ALE}	ALE t_{D2}	$(t_{BCLK}/2)$+0.5 ns	$(t_{BCLK}/2)$+3 ns
t_{D1RD}	RD t_{D1}	0	2 ns
t_{D2RD}	RD t_{D2}	0.5 ns	2.5 ns
t_{D1A}	Address t_{D1}	2 ns	4 ns
t_{D2A}	Address t_{D2}	2.5 ns	3.5 ns
t_{D1CS}	CS t_{D1}	0.5 ns	3 ns
t_{D2CS}	CS t_{D2}	1 ns	3.5 ns
t_{WS}	WAIT set up time	1 ns	4 ns
t_{DS}	Data setup time	4.5 ns	-
t_{DH}	Data hold time	0	-

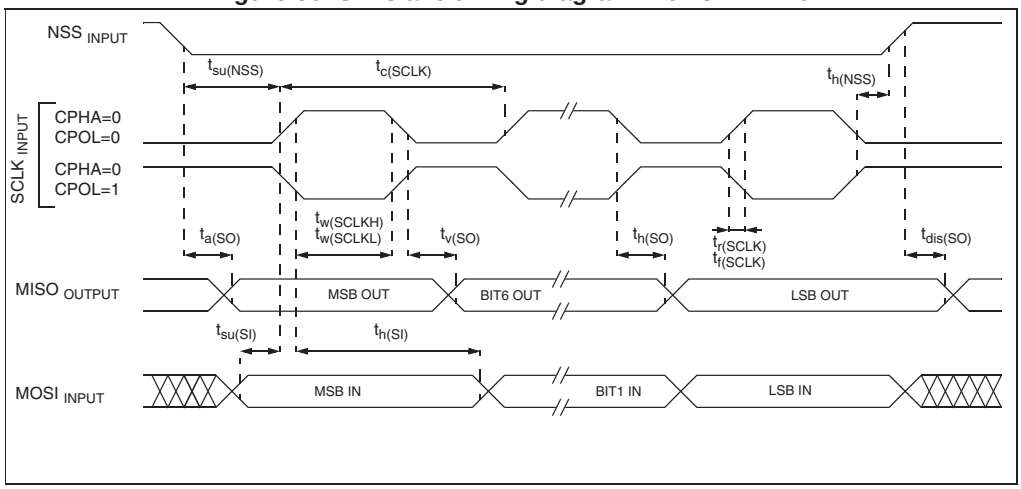
7.12.5 SPI electrical characteristics

V_{DDQ} = 2.7 - 3.6 V, V_{DD} = 1.65 - 2 V, T_A = -40 / 85 °C unless otherwise specified.

Table 46. SPI electrical characteristics

Symbol	Parameter	Test conditions	Value		Unit
			Typ	Max	
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master		24	MHz
		Slave		4	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall times	50pF load	0.1		V/ns
$t_{su(SS)}$	SS setup time	Slave	1		t_{PCLK}
$t_{h(SS)}$	SS hold time	Slave	1		
$t_{w(SCLKH)}$ $t_{w(SCLKL)}$	SCLK high and low time	Master Slave	1		
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master Slave	TBD 5		
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master Slave	TBD 6		
$t_{a(SO)}$	Data output access time	Slave		6	
$t_{dis(SO)}$	Data output disable time	Slave		6	
$t_{v(SO)}$	Data output valid time	Slave (after enable edge)		6	
$t_{h(SO)}$	Data output hold time		0		
$t_{v(MO)}$	Data output valid time	Master (before capture edge)	0.25		
$t_{h(MO)}$	Data output hold time		0.25		

Figure 30. SPI slave timing diagram with CPHA = 0



8 Device marking

8.1 STR91xFAx32 / STR91xFAx42 / STR91xFAx44

Figure 34. Device marking for revision G LQFP80 and LQFP128 packages

Figure 35. Device marking for revision G LFBGA144 packages

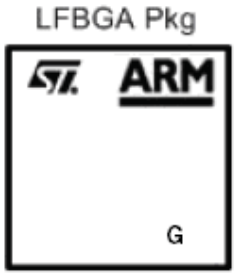


Figure 36. Device marking for revision H LQFP80 and LQFP128 packages

Figure 37. Device marking for revision H LFBGA144 packages

9.1 ECOPACK

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions, and product status are available at *www.st.com*.

9.2 Thermal characteristics

The average chip-junction temperature, T_J must never exceed 125 °C.

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the power dissipation on input and output pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories. The worst case P_{INT} of the STR91xFA is 500 mW ($I_{DD} \times V_{DD}$, or 250 mA x 2.0 V).

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 53. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	***Thermal resistance junction-ambient*** LQFP 80 - 12 x 12 mm / 0.5 mm pitch	41.5	°C/W
Θ_{JA}	***Thermal resistance junction-ambient*** LQFP128 - 14 x 14 mm / 0.4 mm pitch	38	°C/W
Θ_{JA}	***Thermal resistance junction-ambient*** LFBGA 144 - 10 x 10 x 1.7 mm	36.5	°C/W