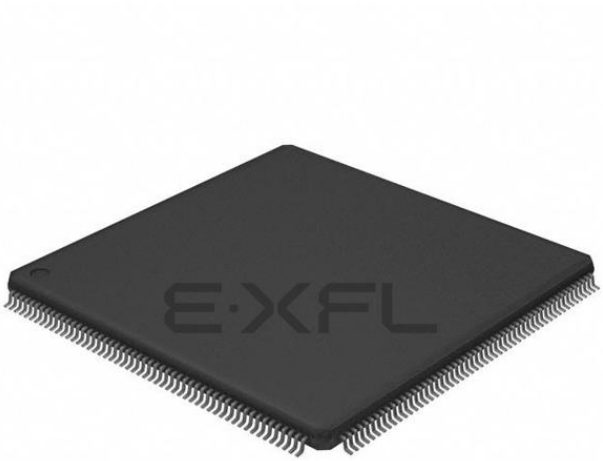


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4/M0 |
| Core Size | 32-Bit Dual-Core |
| Speed | 204MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, QEI, SPI, SSI, SSP, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, WDT |
| Number of I/O | 142 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 136K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 3.6V |
| Data Converters | A/D 8x10b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-LQFP |
| Supplier Device Package | 208-LQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc43s57jbd208e |

- External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
- LCD controller with DMA support and a programmable display resolution of up to 1024 H × 768 V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping. Available on parts LPC4357/53 only.
- Secure Digital Input Output (SD/MMC) card interface.
- Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
- Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
- GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
- Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
- Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- Four general-purpose timer/counters with capture and match capabilities.
- One motor control Pulse Width Modulator (PWM) for three-phase motor control.
- One Quadrature Encoder Interface (QEI).
- Repetitive Interrupt timer (RI timer).
- Windowed watchdog timer (WWDT).
- Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
- Alarm timer; can be battery powered.

- Analog peripherals
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Clock generation unit
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC oscillator trimmed to 3 % accuracy over temperature and voltage (1.5 % accuracy for $T_{amb}$ = 0 °C to 85 °C).
  - Ultra-low power Real-Time Clock (RTC) crystal oscillator.
  - Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL can be used with the High-speed USB, the third PLL can be used as audio PLL.
  - Clock output.
- Power
  - Single 3.3 V (2.4 V to 3.6 V) power supply with on-chip DC-to-DC converter for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_1 | R2 | K2 | 58 | 42 | [2] | N; PU | I/O | **GPIO0[8] —** General purpose digital input/output pin. Boot pin (see Table 5). |
| | | | | | | | O | **CTOUT_7 —** SCT output 7. Match output 3 of timer 1. |
| | | | | | | | I/O | **EMC_A6 —** External memory address line 6. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP0_MISO —** Master In Slave Out for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_D13 —** External memory data line 13. |
| P1_2 | R3 | K1 | 60 | 43 | [2] | N; PU | I/O | **GPIO0[9] —** General purpose digital input/output pin. Boot pin (see Table 5). |
| | | | | | | | O | **CTOUT_6 —** SCT output 6. Match output 2 of timer 1. |
| | | | | | | | I/O | **EMC_A7 —** External memory address line 7. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_D14 —** External memory data line 14. |
| P1_3 | P5 | J1 | 61 | 44 | [2] | N; PU | I/O | **GPIO0[10] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_8 —** SCT output 8. Match output 0 of timer 2. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |
| | | | | | | | O | **EMC_OE —** LOW active Output Enable signal. |
| | | | | | | | O | **USB0_IND1 —** USB0 port indicator LED control output 1. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **SD_RST —** SD/MMC reset signal for MMC4.4 card. |
| P1_4 | T3 | J2 | 64 | 47 | [2] | N; PU | I/O | **GPIO0[11] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_9 —** SCT output 9. Match output 3 of timer 3. |
| | | | | | | | I/O | **SGPIO11 —** General purpose digital input/output pin. |
| | | | | | | | O | **EMC_BLS0 —** LOW active Byte Lane select signal 0. |
| | | | | | | | O | **USB0_IND0 —** USB0 port indicator LED control output 0. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave in for SSP1. |
| | | | | | | | I/O | **EMC_D15 —** External memory data line 15. |
| | | | | | | | O | **SD_VOLT1 —** SD/MMC bus voltage select output 1. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_20 | M10 | K10 | 100 | 70 | [2] | N; PU | I/O | **GPIO0[15] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface). |
| | | | | | | | I | **T0_CAP2 —** Capture input 2 of timer 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D11 —** External memory data line 11. |
| P2_0 | T16 | G10 | 108 | 75 | [2] | N; PU | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| | | | | | | | O | **U0_TXD —** Transmitter output for USART0. See Table 4 for ISP mode. |
| | | | | | | | I/O | **EMC_A13 —** External memory address line 13. |
| | | | | | | | O | **USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH).<br>Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts. |
| | | | | | | | I/O | **GPIO5[0] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP0 —** Capture input 0 of timer 3. |
| | | | | | | | O | **ENET_MDC —** Ethernet MIIM clock. |
| P2_1 | N15 | G7 | 116 | 81 | [2] | N; PU | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| | | | | | | | I | **U0_RXD —** Receiver input for USART0. See Table 4 for ISP mode. |
| | | | | | | | I/O | **EMC_A12 —** External memory address line 12. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |
| | | | | | | | I/O | **GPIO5[1] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP1 —** Capture input 1 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P4_7 | H4 | - | 21 | 14 | [2] | O; PU | O | **LCD_DCLK —** LCD panel clock. |
| | | | | | | | I | **GP_CLKIN —** General purpose clock input to the CGU. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |
| | | | | | | | I/O | **I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |
| P4_8 | E2 | - | 23 | 15 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_5 —** SCT input 5. Capture input 2 of timer 2. |
| | | | | | | | O | **LCD_VD9 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **LCD_VD22 —** LCD data. |
| | | | | | | | O | **CAN1_TD —** CAN1 transmitter output. |
| | | | | | | | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| P4_9 | L2 | - | 48 | 33 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_6 —** SCT input 6. Capture input 1 of timer 3. |
| | | | | | | | O | **LCD_VD11 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[13] —** General purpose digital input/output pin. |
| | | | | | | | O | **LCD_VD15 —** LCD data. |
| | | | | | | | I | **CAN1_RD —** CAN1 receiver input. |
| | | | | | | | I/O | **SGPIO14 —** General purpose digital input/output pin. |
| P4_10 | M3 | - | 51 | 35 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_2 —** SCT input 2. Capture input 2 of timer 0. |
| | | | | | | | O | **LCD_VD10 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **LCD_VD14 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO15 —** General purpose digital input/output pin. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P7_6 | C7 | - | 194 | 134 | [2] | N; PU | I/O | **GPIO3[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_11 —** SCT output 1. Match output 3 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **TRACEDATA[2] —** Trace data, bit 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P7_7 | B6 | - | 201 | 140 | [5] | N; PU | I/O | **GPIO3[15] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_8 —** SCT output 8. Match output 0 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_PWR —** LCD panel power enable. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **TRACEDATA[3] —** Trace data, bit 3. |
| | | | | | | | O | **ENET_MDC —** Ethernet MIIM clock. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | AI | **ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| P8_0 | E5 | - | 2 | - | [3] | N; PU | I/O | **GPIO4[0] —** General purpose digital input/output pin. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **MCI2 —** Motor control PWM channel 2, input. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT0 —** Match output 0 of timer 0. |
| P8_1 | H5 | - | 34 | - | [3] | N; PU | I/O | **GPIO4[1] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_IND1 —** USB0 port indicator LED control output 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **MCI1 —** Motor control PWM channel 1, input. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT1 —** Match output 1 of timer 0. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P8_6 | K3 | - | 43 | - | [2] | N; PU | I/O | **GPIO4[6] —** General purpose digital input/output pin. |
| | | | | | | | I | **USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD5 —** LCD data. |
| | | | | | | | O | **LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP2 —** Capture input 2 of timer 0. |
| P8_7 | K1 | - | 45 | - | [2] | N; PU | I/O | **GPIO4[7] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD4 —** LCD data. |
| | | | | | | | O | **LCD_PWR —** LCD panel power enable. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP3 —** Capture input 3 of timer 0. |
| P8_8 | L1 | - | 49 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CGU_OUT0 —** CGU spare clock output 0. |
| | | | | | | | O | **I2S1_TX_MCLK —** I2S1 transmit master clock. |
| P9_0 | T1 | - | 59 | - | [2] | N; PU | I/O | **GPIO4[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_CRS —** Ethernet Carrier Sense (MII interface). |
| | | | | | | | I/O | **SGPIO0 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PD_3 | P4 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_6 —** SCT output 7. Match output 2 of timer 1. |
| | | | | | | | I/O | **EMC_D17 —** External memory data line 17. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[17] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| PD_4 | T2 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_8 —** SCT output 8. Match output 0 of timer 2. |
| | | | | | | | I/O | **EMC_D18 —** External memory data line 18. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[18] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| PD_5 | P6 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_9 —** SCT output 9. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D19 —** External memory data line 19. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[19] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| PD_6 | R6 | - | 68 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_10 —** SCT output 10. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D20 —** External memory data line 20. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[20] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PF_2 | D11 | - | 168 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **U3_TXD —** Transmitter output for USART3. |
| | | | | | | | I/O | **SSP0_MISO —** Master In Slave Out for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[17] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO1 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| PF_3 | E10 | - | 170 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[18] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO2 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| PF_4 | D10 | H4 | 172 | 120 | [2] | O; PU | I/O | **SSP1_SCK —** Serial clock for SSP1. |
| | | | | | | | I | **GP_CLKIN —** General purpose clock input to the CGU. |
| | | | | | | | O | **TRACECLK —** Trace clock. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S0_TX_MCLK —** I2S transmit master clock. |
| | | | | | | | I/O | **I2S0_RX_SCK —** I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| PF_5 | E9 | - | 190 | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_UCLK —** Serial clock input/output for USART3 in synchronous mode. |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| | | | | | | | O | **TRACEDATA[0] —** Trace data, bit 0. |
| | | | | | | | I/O | **GPIO7[19] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC1_4 —** ADC1 and ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PF_6 | E7 | - | 192 | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | O | **TRACEDATA[1] —** Trace data, bit 1. |
| | | | | | | | I/O | **GPIO7[20] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | | | | | | AI | **ADC1_3 —** ADC1 and ADC0, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_7 | B7 | - | 193 | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_BAUD —** Baud pin for USART3. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave in for SSP1. |
| | | | | | | | O | **TRACEDATA[2] —** Trace data, bit 2. |
| | | | | | | | I/O | **GPIO7[21] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | AI/O | **ADC1_7 —** ADC1 and ADC0, input channel 7 or band gap output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_8 | E6 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U0_UCLK —** Serial clock input/output for USART0 in synchronous mode. |
| | | | | | | | I | **CTIN_2 —** SCT input 2. Capture input 2 of timer 0. |
| | | | | | | | O | **TRACEDATA[3] —** Trace data, bit 3. |
| | | | | | | | I/O | **GPIO7[22] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC0_2 —** ADC0 and ADC1, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| VSS | G9, H7, J10, J11, K8 | C8, D4, D5, G8, J3, J6 | - | - | [13] | - | - | Ground. |
| VSSIO | C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13 | - | 5, 56, 109, 157 | 4, 40, 76, 109 | [13] | - | - | Ground. |
| VSSA | B2 | C2 | 196 | 135 | | - | - | Analog ground. |

[1] N = neutral, input buffer disabled; no extra VDDIO current consumption if the input is driven midway between supplies; set the EZI bit in the SFS register to enable the input buffer; I = input, OL = output driving LOW; OH = output driving HIGH; AI/O = analog input/output; IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to VDDIO; F = floating. Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[3] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels, and hysteresis; high drive strength.

[4] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides high-speed digital I/O functions with TTL levels and hysteresis.

[5] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input or output (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V). When configured as a ADC input or DAC output, the pin is not 5 V tolerant and the digital section of the pad must be disabled by setting the pin to an input function and disabling the pull-up resistor through the pin's SFSP register.

[6] 5 V tolerant transparent analog pad.

[7] For maximum load $C_L$ = 6.5 μF and maximum resistance $R_{pd}$ = 80 kΩ, the VBUS signal takes about 2 s to fall from VBUS = 5 V to VBUS = 0.2 V when it is no longer driven.

[8] Transparent analog pad. Not 5 V tolerant.

[9] Pad provides USB functions; 5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only).

[10] Open-drain 5 V tolerant digital I/O pad, compatible with I2C-bus Fast Mode Plus specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I2C-bus is floating and does not disturb the I2C lines.

[11] 5 V tolerant pad with 20 ns glitch filter; provides digital I/O functions with open-drain output and hysteresis.

[12] On the LQFP208, VPP is internally connected to VDDIO.

[13] On the LQFP208 package, VSSIO and VSS are connected to a common ground plane.

# 7. Functional description

## 7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-CODE bus, and the D-code bus. The I-CODE and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC43S5x/S3x use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

An ARM Cortex-M0 co-processor is included in the LPC43S5x/S3x, capable of off-loading the main ARM Cortex-M4 application processor. Most peripheral interrupts are connected to both processors. The processors communicate with each other via an interprocessor communication protocol.

## 7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core. The processor includes a NVIC with up to 53 interrupts.

## 7.3 ARM Cortex-M0 co-processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M0 co-processor uses a 3-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The co-processor incorporates a NVIC with 32 interrupts.

## 7.4 Interprocessor communication

The ARM Cortex-M4 and ARM Cortex-M0 interprocessor communication is based on using shared SRAM as mailbox and one processor raising an interrupt on the other processor's NVIC, for example after it has delivered a new message in the mailbox. The receiving processor can reply by raising an interrupt on the sending processor's NVIC to acknowledge the message.

Several boot modes are available if P2_7 is LOW on reset depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the boot mode is determined by the states of the boot pins P2_9, P2_8, P1_2, and P1_1.

**Table 4. Boot mode when OTP BOOT_SRC bits are programmed**

| Boot mode | BOOT_SRC bit 3 | BOOT_SRC bit 2 | BOOT_SRC bit 1 | BOOT_SRC bit 0 | Description |
|---|---|---|---|---|---|
| Pin state | 0 | 0 | 0 | 0 | Boot source is defined by the reset state of P1_1, P1_2, P2_8 pins, and P2_9. See Table 5. |
| USART0 | 0 | 0 | 0 | 1 | Enter ISP mode using USART0 pins P2_0 and P2_1. |
| SPIFI | 0 | 0 | 1 | 0 | Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8. |
| EMC 8-bit | 0 | 0 | 1 | 1 | Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus. |
| EMC 16-bit | 0 | 1 | 0 | 0 | Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus. |
| EMC 32-bit | 0 | 1 | 0 | 1 | Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus. |
| USB0 | 0 | 1 | 1 | 0 | Boot from USB0. |
| USB1 | 0 | 1 | 1 | 1 | Boot from USB1. |
| SPI (SSP) | 1 | 0 | 0 | 0 | Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1]. |
| USART3 | 1 | 0 | 0 | 1 | Enter ISP mode using USART3 pins P2_3 and P2_4. |

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
**Remark:** Pin functions for SPIFI and SSP0 boot are different.

**Table 5. Boot mode when OPT BOOT_SRC bits are zero**

| Boot mode | Pins | | | | Description |
|---|---|---|---|---|---|
| | P2_9 | P2_8 | P1_2 | P1_1 | |
| USART0 | LOW | LOW | LOW | LOW | Enter ISP mode using USART0 pins P2_0 and P2_1. |
| SPIFI | LOW | LOW | LOW | HIGH | Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1]. |
| EMC 8-bit | LOW | LOW | HIGH | LOW | Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus. |
| EMC 16-bit | LOW | LOW | HIGH | HIGH | Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus. |
| EMC 32-bit | LOW | HIGH | LOW | LOW | Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus. |
| USB0 | LOW | HIGH | LOW | HIGH | Boot from USB0 |

**Table 6. EMC pinout for different packages**

| Function | LBGA256 | TFBGA100 | LQFP208 | LQFP144 |
|---|---|---|---|---|
| $\overline{DYCS}$ | $\overline{EMC\_DYCS[3:0]}$ | $\overline{EMC\_DYCS[1:0]}$ | $\overline{EMC\_DYCS[2:0]}$ | $\overline{EMC\_DYCS[1:0]}$ |
| $\overline{CAS}$ | $\overline{EMC\_CAS}$ | $\overline{EMC\_CAS}$ | $\overline{EMC\_CAS}$ | $\overline{EMC\_CAS}$ |
| $\overline{RAS}$ | $\overline{EMC\_RAS}$ | $\overline{EMC\_RAS}$ | $\overline{EMC\_RAS}$ | $\overline{EMC\_RAS}$ |

#### 7.18.5.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

**Note:** Synchronous static memory devices (synchronous burst mode) are not supported.

### 7.18.6 High-speed USB Host/Device/OTG interface (USB0)

**Remark:** USB0 is available on the following parts: LPC435x, LPC433x, LPC432x. USB0 is not available on the LPC431x parts.

The USB OTG module allows the LPC43S5x/S3x to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

#### 7.18.6.1 Features

- Contains UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.

- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

### 7.21.2 Digital-to-Analog Converter (DAC)

#### 7.21.2.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

## 7.22 Peripherals in the RTC power domain

### 7.22.1 RTC

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

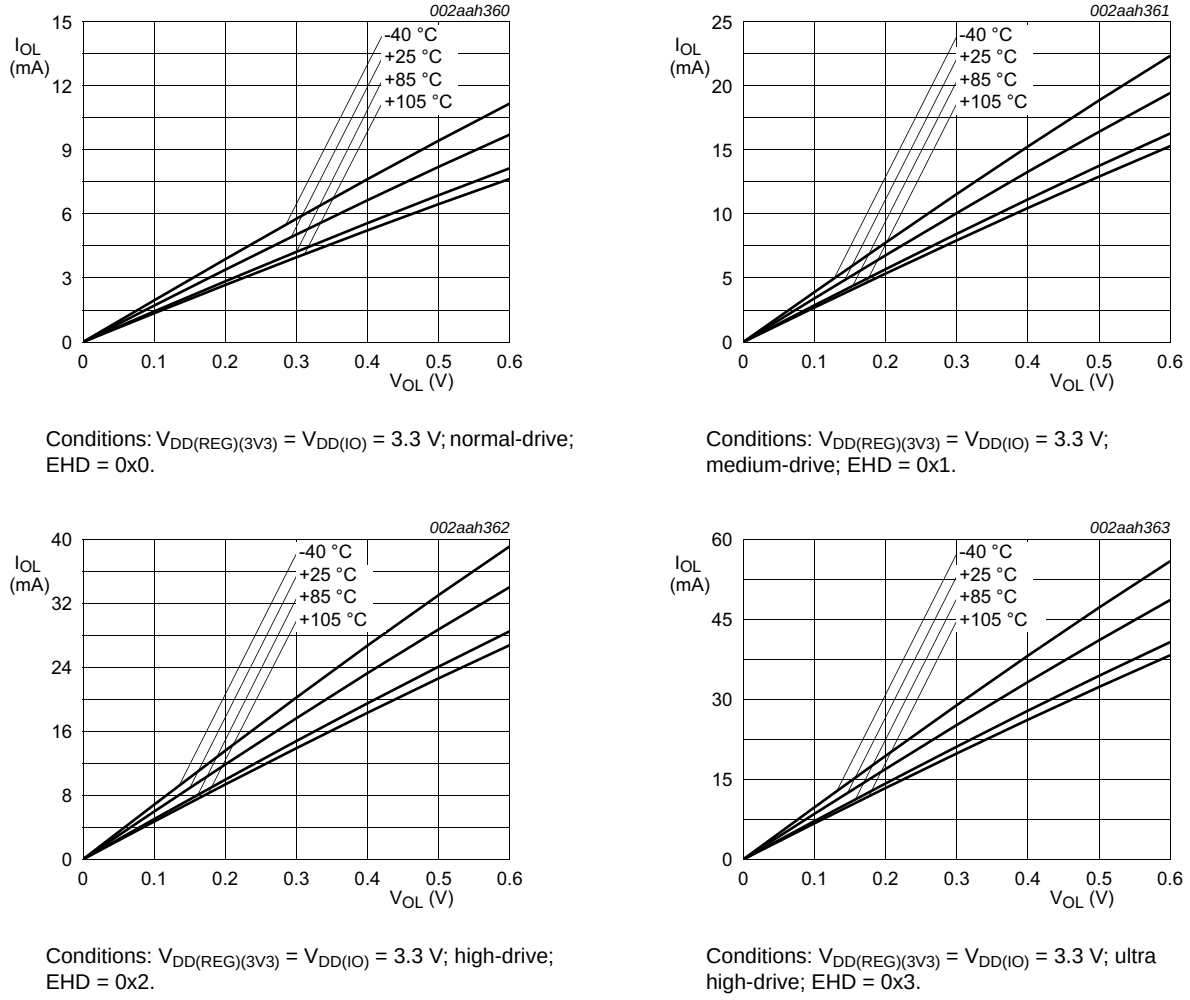
#### 7.22.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

#### 7.22.1.2 Event monitor/recorder

The event monitor/recorder allows recording and creating a time stamp of events related to the WAKEUP pins. Sensors report changes to the state of the WAKEUP pins, and the event monitor/recorder stores records of such events. The event recorder can be powered by the backup battery.

The event monitor/recorder can monitor the integrity of the device and record any tampering events.




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.

Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.

Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.

Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

**Fig 22. High-drive pins; typical LOW level output current $I_{OL}$ versus LOW level output voltage $V_{OL}$**

# 11. Dynamic characteristics

## 11.1 Flash/EEPROM memory

**Table 15. Flash characteristics**

*$T_{amb}$ = −40 °C to +105 °C, unless otherwise specified. $V_{DD(REG)(3V3)}$ = 2.4 V to 3.6 V for read operations; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V for erase/program operations.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $N_{endu}$ | endurance | sector erase/program | [1] | 10000 | - | - | cycles |
| | | page erase/program; page in large sector | | 1000 | - | - | cycles |
| | | page erase/program; page in small sector | | 10000 | - | - | cycles |
| $t_{ret}$ | retention time | powered | | 10 | - | - | years |
| | | unpowered | | 10 | - | - | years |
| $t_{er}$ | erase time | page, sector, or multiple consecutive sectors | | - | 100 | - | ms |
| $t_{prog}$ | programming time | | [2] | - | 1 | - | ms |

[1] Number of erase/program cycles.

[2] Programming times are given for writing 512 bytes from RAM to the flash. Data must be written to the flash in blocks of 512 bytes.

**Table 16. EEPROM characteristics**

*$T_{amb}$ = −40 °C to +105 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | | | 800 | 1500 | 1600 | kHz |
| $N_{endu}$ | endurance | | | 100 000 | - | - | cycles |
| $t_{ret}$ | retention time | $T_{amb}$ = −40 °C to +85 °C | | 20 | - | - | years |
| | | 85 °C < $T_{amb}$ ≤ 105 °C | | 10 | - | - | years |
| $t_a$ | access time | read | | - | 120 | - | ns |
| | | erase/program; $f_{clk}$ = 1500 kHz | | - | 1.99 | - | ms |
| | | erase/program; $f_{clk}$ = 1600 kHz | | - | 1.87 | - | ms |
| $t_{wait}$ | wait time | read; RPHASE1 | [1] | 70 | - | - | ns |
| | | read; RPHASE2 | [1] | 35 | - | - | ns |
| | | write; PHASE1 | [1] | 20 | - | - | ns |
| | | write; PHASE2 | [1] | 40 | - | - | ns |
| | | write; PHASE3 | [1] | 10 | - | - | ns |

[1] See the LPC43xx user manual how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx)

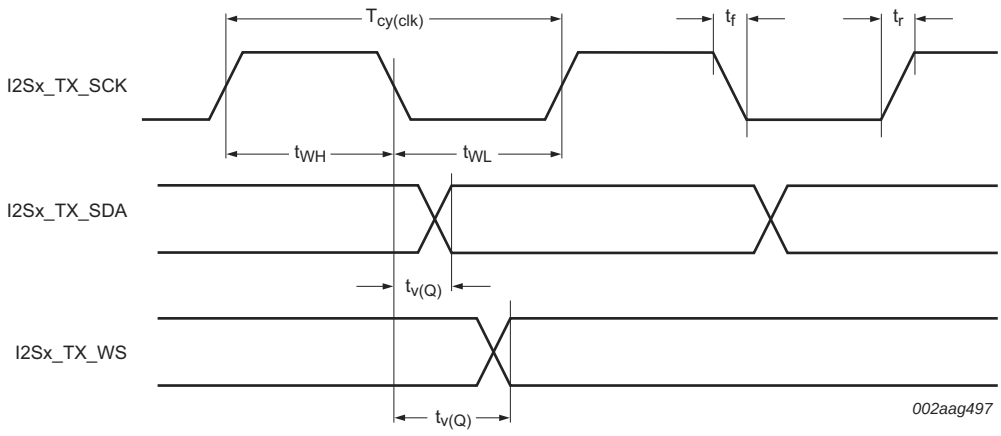



**Fig 28. I²S-bus timing (transmit)**

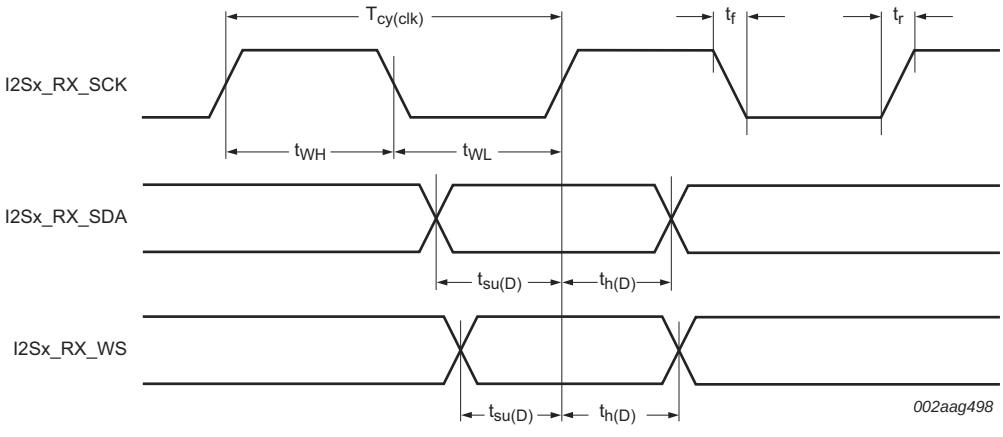



**Fig 29. I²S-bus timing (receive)**

## 11.11 USART interface

**Table 26. Dynamic characteristics: USART interface**

*$T_{amb}$ = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $T_{cy(clk)}$ | clock cycle time | on pins Ux_UCLK | | - | 0.1 | - | µs |
| **output** | | | | | | | |
| $t_{v(Q)}$ | data output valid time | on pin Ux_TXD | | - | 6.5 | - | ns |

**Table 45. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode**

| Fundamental oscillation frequency | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|
| 12 MHz | < 160 Ω | 18 pF, 18 pF |
| | < 160 Ω | 39 pF, 39 pF |
| 16 MHz | < 120 Ω | 18 pF, 18 pF |
| | < 80 Ω | 33 pF, 33 pF |
| 20 MHz | < 100 Ω | 18 pF, 18 pF |
| | < 80 Ω | 33 pF, 33 pF |

**Table 46. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode**

| Fundamental oscillation frequency | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|
| 15 MHz | < 80 Ω | 18 pF, 18 pF |
| 20 MHz | < 80 Ω | 39 pF, 39 pF |
| | < 100 Ω | 47 pF, 47 pF |

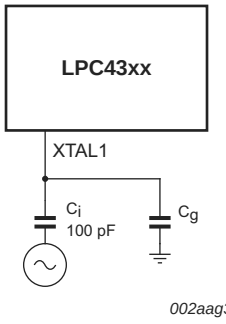



**Fig 43. Slave mode operation of the on-chip oscillator**

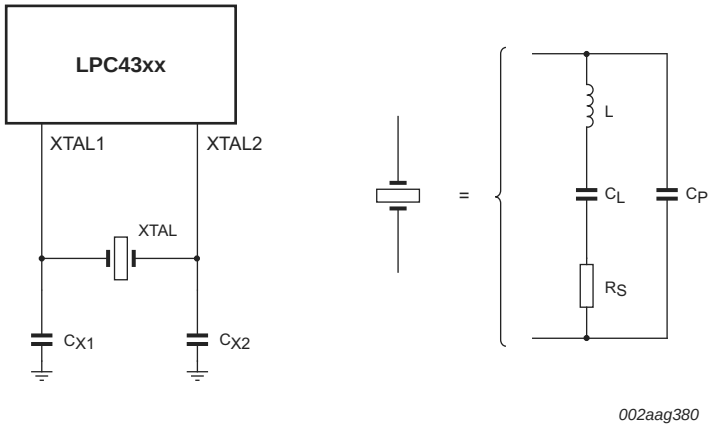
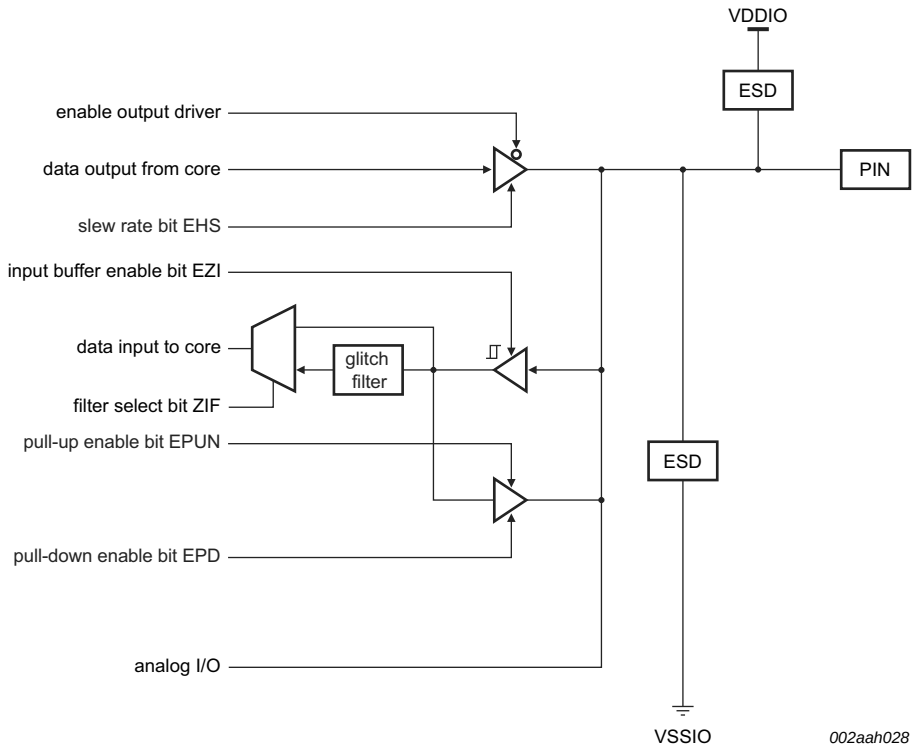



**Fig 44. Oscillator modes with external crystal model used for $C_{X1}$/$C_{X2}$ evaluation**




The glitch filter rejects pulses of typical 12 ns width.

**Fig 46. Standard I/O pin configuration with analog input**

### 13.5.1 Reset pin configuration

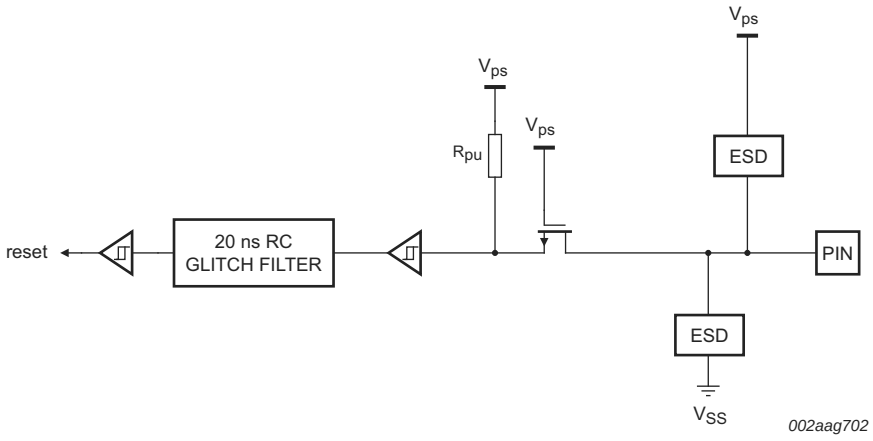



**Fig 47. Reset pin configuration**

### 13.5.2 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 48) or bus-powered device (see Figure 49).

On the LPC43S5x/S3x, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

VDDIO = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See Figure 49.

**Remark:** Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.

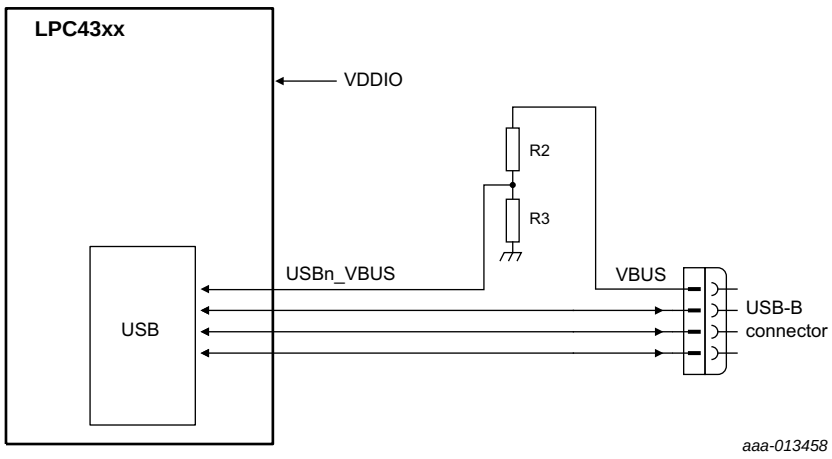



**Fig 48. USB interface on a self-powered device where USBn_VBUS = 5 V**