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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x16b; D/A 1x6b, 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl82z128vlk7r

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

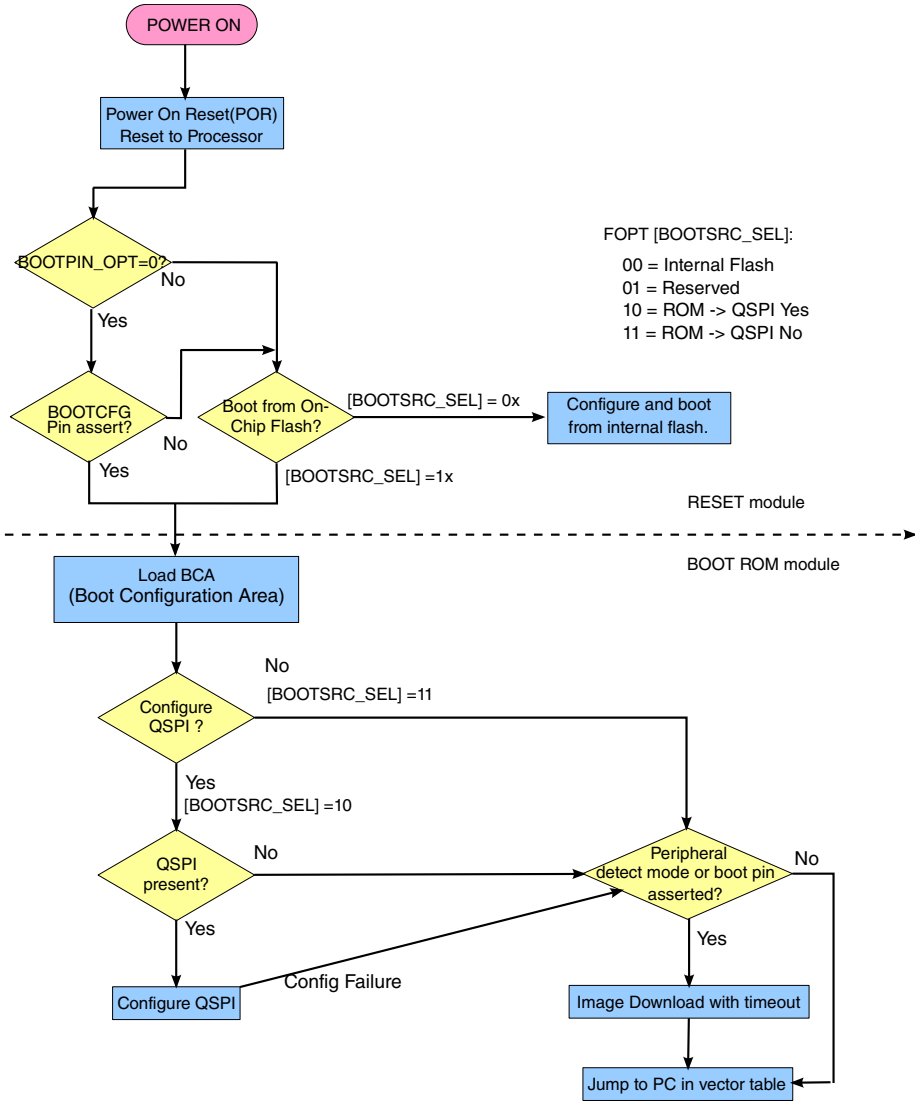
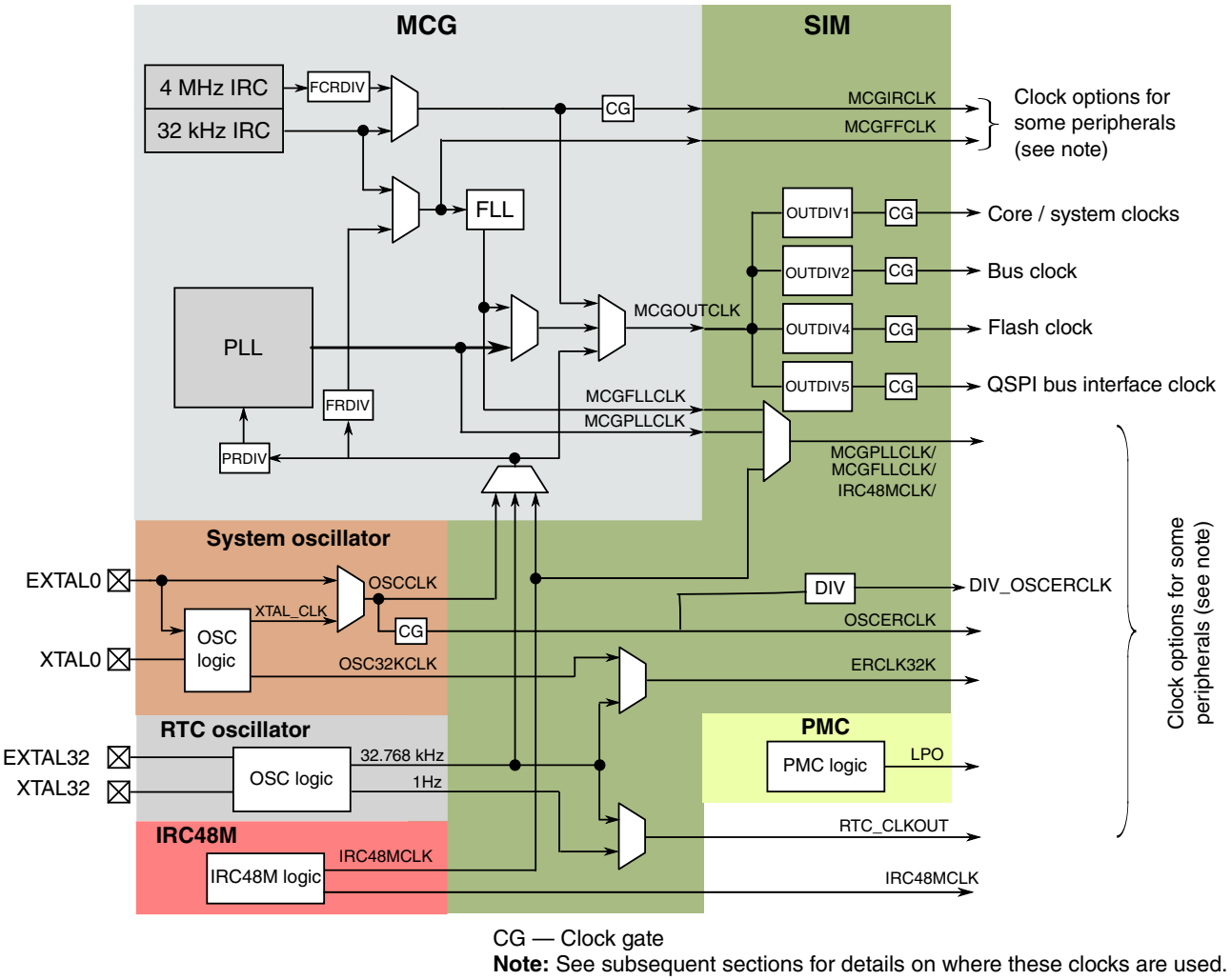


Figure 2. Boot Flow For Devices with QSPI

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

The phase-locked loop (PLL) can generate up to 144 MHz high speed, low jitter clock with 8–16 MHz internal or external reference clock. The PLL can be used as the system clock or clock source for other on-chip modules.

For more details on the clock operations and configurations, see Reference Manual.



CG — Clock gate
Note: See subsequent sections for details on where these clocks are used.

Figure 3. Clocking diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

2.2.7 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers. During chip power-down, RTC is powered from the backup power supply (VBAT), electrically isolated from the rest of the chip, continues to increment the time counter (if enabled) and retain the state of the RTC registers. The RTC registers are not accessible.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt
- 64-bit monotonic counter with roll-over protection

2.2.8 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has four independent channels and each channel has a 32-bit counter. Two channels can be chained together to form a 64-bit counter.

The PIT module can trigger a DMA transfer on the first four DMA channels. and also can be selected as ADC, TPM, and DAC trigger source.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.11 LPUART

This product contains three Low-Power UART modules, both of their clock sources are selectable fromIRC48M, MCGFLLCLK, MCGPLLCLK, MCGIRCCLK or external crystal clock, and can work in Stop and VLPS modes. They also support 4x to 32x data oversampling rate to meet different applications.

The LPUART module has the following features:

- Full-duplex, standard non-return-to-zero (NRZ) format

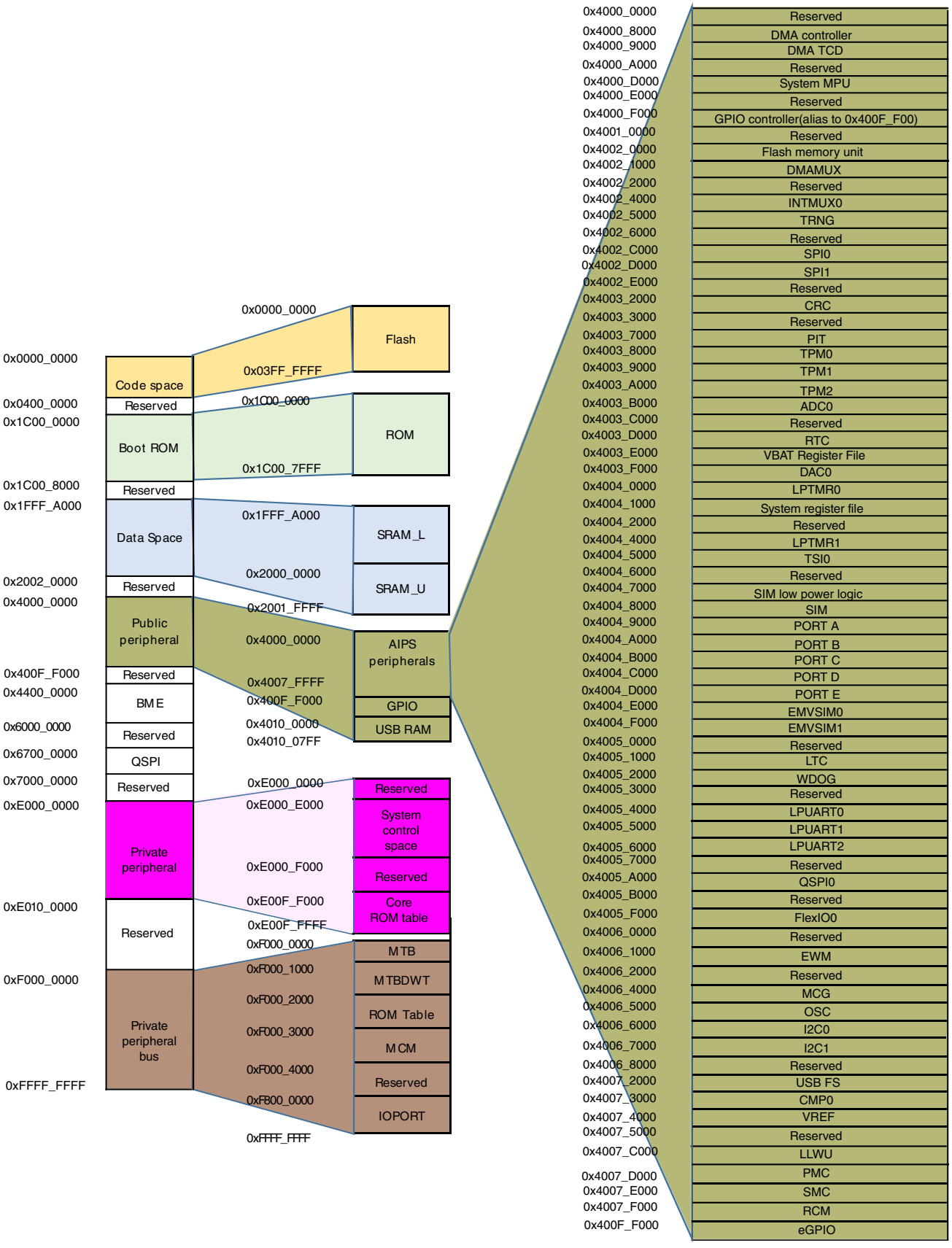


Figure 4. Memory map

121 MAP BGA	100 LQFP	80 LQFP	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
K8	42	—	—	—	PTA12	DISABLED		PTA12		TPM1_CH0		FXIO0_D18		
L8	43	—	—	—	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		TPM1_CH1		FXIO0_D19		
K9	44	34	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	LPUART0_ TX		FXIO0_D20		
L9	45	35	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	LPUART0_ RX		FXIO0_D21		
J10	46	36	—	—	PTA16	DISABLED		PTA16	SPI0_SOUT	LPUART0_ CTS_b		FXIO0_D22		
H10	47	37	—	—	PTA17	DISABLED		PTA17	SPI0_SIN	LPUART0_ RTS_b		FXIO0_D23		
E6	48	38	H7	30	VDD	VDD	VDD							
G7	49	39	G7	31	VSS	VSS	VSS							
L11	50	40	H8	32	PTA18	EXTAL0	EXTAL0	PTA18			TPM_ CLKIN0			
K11	51	41	G8	33	PTA19	XTAL0	XTAL0	PTA19			TPM_ CLKIN1		LPTMR0_ ALT1/ LPTMR1_ ALT1	
J11	52	42	F8	34	RESET_b	RESET_b	RESET_b							
H11	—	—	—	—	PTA29	DISABLED		PTA29						
G11	53	43	E6	35	PTB0/ LLWU_P5	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				FXIO0_D0
G10	54	44	—	—	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	TPM1_CH1				FXIO0_D1
G9	55	—	—	—	PTB2	ADC0_ SE12/ TSI0_CH7	ADC0_ SE12/ TSI0_CH7	PTB2	I2C0_SCL	LPUART0_ RTS_b				FXIO0_D2
G8	56	—	—	—	PTB3	ADC0_ SE13/ TSI0_CH8	ADC0_ SE13/ TSI0_CH8	PTB3	I2C0_SDA	LPUART0_ CTS_b				FXIO0_D3
B11	—	45	F7	36	PTB4	DISABLED		PTB4	EMVSIM1_ IO					
C11	—	46	F6	37	PTB5	DISABLED		PTB5	EMVSIM1_ CLK					
F11	—	47	E7	38	PTB6	DISABLED		PTB6	EMVSIM1_ VCCEN					
E11	—	48	E8	39	PTB7	DISABLED		PTB7	EMVSIM1_ PD					
D11	—	49	D7	40	PTB8	DISABLED		PTB8	EMVSIM1_ RST					
E10	57	—	—	—	PTB9	DISABLED		PTB9	SPI1_PCS1					
D10	58	—	—	—	PTB10	DISABLED		PTB10	SPI1_PCS0					FXIO0_D4
C10	59	50	—	—	PTB11	DISABLED		PTB11	SPI1_SCK					FXIO0_D5
L6	60	—	—	—	VSS	VSS	VSS							

121 MAPBGA	100 LQFP	80 LQFP	64 LQFP	64 MAPBGA	Pin Name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
E9	63	52			PTB17	ND	Hi-Z	—	FS	N	N	Y
D9	64	53	41	D6	PTB18	ND	Hi-Z	—	FS	N	N	Y
C9	65	54	42	C7	PTB19	ND	Hi-Z	—	FS	N	N	Y
F10	66				PTB20	ND	Hi-Z	—	FS	N	N	Y
F9	67				PTB21	ND	Hi-Z	—	FS	N	N	Y
F8	68				PTB22	ND	Hi-Z	—	FS	N	N	Y
E8	69				PTB23	ND	Hi-Z	—	FS	N	N	Y
B9	70	55	43	D8	PTC0	ND	Hi-Z	—	FS	N	N	Y
D8	71	56	44	C6	PTC1/LLWU_P6	ND	Hi-Z	—	FS	N	N	Y
C8	72	57	45	B7	PTC2	ND	Hi-Z	—	FS	N	N	Y
B8	73	58	46	C8	PTC3/LLWU_P7	ND	Hi-Z	—	FS	N	N	Y
	74	59	47	E3	VFS	—	—	—	—	—	—	—
	75	60	48	E4	VDD	—	—	—	—	—	—	—
A8	76	61	49	B8	PTC4/LLWU_P8	ND	Hi-Z	—	FS	N	N	Y
D7	77	62	50	A8	PTC5/LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
C7	78	63	51	A7	PTC6/LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
B7	79	64	52	B6	PTC7	ND	Hi-Z	—	FS	N	N	Y
A7	80	65	53	A6	PTC8	ND	Hi-Z	—	FS	N	N	Y
D6	81	66	54	B5	PTC9	ND	Hi-Z	—	FS	N	N	Y
C6	82	67	55	B4	PTC10	ND	Hi-Z	—	FS	N	N	Y
C5	83	68	56	A5	PTC11/LLWU_P11	ND	Hi-Z	—	FS	N	N	Y
B6	84	69			PTC12	ND	Hi-Z	—	FS	N	N	Y
A6	85	70			PTC13	ND	Hi-Z	—	FS	N	N	Y
A5	86				PTC14	ND	Hi-Z	—	FS	N	N	Y
B5	87				PTC15	ND	Hi-Z	—	FS	N	N	Y
	88				VFS	—	—	—	—	—	—	—
	89				VDD	—	—	—	—	—	—	—
D5		71			PTC16	ND	Hi-Z	—	FS	N	N	Y
C4	90	72			PTC17	ND	Hi-Z	—	FS	N	N	Y

Table continues on the next page...

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impendence
	H	High level
	L	Low level
Pullup/ pulldown setting after POR	PD	Pulldown
	PU	Pullup
Slew rate after POR	FS	Fast slew rate
	SS	Slow slew rate
Passive Pin Filter after POR	N	Disabled
	Y	Enabled
Open drain	N	Disabled[1]
	Y	Enabled[2]
Pin interrupt	Y	Yes

1. When I2C module is enabled and a pin is functional for I2C, this pin is (pseudo-) open drain enabled. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.
2. PTA20 is a true open drain pin that must never be pulled above VDD.

4.3 Module signal description tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

4.3.1 Core Modules

Table 9. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	SWD_DIO	Serial Wire Data	I/O
SWD_CLK	SWD_CLK	Serial Wire Clock	I

4.3.2 System modules

Table 10. System signal descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt **NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin.	I
RESET_b	—	Reset bi-directional signal	I/O
VDD	—	MCU power	I
VDDIO_E	PTE	MCU power for IOs on PTE	I
VDDA	—	MCU analog power	I
VSS	—	MCU ground	I
VREFH	—	MCU analog voltage reference-high	I
VREFL	—	MCU analog voltage reference--low	I

Table 11. EWM signal descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_ b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

Table 12. LLWU signal descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn	LLWU_Pn	Wakeup inputs	I

Table 13. EMVSIM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM0_CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM0_IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM0_PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM0_RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM0_VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O

Table 17. QSPI signal description (continued)

Chip signal name	Module signal Name	Description	I/O
		second device in a dual-die package flash A or the second of the two flash devices that share IOFA.	
QSPI0B_SS0_B	PCSFB1	Peripheral Chip Select Flash B1. This signal is the chip select for the serial flash device B1. B1 represents the first device in a dual-die package flash B or the first of the two flash devices that share IOFB.	O
QSPI0A_SCLK	SCKFA	Serial Clock Flash A. This signal is the serial clock output to the serial flash device A.	O
QSPI0B_SCLK	SCKFB	Serial Clock Flash B. This signal is the serial clock output to the serial flash device B.	O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0 QSPI0A_DATA3 QSPI0A_DATA2 QSPI0A_DATA1 QSPI0A_DATA0	IOFA[7:0]	Serial I/O Flash A. These signals are the data I/O lines to/from the serial flash device A. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values.	I/O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0	IOFB[3:0]	Serial I/O Flash B. These signals are the data I/O lines to/from the serial flash device B. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values.	I/O
QSPI0A_DQS	DQSFA	Data Strobe signal Flash A. Data strobe signal for port A. Some flash vendors provide the DQS signal to which the read data is aligned in DDR mode.	I

Table 27. TPM2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM1_CH[1:0]	TPM_CHn	A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

4.3.7 Communication interfaces

Table 28. USB FS OTG signal descriptions

Chip signal name	Module signal name	Description	I/O
USB0_DM	usb_dm	USB D- analog data signal on the USB bus.	I/O
USB0_DP	usb_dp	USB D+ analog data signal on the USB bus.	I/O
USB0_CLKIN	—	Alternate USB clock input	I
USB_VDD	—	USB domain power supply, 3.3 V.	I
USB0_SOF_OUT	—	USB start of frame signal. Can be used to make the USB start of frame available for external synchronization.	O

Table 29. SPI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O) in the master mode and Slave Select (I) in the slave mode	I/O
SPI0_PCS[1:3]	PCS[1:3]	Peripheral Chip Selects 1–3 in the master mode	O
SPI0_PCS4	PCS4	Peripheral Chip Select 4 in the master mode	O
SPI0_PCS5	PCS5	Peripheral Chip Select 5 /Peripheral Chip Select Strobe in the master mode	O
SPI0_SIN	SIN	Serial Data In	I
SPI0_SOUT	SOUT	Serial Data Out	O
SPI0_SCK	SCK	Serial Clock (O) in the master mode and Serial Clock (I) in the slave mode	I/O

Table 38. EMVSIM1 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
EMVSIM1_ PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM1_ RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM1_ VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O

4.3.8 Human-machine interfaces (HMI)

Table 39. GPIO signal descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0][1]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0][1]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[31:0][1]	PORTC31–PORTC0	General-purpose input/output	I/O
PTD[31:0][1]	PORTD31–PORTD0	General-purpose input/output	I/O
PTE[31:0][1]	PORTE31–PORTE0	General-purpose input/output	I/O

1. The available GPIO pins depends on the specific package. See the signal multiplexing section for which exact GPIO signals are available.

Table 40. TSI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
TSI0_CH[15:0]	TSI[15:0]	TSI capacitive pins. Switches driver that connects directly to the electrode pins TSI[15:0] can operate as GPIO pins.	I/O

4.4 KL82 Pinouts

The below figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage [1]	–0.3	3.8	V
V_{DDIO}	V_{DDIO} is an independent voltage supply for PORTE [2]	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[3], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. It applies for all port pins.
2. V_{DDIO} is independent of V_{DD} domain and can operate at a voltage independent of V_{DD}. However, it is required that V_{DD} domain be powered up first prior to V_{DDIO}. V_{DDIO} must never be higher than V_{DD} during power ramp up, or power down. V_{DD} and V_{DDIO} may ramp together if tied to the same power supply.

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
		85 °C	4000	5546		
		105 °C	9760	12709		
I_{DD_VLLS0}	VLLS0 current, all peripheral disabled, (SMC_STOPCTRL[PORPO] = 1), VDD = 3 V	25 °C and below	272	520	nA	
		50 °C	743	1398		
		70 °C	1700	2927		
		85 °C	3650	5177		
		105 °C	9300	12191		
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3 V	25 °C and below	160	218.10	nA	
		50 °C	269	366.96		
		70 °C	483	714.32		
		85 °C	851	1211.88		
		105 °C	1870	2715.16		
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 1.8 V	25 °C and below	137	195.10	nA	
		50 °C	230	327.96		
		70 °C	422	653.32		
		85 °C	746	1106.88		
		105 °C	1660	2505.16		
I_{DD_VBAT}	Average current when CPU is not accessing RTC register at 3.0 V including 32 kHz	25 °C and below	676	784.00	nA	
		50 °C	809	1013.00		
		70 °C	1040	1538.08		
		85 °C	1420	2022.17		
		105 °C	2460	3571.81		
I_{DD_VBAT}	Average current when CPU is not accessing RTC register at 1.8 V including 32 kHz	25 °C and below	556	664.00	nA	
		50 °C	674	878.00		
		70 °C	880	1378.08		
		85 °C	1220	1822.17		
		105 °C	2160	3271.81		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. CoreMark benchmark compiled using IAR 7.40 with optimization level high, optimized for balanced.
3. MCG configured for PEE mode.
4. MCG configured for FEE mode.
5. MCG configured for PBE mode.
6. MCG configured for BLPE mode.
7. MCG configured for FEI mode.

5.3.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, LPUART, timers, and I^2C signals.

Table 50. General switching specifications

Description		Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path		1.5	—	Bus clock cycles	1
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path		16 [2]	—	ns	3
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path		50	—	ns	3
External reset pulse width (digital glitch filter disabled)		100	—	ns	3
Port rise and fall time (high drive) — slew enabled	1.71 V < V_{DDIO_E} < 2.7 V	—	34	ns	4, 5
	2.7 V < V_{DDIO_E} ≤ 3.6 V	—	16		
Port rise and fall time (high drive) — slew disabled	1.71 V < V_{DDIO_E} < 2.7 V	—	4.5	ns	4, 5
	2.7 V < V_{DDIO_E} ≤ 3.6V	—	3		
Port rise and fall time (low drive) — slew enabled	1.71 V < V_{DDIO_E} < 2.7 V	—	25	ns	6, 5
	2.7 V < V_{DDIO_E} ≤ 3.6 V	—	16		
Port rise and fall time (high drive) — slew disabled	1.71 V < V_{DDIO_E} < 2.7 V	—	4.2	ns	6, 5
	2.7 V < V_{DDIO_E} ≤ 3.6V	—	2.5		
Port rise and fall time (low drive) — slew enabled	1.71 < V_{DDIO_E} < 2.7V	—	25	ns	6, 7
	2.7 < V_{DDIO_E} ≤ 3.6V	—	13		
Port rise and fall time (low drive) — slew disabled	1.71 < V_{DDIO_E} < 2.7V	—	5.5	ns	6, 7
	2.7 < V_{DDIO_E} ≤ 3.6V	—	3.5		

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. This is applicable for Port E pins
6. 25 pF load
7. This is applicable for Ports A, B, C, and D.

5.3.4 Thermal specifications

Table 66. QuadSPI output timing (Hyperflash mode) specifications (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Tho	Output Data Hold	1.3	—	ns
$Tclk_{SKMAX}$	Ck to Ck2 skew max	—	T/4 + 0.5	ns
$Tclk_{SKMIN}$	Ck to Ck2 skew min	T/4 - 0.5	—	ns

NOTE

Maximum clock frequency = 72 MHz.

5.4.3.2 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.4.3.2.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 67. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.4.3.2.2 Flash timing specifications — commands

Table 68. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	100	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	140	1150	ms	2

Table continues on the next page...

4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

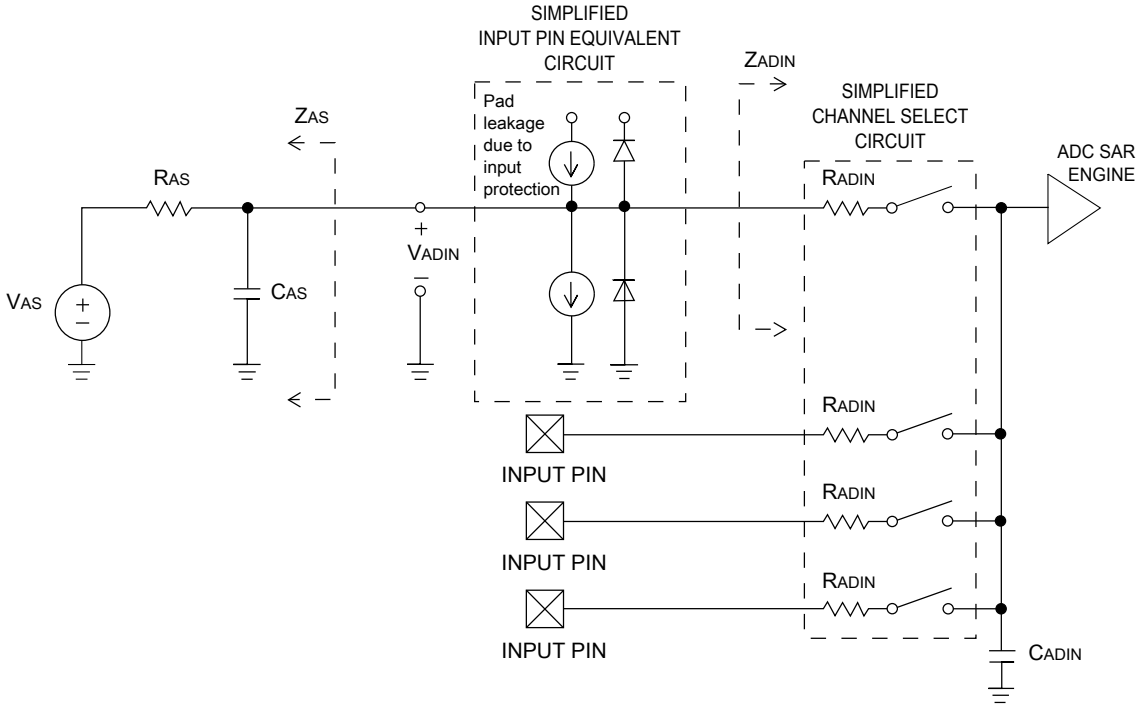


Figure 29. ADC input impedance equivalency diagram

5.4.5.1.2 16-bit ADC electrical characteristics

Table 72. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		

Table continues on the next page...

5.4.7.1 EMV SIM specifications

Each EMV SIM module interface consists of a total of five pins.

The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

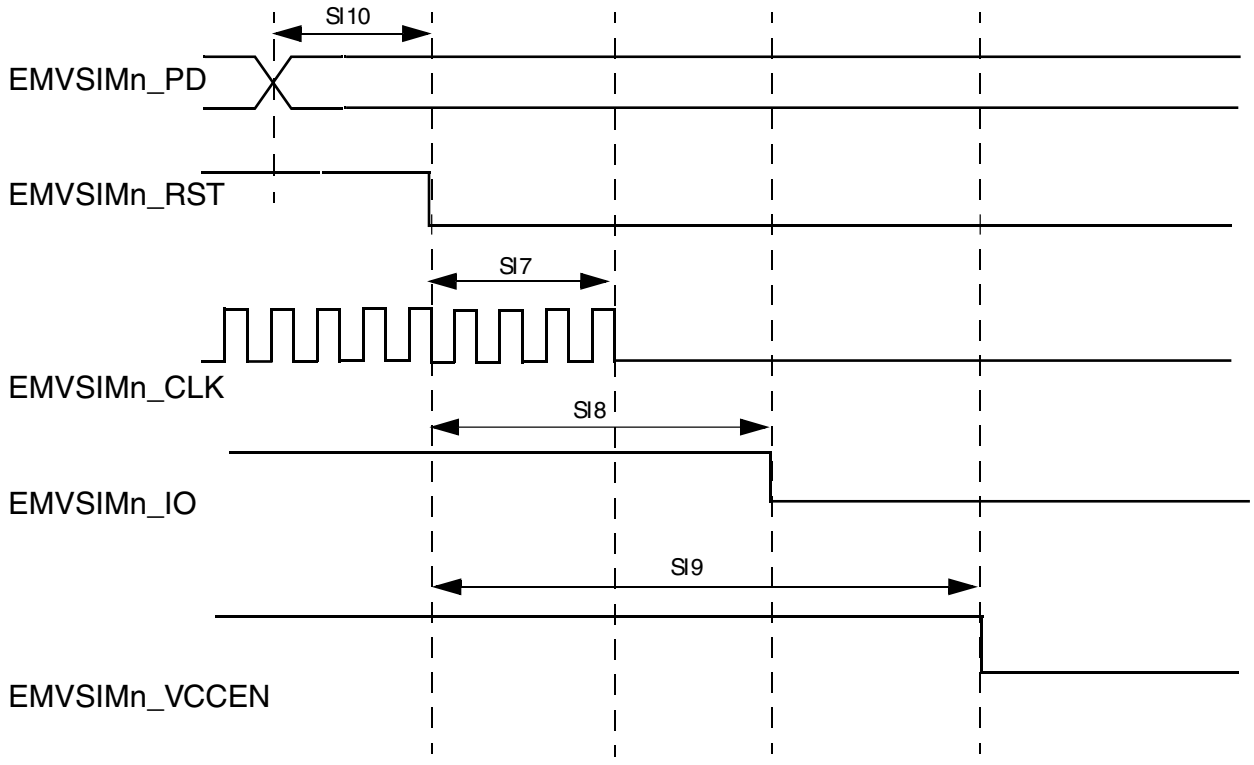


Figure 36. EMV SIM Clock Timing Diagram

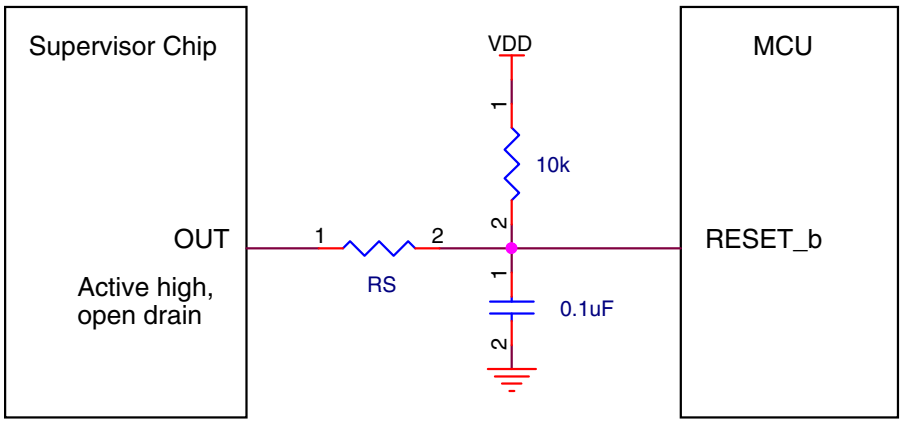


Figure 48. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

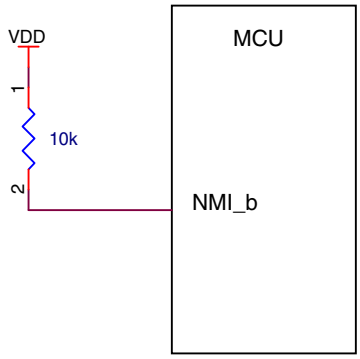


Figure 49. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

Table 91. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768kHz), low power	Diagram 1
Low frequency (32.768kHz), high gain	Diagram 2, Diagram 4
High frequency (3-32MHz), low power	Diagram 3
High frequency (3-32MHz), high gain	Diagram 4

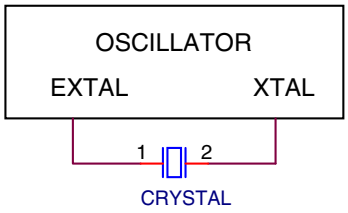


Figure 51. Crystal connection – Diagram 1

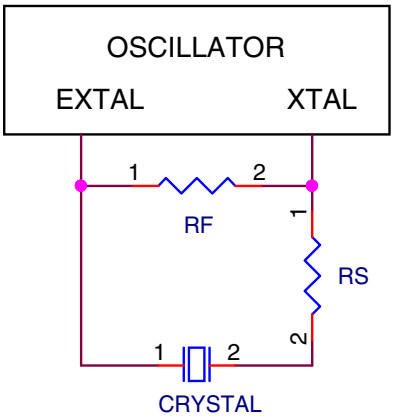


Figure 52. Crystal connection – Diagram 2

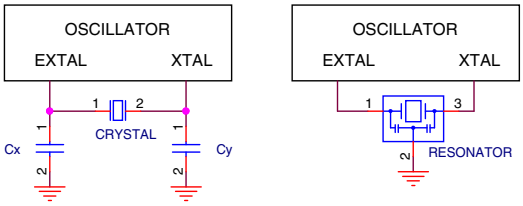


Figure 53. Crystal connection – Diagram 3