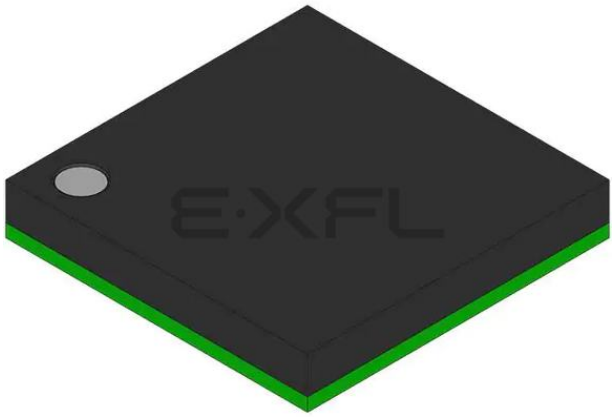

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | I²C, SPI, UART/USART, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 12x16b; D/A 1x6b, 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-LFBGA |
| Supplier Device Package | 121-MAPBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl82z128vmc7 |

- Memory protection unit
- SRAM bit-banding

**Clocks**

- 48 MHz high accuracy (up to 0.5%) internal reference clock for high-speed run
- 4 MHz high accuracy (up to 2%) internal reference clock for low-speed run
- 32 kHz internal reference clock
- 1 kHz internal reference clock
- 32–40 kHz and 3–32 MHz crystal oscillator
- PLL/FLL

**Timers**

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- Two low-power timers
- 4-channel periodic interrupt timer
- Independent real time clock

**Security**

- 128-bit unique identification number per chip
- Advanced flash security and access control
- Hardware CRC module
- Low-power trusted crypto engine supporting AES128/256, DES, 3DES, SHA256, RSA and ECC, with hardware DPA
- True random number generator

**I/O**

- Up to 85 General-purpose input/output pins (GPIO)

**Operating Characteristics**

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

**Low Power**

- Down to 125 µA/MHz in Run mode
- Down to 272 nA in Stop mode (RAM and RTC retained)
- Six flexible static modes

**Packages**

- 121 MAPBGA 8mm x 8mm, 0.65mm pitch, 1.43mm max thickness
- 80 LQFP 12mm x 12mm, 0.5mm pitch, 1.6mm max thickness
- 100 LQFP 14mm x 14mm, 0.5mm pitch, 1.7mm max thickness (Package Your Way)
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm max thickness (Package Your Way)
- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm max thickness (Package Your Way)

**NOTE**

The 100-, 64-pin LQFP and 64-pin MAPBGA packages supporting MKL82Z128VLL7, MKL82Z128VLH7 and MKL82Z128VMP7 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

## Related resources

| Type | Description | Resource |
|---|---|---|
| Selector Guide | The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KL82P121M72SF0RM[1] |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | KL82P121M72SF0[1] |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | *x*N51R[2] |
| Package drawing | Package dimensions are provided in package drawings. | MAPBGA 121-pin: 98ASA00423D<br>MAPBGA 64-pin: 98ASA00420D<br>LQFP 100-pin: 98ASS23308W<br>LQFP 80-pin: 98ASS23174W<br>LQFP 64-pin: 98ASS23234W |

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

The following table summarizes the clocks associated with each module.

**Table 4. Module clocks**

| Module | Bus interface clock | Internal clocks | I/O interface clocks |
|---|---|---|---|
| **Core modules** | | | |
| ARM Cortex-M0+ core | System clock | Core clock | — |
| NVIC | System clock | — | — |
| DAP | System clock | — | SWD_CLK |
| **System modules** | | | |
| DMA | System clock | — | — |
| DMAMUX | Bus clock | — | — |
| Port control | Bus clock | LPO | — |
| Crossbar Switch | System clock | — | — |
| Peripheral bridges | System clock | Bus clock | — |
| LLWU, PMC, SIM, RCM | Bus clock | LPO | — |
| Mode controller | Bus clock | — | — |
| INTMUX | Bus clock | — | — |
| MCM | System clock | — | — |
| EWM | Bus clock | LPO | — |
| Watchdog timer | Bus clock | LPO | — |
| **Clocks** | | | |
| MCG | Flash clock | MCGOUTCLK, MCGPLLCLK, MCGFLLCLK, MCGIRCLK, OSCERCLK | — |
| OSC | Bus clock | OSCERCLK | — |
| IRC48M | — | IRC48MCLK | — |
| **Memory and memory interfaces** | | | |
| Flash controller | System clock | Flash clock | — |
| Flash memory | Flash clock | — | — |
| QSPI controller | QSPI bus interface clock | QSPI clock | QSPIx_SCK |
| **Security** | | | |
| CRC | Bus clock | — | — |
| TRNG | Bus clock | — | — |
| LTC Encryption Engine | System clock | — | — |
| **Analog** | | | |
| ADC | Bus clock | OSCERCLK, IRC48MCLK | — |
| CMP | Bus clock | — | — |
| DAC | Bus clock | — | — |
| VREF | Flash clock | — | — |
| **Timers** | | | |

*Table continues on the next page...*

### 2.2.13 I2C

This device contains two I2C modules, which support up to 1 Mbits/s by dual buffer features, and address match to wake MCU from the low power mode.

I2C modules support DMA transfer, and the interrupt condition can trigger DMA request when DMA function is enabled.

The I2C modules have the following features:

- Support for system management bus (SMBus) Specification, version 2
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition
- 10-bit address extension
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support
- DMA support
- Double buffering support to achieve higher baud rate

### 2.2.14 USB

This device contains one USB module which implements a USB2.0 full-speed compliant peripheral and interfaces to the on-chip USBFS transceiver. It implements keep-alive feature to avoid re-enumerating when exiting from low power modes and enables HIRC48M to allow crystal-less USB operation.

The USBFS has the following features:

- USB 1.1 and 2.0 compatible FS device controller
- 16 bidirectional endpoints
- DMA or FIFO data stream interfaces
- Low-power consumption

- IRC48M with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.
- Keep-alive feature is supported to power down system bus and CPU. USB can respond to IN with NAK and wake up for SETUP/OUT.

### 2.2.15 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to LPUART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/ Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation. It also supports to work in VLPR, VLPW, Stop, and VLPS modes when clock source remains enabled.

The FlexIO module has the following features:

- Array of 32-bit shift registers with transmit, receive and data match modes
- Double buffered shifter operation for continuous data transfer
- Shifter concatenation to support large transfer sizes
- Automatic start/stop bit generation
- 1, 2, 4, 8, 16 or 32 multi-bit shift widths for parallel interface support
- Interrupt, DMA or polled transmit/receive operation
- Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during stop modes
- Highly flexible 16-bit timers with support for a variety of internal or external trigger, reset, enable and disable conditions
- Programmable logic mode for integrating external digital logic functions on-chip or combining pin/shifter/timer functions to generate complex outputs
- Programmable state machine for offloading basic system control functions from CPU with support for up to 8 states, 8 outputs and 3 selectable inputs per state

### 2.2.16 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, OPAMPS or ADC.

DAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 $V_{in}$ to $V_{in}$, and the step is 1⁄4096 $V_{in}$, where $V_{in}$ is the input voltage.

| 121 MAPBGA | 100 LQFP | 80 LQFP | 64 LQFP | 64 MAPBGA | Pin Name | Driver strength | Default status after POR | Pullup/ pulldown setting after POR | Slew rate after POR | Passive pin filter after POR | Open drain | Pin interrupt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J2 | 20 | | | | NC | — | — | — | — | — | — | — |
| | 21 | | | | NC | — | — | — | — | — | — | — |
| K2 | | | | | ADC0_DP0 | ND | Hi-Z | — | FS | N | N | — |
| K1 | | | | | ADC0_DM0 | ND | Hi-Z | — | FS | N | N | — |
| F5 | 22 | 17 | 13 | G2 | VDDA | — | — | — | — | — | — | — |
| G5 | 23 | 18 | 14 | H3 | VREFH | — | — | — | — | — | — | — |
| G6 | 24 | 19 | 15 | H2 | VREFL | — | — | — | — | — | — | — |
| F6 | 25 | 20 | 16 | G1 | VFSA | — | — | — | — | — | — | — |
| L2 | 26 | 21 | 17 | H1 | ADC0_DP1 | ND | Hi-Z | — | FS | N | N | — |
| L1 | 27 | 22 | 18 | G3 | ADC0_DM1 | ND | Hi-Z | — | FS | N | N | — |
| L3 | 28 | 23 | 19 | F4 | VREF_OUT/ CMP0_IN5/ ADC0_SE22 | ND | Hi-Z | — | FS | N | N | — |
| K4 | 29 | 24 | 20 | G4 | DAC0_OUT/ ADC0_SE23 | ND | Hi-Z | — | FS | N | N | — |
| H6 | | | | | NC | — | — | — | — | — | — | — |
| K5 | 30 | 25 | 21 | F5 | RTC_WAKEUP_B | ND | Hi-Z | — | FS | N | Y | — |
| L4 | 31 | 26 | 22 | H4 | XTAL32 | ND | Hi-Z | — | FS | N | N | Y |
| L5 | 32 | 27 | 23 | H5 | EXTAL32 | ND | Hi-Z | — | FS | N | N | Y |
| K6 | 33 | 28 | 24 | G5 | VBAT | — | — | — | — | — | — | — |
| | 34 | | | | VDD | — | — | — | — | — | — | — |
| | 35 | | | | VFS | — | — | — | — | — | — | — |
| L7 | 36 | 29 | 25 | D4 | PTA0 | ND | L | PU | FS | N | N | Y |
| H8 | 37 | 30 | 26 | D5 | PTA1 | ND | H | PU | FS | N | N | Y |
| J7 | 38 | 31 | 27 | E5 | PTA2 | ND | H | PU | FS | N | N | Y |
| H9 | 39 | 32 | 28 | H6 | PTA3 | ND | H | PU | FS | N | N | Y |
| J8 | 40 | 33 | 29 | G6 | PTA4/LLWU_P3 | ND | H | PU | FS | Y | N | Y |
| K7 | 41 | | | | PTA5 | ND | H | PU | FS | N | N | Y |
| L10 | | | | | VDD | — | — | — | — | — | — | — |
| K10 | | | | | VFS | — | — | — | — | — | — | — |

*Table continues on the next page...*

## 4.3.2 System modules

### Table 10. System signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| NMI_b | — | Non-maskable interrupt<br>**NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin. | I |
| RESET_b | — | Reset bi-directional signal | I/O |
| VDD | — | MCU power | I |
| VDDIO_E | PTE | MCU power for IOs on PTE | I |
| VDDA | — | MCU analog power | I |
| VSS | — | MCU ground | I |
| VREFH | — | MCU analog voltage reference-high | I |
| VREFL | — | MCU analog voltage reference--low | I |

### Table 11. EWM signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EWM_IN | EWM_in | EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low. | I |
| EWM_OUT_ b | $\overline{\text{EWM\_out}}$ | EWM reset out signal | O |

### Table 12. LLWU signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LLWU_Pn | LLWU_Pn | Wakeup inputs | I |

### Table 13. EMVSIM0 signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EMVSIM0_CLK | EMVSIM_SCLK | Card Clock. Clock to Smart Card. | O |
| EMVSIM0_IO | EMVSIM_IO | Card Data Line. Bi-directional data line. | I/O |
| EMVSIM0_PD | EMVSIM_PD | Card Presence Detect. Signal indicating presence or removal of card | I |
| EMVSIM0_RST | EMVSIM_SRST | Card Reset. Reset signal to Smart Card | O |
| EMVSIM0_VCCEN | EMVSIM_VCC_EN | Card Power Enable. This signal controls the power to Smart Card | O |

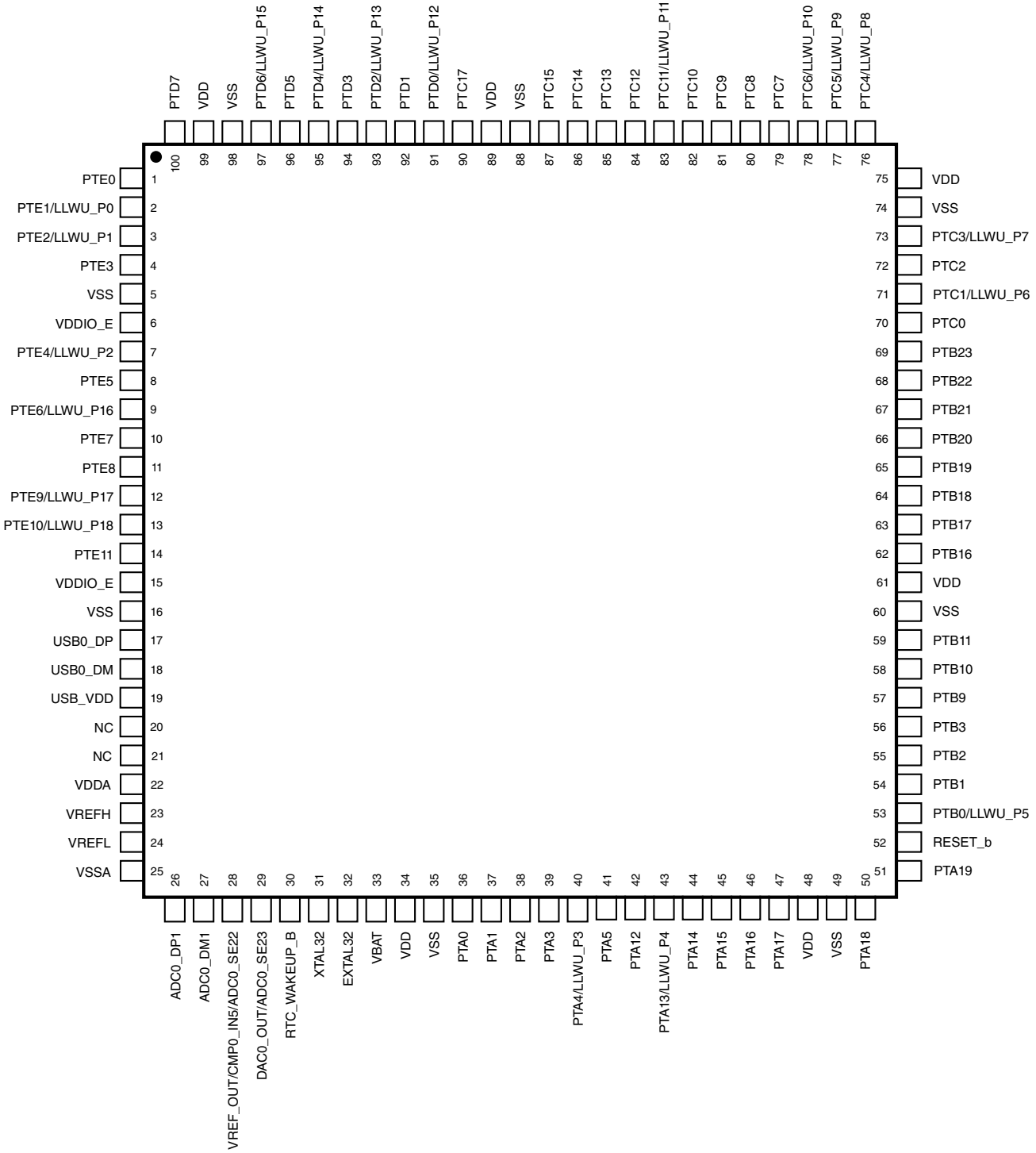


**Figure 6. KL82 100-pin LQFP pinout diagram**

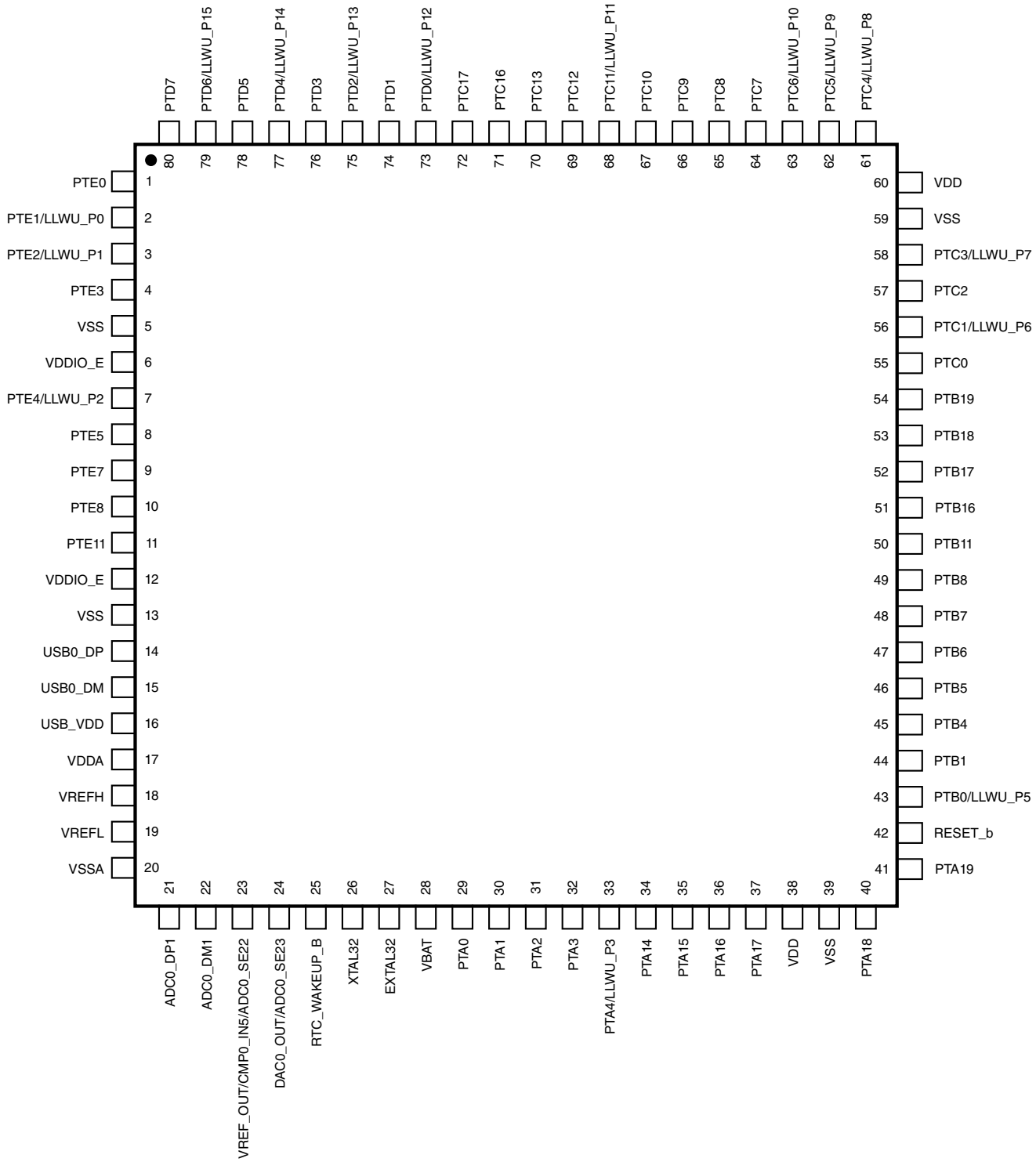


**Figure 7. KL82 80-pin LQFP pinout diagram**

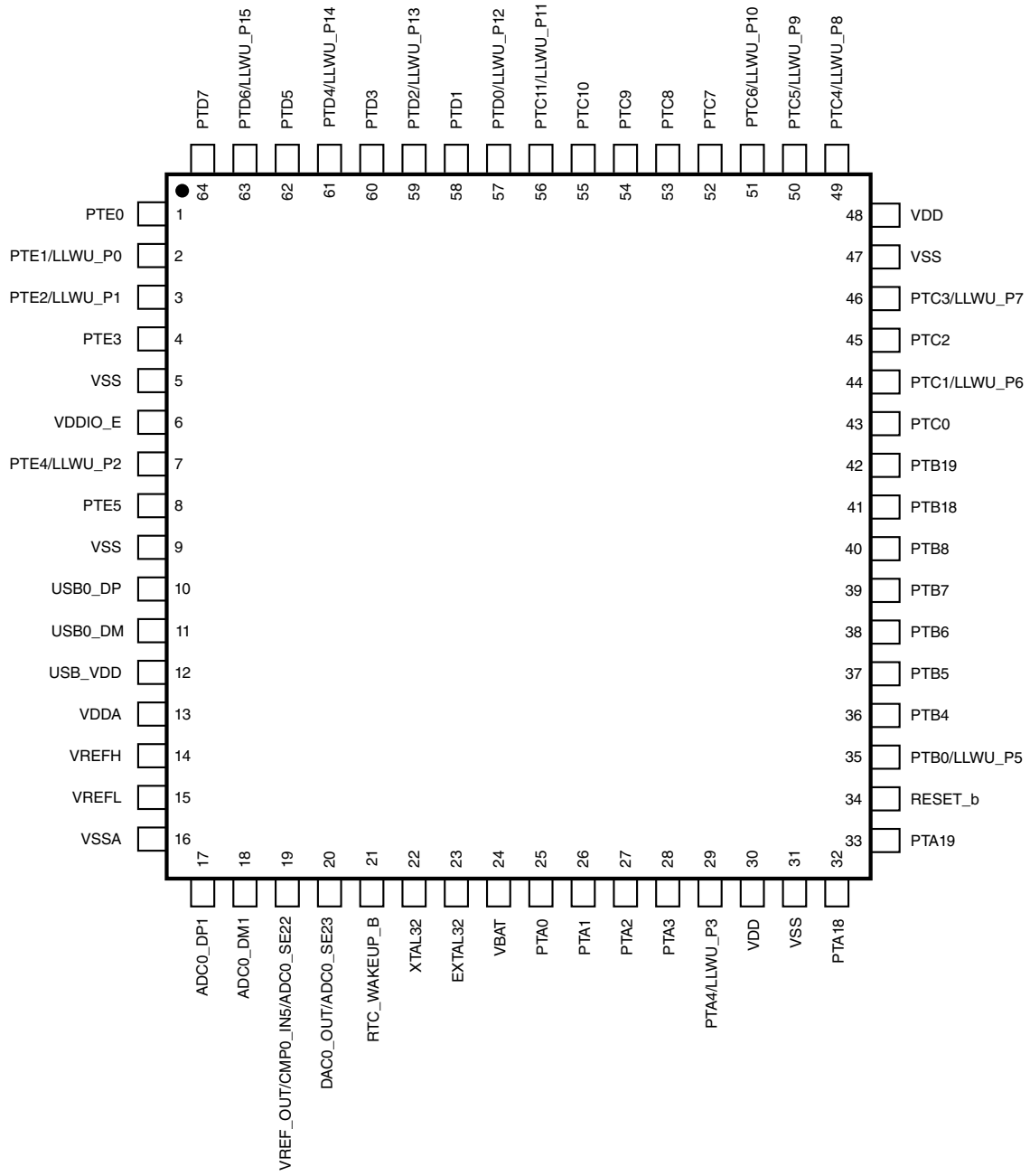


**Figure 9. KL82 64-pin LQFP pinout diagram**

## NOTE

The 100-, 64-pin LQFP and 64-pin MAPBGA packages for this product are not yet available, however they are included in a Package Your Way program for KL MCUs. Please visit nxp.com/KPYW for more details.

# 5.1 Terminology and guidelines

## 5.1.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|---|---|
| Rating | A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:<br>• *Operating ratings* apply during operation of the chip.<br>• *Handling ratings* apply when the chip is not powered.<br>**NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings. |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | A specified value for a technical characteristic that:<br>• Lies within the range of values specified by the operating behavior<br>• Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions<br>**NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed. |

## Table 47. Power consumption operating behaviors (continued)

| Symbol | Description | | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_RUN}$ | Running CoreMark in Flash all peripheral clock disabled, Core at 12 MHz, bus at 6 MHz, flash at 6 MHz , VDD = 3 V | 25 °C | 2.8 | 4.40 | mA | 2, 5 |
| | | 105 °C | 3.22 | 4.67 | | |
| $I_{DD\_RUN}$ | Running CoreMark in Flash all peripheral clock enabled, Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V | 25 °C | 12.94 | 14.54 | mA | 2, 4 |
| | | 105 °C | 13.35 | 14.80 | | |
| $I_{DD\_RUN}$ | Running While(1) loop in Flash, all peripheral clock disabled Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V | 25 °C | 7.6 | 9.20 | mA | 4 |
| | | 105 °C | 8.08 | 9.53 | | |
| $I_{DD\_RUN}$ | Running While(1) loop in Flash, all peripheral clock disabled Core at 48 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V | 25 °C | 6.3 | 7.90 | mA | 5 |
| | | 105 °C | 6.79 | 8.24 | | |
| $I_{DD\_RUN}$ | Running While(1) loop in Flash, all peripheral clock disabled Core at 24 MHz, bus at 12 MHz, flash at 12 MHz , VDD = 3 V | 25 °C | 4.08 | 5.68 | mA | 5 |
| | | 105 °C | 4.53 | 5.98 | | |
| $I_{DD\_RUN}$ | Running While(1) loop in Flash, all peripheral clock disabled Core at 12 MHz, bus at 6 MHz, flash at 6 MHz , VDD = 3 V | 25 °C | 3.03 | 4.63 | mA | 5 |
| | | 105 °C | 3.46 | 4.91 | | |
| $I_{DD\_RUN}$ | Running While(1) loop in Flash, all peripheral clock enabled Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V | 25 °C | 10.93 | 12.53 | mA | 4 |
| | | 105 °C | 11.45 | 12.90 | | |
| $I_{DD\_RUN}$ | Running CoreMark loop in SRAM all peripheral clock disabled, Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V | 25 °C | 11.64 | 13.24 | mA | 2, 4 |
| | | 105 °C | 12.17 | 13.62 | | |
| $I_{DD\_RUN}$ | Running CoreMark loop in SRAM in Compute Operation mode, Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V | 25 °C | 10.52 | 12.12 | mA | 2, 4 |
| | | 105 °C | 11.03 | 12.48 | | |
| $I_{DD\_WAIT}$ | Core disabled, system at 72 MHz, bus at 24 MHz, flash disabled (flash doze enabled), VDD = 3 V, all peripheral clocks disabled | 25 °C | 5.11 | 6.47 | mA | 4 |
| $I_{DD\_WAIT}$ | Core disabled, system at 48 MHz, bus at 24 MHz, flash disabled (flash doze enabled), VDD = 3 V, all peripheral clocks disabled | 25 °C | 4.33 | 5.69 | mA | 5 |
| $I_{DD\_WAIT}$ | Core disabled, system at 24 MHz, bus at 12 MHz, flash disabled (flash doze enabled), VDD = 3 V, all peripheral clocks disabled | 25 °C | 2.76 | 4.12 | mA | 5 |

*Table continues on the next page...*

## Table 47. Power consumption operating behaviors (continued)

| Symbol | Description | | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLLS2}$ | VLLS2 current, all peripheral disable, VDD = 3 V | 25 °C and below | 1.98 | 3.78 | µA | |
| | | 50 °C | 2.95 | 5.71 | | |
| | | 70 °C | 4.83 | 9.33 | | |
| | | 85 °C | 7.95 | 13.80 | | |
| | | 105 °C | 16.92 | 24.26 | | |
| $I_{DD\_VLLS2}$ | VLLS2 with RTC current, VDD = 3 V | 25 °C and below | 2.8 | 4.60 | µA | |
| | | 50 °C | 3.74 | 6.50 | | |
| | | 70 °C | 5.96 | 10.46 | | |
| | | 85 °C | 9.35 | 15.20 | | |
| | | 105 °C | 19.37 | 26.71 | | |
| $I_{DD\_VLLS2}$ | VLLS2 with RTC current, VDD = 1.8 V | 25 °C and below | 2.56 | 4.36 | µA | |
| | | 50 °C | 3.43 | 6.19 | | |
| | | 70 °C | 5.51 | 10.01 | | |
| | | 85 °C | 8.61 | 14.46 | | |
| | | 105 °C | 18.87 | 26.21 | | |
| $I_{DD\_VLLS1}$ | VLLS1 current, all peripheral disable, VDD = 3 V | 25 °C and below | 0.718 | 1.11 | µA | |
| | | 50 °C | 1.28 | 2.48 | | |
| | | 70 °C | 2.4 | 4.56 | | |
| | | 85 °C | 4.38 | 7.62 | | |
| | | 105 °C | 10.28 | 15.68 | | |
| $I_{DD\_VLLS1}$ | VLLS1 with RTC current, VDD = 3 V | 25 °C and below | 1.51 | 1.90 | µA | |
| | | 50 °C | 2.13 | 3.63 | | |
| | | 70 °C | 3.65 | 6.29 | | |
| | | 85 °C | 5.76 | 9.00 | | |
| | | 105 °C | 12.89 | 18.29 | | |
| $I_{DD\_VLLS1}$ | VLLS1 with RTC current, VDD = 1.8 V | 25 °C and below | 1.26 | 1.65 | µA | |
| | | 50 °C | 1.73 | 3.23 | | |
| | | 70 °C | 2.93 | 5.57 | | |
| | | 85 °C | 4.98 | 8.22 | | |
| | | 105 °C | 11.21 | 16.61 | | |
| $I_{DD\_VLLS0}$ | VLLS0 current, all peripheral disabled, (SMC_STOPCTRL[PORPO] = 0), VDD = 3 V | 25 °C and below | 432 | 835 | nA | |
| | | 50 °C | 986 | 1723 | | |
| | | 70 °C | 2030 | 3270 | | |

*Table continues on the next page...*

#### 5.3.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

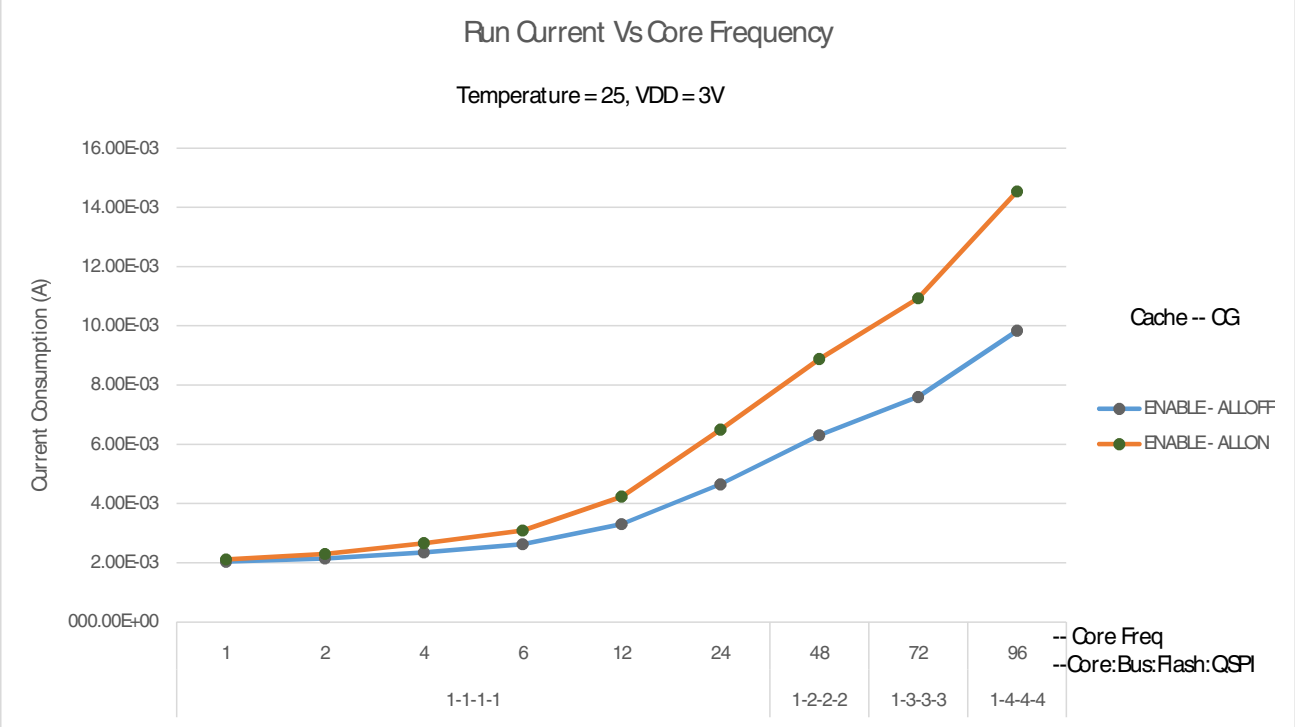


**Figure 19. Run mode supply current vs. core frequency**

### 5.4.1.2 SWD electricals

**Table 53. SWD full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation<br>• Serial wire debug | <br>0 | <br>25 | <br>MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width<br>• Serial wire debug | <br>20 | <br>— | <br>ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

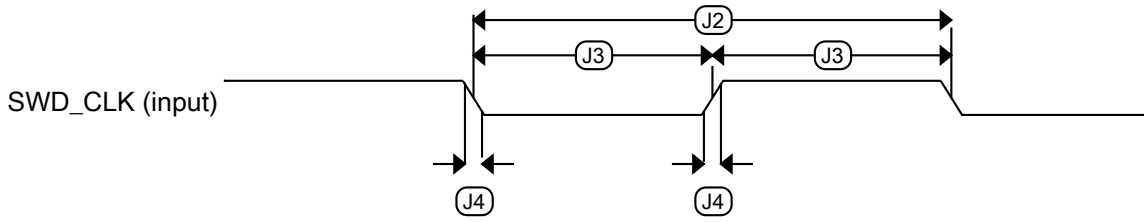


**Figure 21. Serial wire clock input timing**

**NOTE**

- Numbers are for a load of 15pf (1.8V) and 35pf (3V)
- The numbers are for setting of hold condition in register QuadSPI_SMPR[DDRSNP]

**Table 63. QuadSPI input timing (DDR mode) specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{is}$ | Setup time for incoming data | 4 (Without learning) | — | ns |
| | | 1 (With learning) | — | |
| $T_{ih}$ | Hold time requirement for incoming data | 1.5 | — | ns |

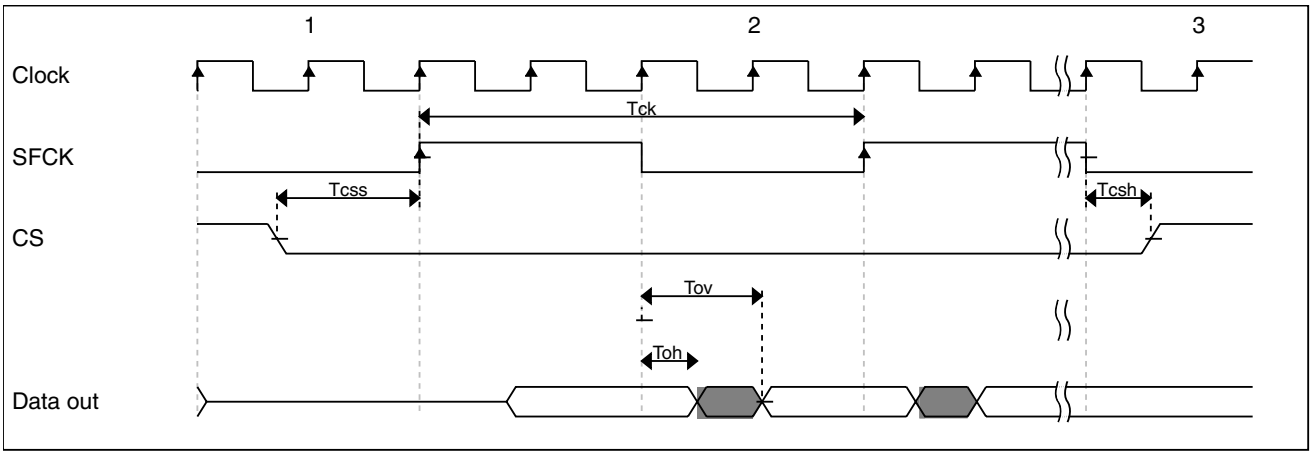


**Figure 26. QuadSPI output timing (DDR mode) diagram**

**Table 64. QuadSPI output timing (DDR mode) specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{ov}$ | Output Data Valid | — | 4.5 | ns |
| $T_{oh}$ | Output Data Hold | 1.5 | — | ns |
| $T_{ck}$ | SCK clock period | — | 72 (with learning) | MHz |
| | | — | 45 (without learning) | |
| $T_{css}$ | Chip select output setup time | 2 | — | Clk(sck) |
| $T_{csh}$ | Chip select output hold time | -1 | — | Clk(sck) |

## Hyperflash mode

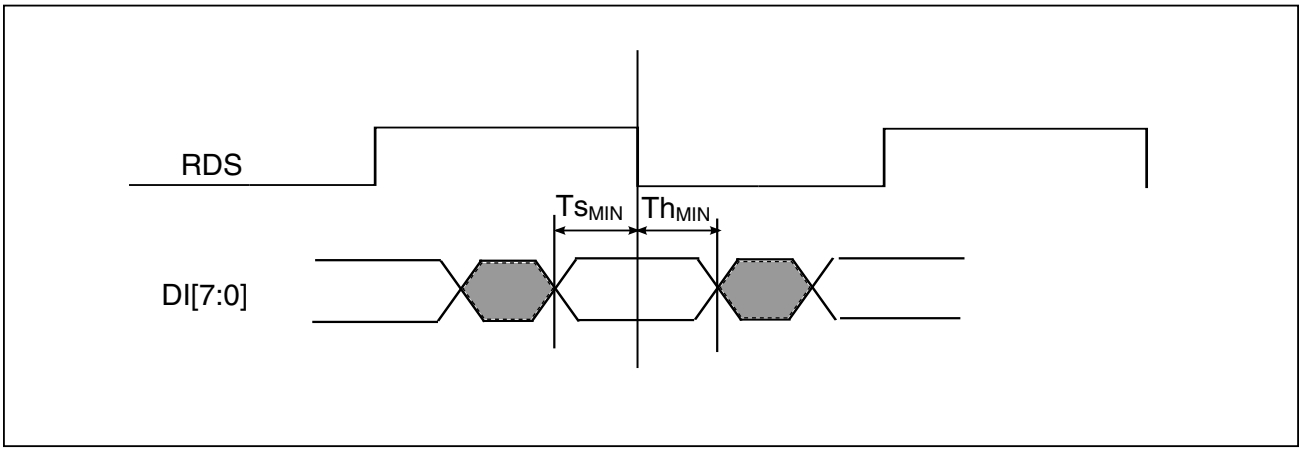


**Figure 27. QuadSPI input timing (Hyperflash mode) diagram**

**Table 65. QuadSPI input timing (Hyperflash mode) specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $Ts_{MIN}$ | Setup time for incoming data | 2 | — | ns |
| $Th_{MIN}$ | Hold time requirement for incoming data | 2 | — | ns |

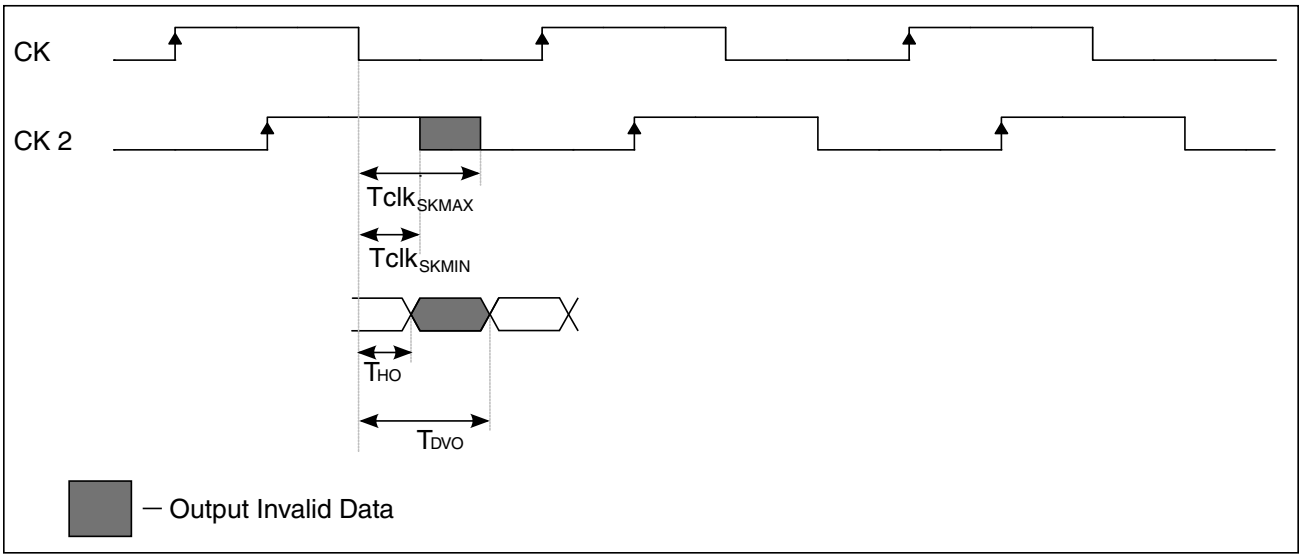


**Figure 28. QuadSPI output timing (Hyperflash mode) diagram**

**Table 66. QuadSPI output timing (Hyperflash mode) specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $Tdv_{MAX}$ | Output Data Valid | — | 4.3 | ns |

*Table continues on the next page...*

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 5.4.5.1.1 16-bit ADC operating conditions

**Table 71. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | — |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br>• All other modes | VREFL<br>VREFL | —<br>— | 31/32 × VREFH<br>VREFH | V | — |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-bit / 10-bit / 12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | — |
| $R_{ADIN}$ | Input series resistance | | — | 2 | 5 | kΩ | — |
| $R_{AS}$ | Analog source resistance (external) | 13-bit / 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | ksps | 5 |
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1 ns.

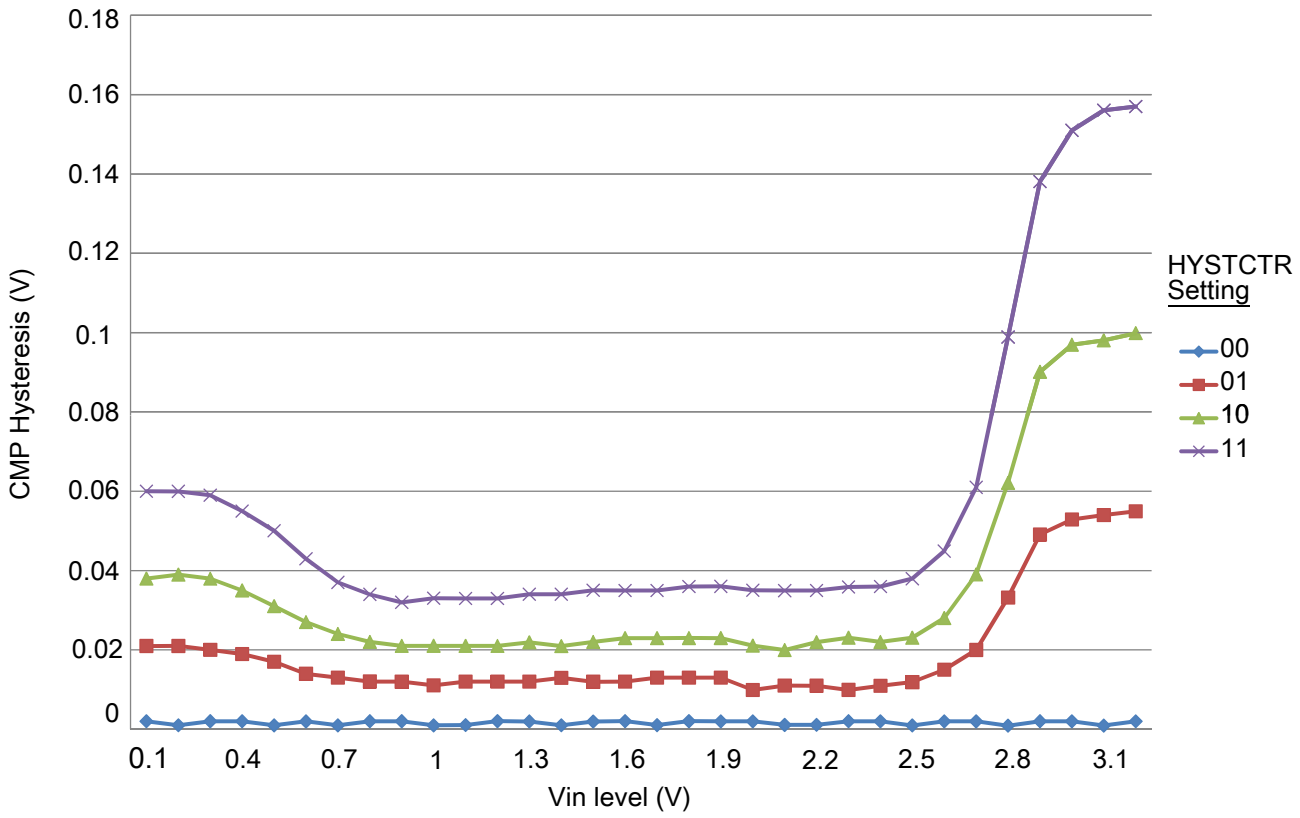


**Figure 33. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

## 5.4.5.3 12-bit DAC electrical characteristics

### 5.4.5.3.1 12-bit DAC operating requirements

**Table 74. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or $V_{REFH}$.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

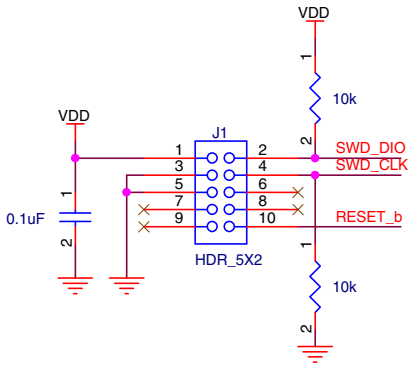


**Figure 50. SWD debug interface**

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect USB_VDD to ground through a 10 kΩ resistor if the USB module is not used.

## 6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16pF are sufficient for 32.768kHz crystals that have a 12.5pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.


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