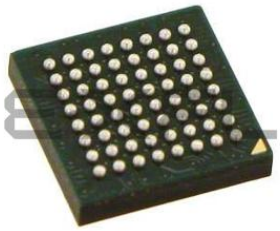

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x16b; D/A 1x6b, 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	64-MAPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl82z128vmp7

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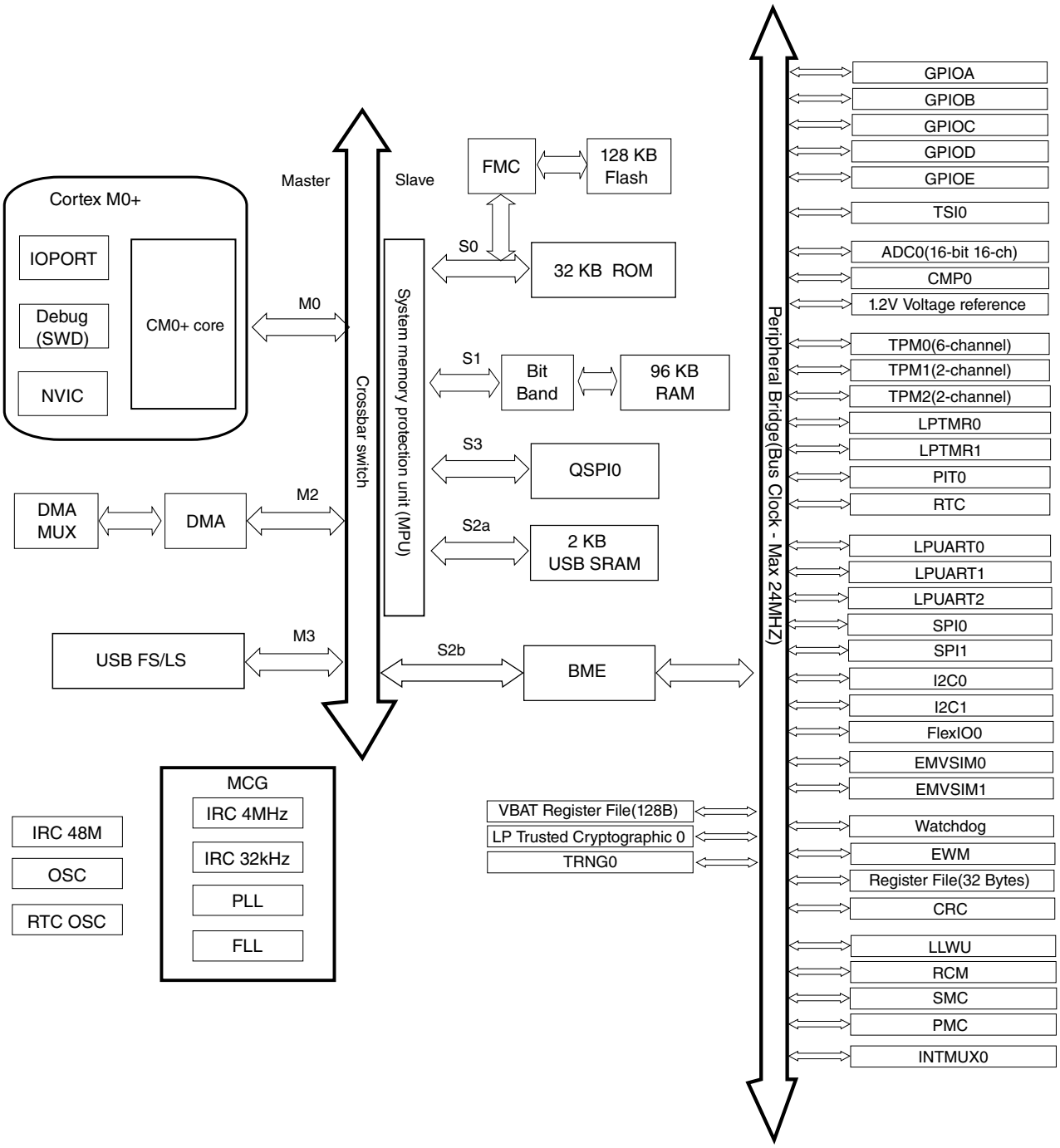

Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

Table 2. AWIC Partial Stop, Stop and VLPS wake-up sources

Wake-up source	Description
Available system resets	RESET_b pin and WDOG when LPO is its clock source, and Debug
Low-voltage detect	Power mode controller
Low-voltage warning	Power mode controller
Pin interrupts	Port control module - any enabled pin interrupt is capable of waking the system
ADC0	The ADC is functional when using internal clock source
CMPx	Since no system clocks are available, functionality is limited, trigger mode provides wakeup functionality with periodic sampling
I2Cx	Address match wakeup
LPUARTx	Functional when using clock source which is active in Stop and VLPS modes
USB FS/LS Controller	Wakeup
FlexIO0	Functional when using clock source which is active in Stop and VLPS modes
LPTMR	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
RTC	Functional in Stop/VLPS modes
TPM	Functional when using clock source which is active in Stop and VLPS modes
TSI0	Wakeup
NMI	Non-maskable interrupt

2.1.4 Memory

This device has the following features:

- 96 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into two arrays
  - 128 KB of embedded program memory
  - 32 KB ROM (built-in bootloader to support UART, I2C, USB, and SPI interfaces)

  The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 1 KB.

  The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

This device contains a 32-byte register file that is powered in all power modes.

Also, it retains contents during low power modes and is reset only during a power-on reset.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC[1]	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	N	Y	Y
System reset	Low leakage wakeup (LLWU) reset	N	Y[2]	N	Y	N	Y[3]	N	N	Y
	External pin reset ($\overline{\text{RESET}}$)	Y	Y[2]	Y[4]	Y	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Software reset (SW)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	MDM DAP system reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
Debug reset	Debug reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y

1. The VBAT POR asserts on a VBAT POR reset source. It affects only the modules withinthe VBAT power domain: RTC and VBAT Register File. These modules are notaffected by the other reset types.
2. Except SIM_SOPT1
3. Only if $\overline{\text{RESET}}$ is used to wake from VLLS mode.
4. Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
5. Except RCM_RPFC, RCM_RPFW, RCM_FM

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

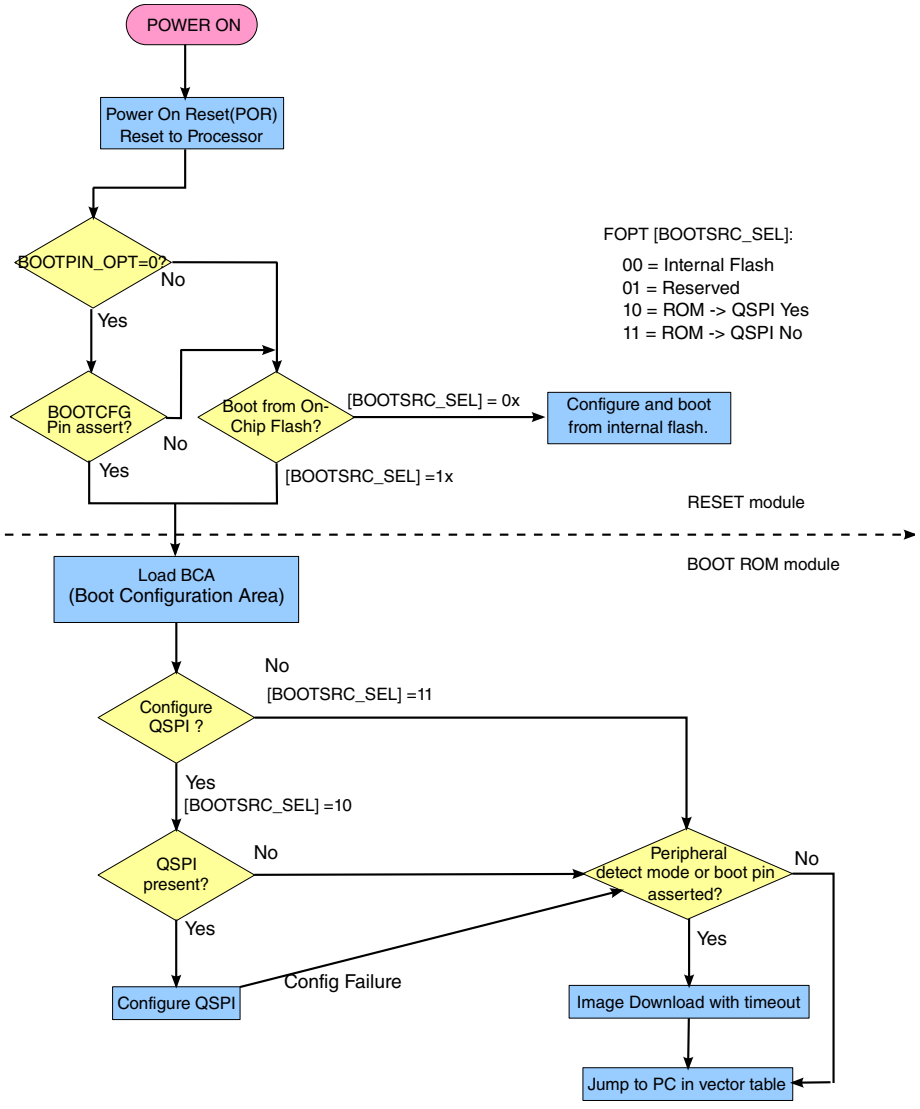

Figure 2. Boot Flow For Devices with QSPI

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

The following table summarizes the clocks associated with each module.

Table 4. Module clocks

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			
ARM Cortex-M0+ core	System clock	Core clock	—
NVIC	System clock	—	—
DAP	System clock	—	SWD_CLK
System modules			
DMA	System clock	—	—
DMAMUX	Bus clock	—	—
Port control	Bus clock	LPO	—
Crossbar Switch	System clock	—	—
Peripheral bridges	System clock	Bus clock	—
LLWU, PMC, SIM, RCM	Bus clock	LPO	—
Mode controller	Bus clock	—	—
INTMUX	Bus clock	—	—
MCM	System clock	—	—
EWM	Bus clock	LPO	—
Watchdog timer	Bus clock	LPO	—
Clocks			
MCG	Flash clock	MCGOUTCLK, MCGPLLCLK, MCGFLLCLK, MCGIRCLK, OSCERCLK	—
OSC	Bus clock	OSCERCLK	—
IRC48M	—	IRC48MCLK	—
Memory and memory interfaces			
Flash controller	System clock	Flash clock	—
Flash memory	Flash clock	—	—
QSPI controller	QSPI bus interface clock	QSPI clock	QSPIx_SCK
Security			
CRC	Bus clock	—	—
TRNG	Bus clock	—	—
LTC Encryption Engine	System clock	—	—
Analog			
ADC	Bus clock	OSCERCLK, IRC48MCLK	—
CMP	Bus clock	—	—
DAC	Bus clock	—	—
VREF	Flash clock	—	—
Timers			

Table continues on the next page...

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
TPM	Bus clock	TPM clock	TPM_CLKIN0, TPM_CLKIN1
PDB	Bus clock	—	—
PIT	Bus clock	—	—
LPTMR	Bus clock	LPO, OSCERCLK, MCGIRCLK, ERCLK32K	—
RTC	Bus clock	EXTAL32	—
Communication interfaces			
USB FS OTG	System clock	USB FS clock	—
USB DCD	Bus clock	—	—
SPI	System clock	—	DSPI_SCK
I2C	Bus clock	—	I2C_SCL
LPUART	Bus clock	LPUART clock	—
EMVSIM	Bus clock	EMVSIM clock	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—
TSI	Bus clock	LPO, ERCLK32K, MCGIRCLK	—

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 128-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

121 MAPBGA	100 LQFP	80 LQFP	64 LQFP	64 MAPBGA	Pin Name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
E9	63	52			PTB17	ND	Hi-Z	—	FS	N	N	Y
D9	64	53	41	D6	PTB18	ND	Hi-Z	—	FS	N	N	Y
C9	65	54	42	C7	PTB19	ND	Hi-Z	—	FS	N	N	Y
F10	66				PTB20	ND	Hi-Z	—	FS	N	N	Y
F9	67				PTB21	ND	Hi-Z	—	FS	N	N	Y
F8	68				PTB22	ND	Hi-Z	—	FS	N	N	Y
E8	69				PTB23	ND	Hi-Z	—	FS	N	N	Y
B9	70	55	43	D8	PTC0	ND	Hi-Z	—	FS	N	N	Y
D8	71	56	44	C6	PTC1/LLWU_P6	ND	Hi-Z	—	FS	N	N	Y
C8	72	57	45	B7	PTC2	ND	Hi-Z	—	FS	N	N	Y
B8	73	58	46	C8	PTC3/LLWU_P7	ND	Hi-Z	—	FS	N	N	Y
	74	59	47	E3	VFS	—	—	—	—	—	—	—
	75	60	48	E4	VDD	—	—	—	—	—	—	—
A8	76	61	49	B8	PTC4/LLWU_P8	ND	Hi-Z	—	FS	N	N	Y
D7	77	62	50	A8	PTC5/LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
C7	78	63	51	A7	PTC6/LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
B7	79	64	52	B6	PTC7	ND	Hi-Z	—	FS	N	N	Y
A7	80	65	53	A6	PTC8	ND	Hi-Z	—	FS	N	N	Y
D6	81	66	54	B5	PTC9	ND	Hi-Z	—	FS	N	N	Y
C6	82	67	55	B4	PTC10	ND	Hi-Z	—	FS	N	N	Y
C5	83	68	56	A5	PTC11/LLWU_P11	ND	Hi-Z	—	FS	N	N	Y
B6	84	69			PTC12	ND	Hi-Z	—	FS	N	N	Y
A6	85	70			PTC13	ND	Hi-Z	—	FS	N	N	Y
A5	86				PTC14	ND	Hi-Z	—	FS	N	N	Y
B5	87				PTC15	ND	Hi-Z	—	FS	N	N	Y
	88				VFS	—	—	—	—	—	—	—
	89				VDD	—	—	—	—	—	—	—
D5		71			PTC16	ND	Hi-Z	—	FS	N	N	Y
C4	90	72			PTC17	ND	Hi-Z	—	FS	N	N	Y

Table continues on the next page...

Table 17. QSPI signal description (continued)

Chip signal name	Module signal Name	Description	I/O
		second device in a dual-die package flash A or the second of the two flash devices that share IOFA.	
QSPI0B_SS0_B	PCSFB1	Peripheral Chip Select Flash B1. This signal is the chip select for the serial flash device B1. B1 represents the first device in a dual-die package flash B or the first of the two flash devices that share IOFB.	O
QSPI0A_SCLK	SCKFA	Serial Clock Flash A. This signal is the serial clock output to the serial flash device A.	O
QSPI0B_SCLK	SCKFB	Serial Clock Flash B. This signal is the serial clock output to the serial flash device B.	O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0 QSPI0A_DATA3 QSPI0A_DATA2 QSPI0A_DATA1 QSPI0A_DATA0	IOFA[7:0]	Serial I/O Flash A. These signals are the data I/O lines to/from the serial flash device A. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values.	I/O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0	IOFB[3:0]	Serial I/O Flash B. These signals are the data I/O lines to/from the serial flash device B. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values.	I/O
QSPI0A_DQS	DQSFA	Data Strobe signal Flash A. Data strobe signal for port A. Some flash vendors provide the DQS signal to which the read data is aligned in DDR mode.	I

4.3.5 Analog

Table 18. ADC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC0_DP[1:0]	DADP1–DADP0	Differential analog channel inputs	I
ADC0_DM[1:0]	DADM1–DADM0	Differential Analog Channel Inputs	I
ADC0_SEn	ADn	Single-Ended Analog Channel Inputs[1]	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog power supply	I
VSSA	V_{SSA}	Analog ground	I

1. See ADC channel assignment for the n.

Table 19. CMP0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CMP0_INn, n=[5,3:0]	INn, n=[5,3:0]	Analog voltage inputs, see CMP input connection for more details about the n.	I
CMP0_OUT	CMPO	Comparator output	O

NOTE

There is no CMP0_IN[4] coming from pad.

Table 20. DAC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
DAC0_OUT	—	DAC output	O

Table 21. VREF Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated Voltage Reference output	O

Table 34. LPUART1 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
LPUART1_TX	LPUART_TX	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART1_RX	LPUART_RX	Receive Data	I

Table 35. LPUART2 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART2_CTS_b	LPUART_CTS	Clear to Send	I
LPUART2_RTS_b	LPUART_RTS	Request to send	O
LPUART2_TX	LPUART_TX	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART2_RX	LPUART_RX	Receive Data	I

Table 36. FlexIO signal descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dn(n=0-31)	FXIO_Dn (n=0...31)	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

Table 37. EMVSIM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM0_ CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM0_ IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM0_ PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM0_ RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM0_ VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O

Table 38. EMVSIM1 signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM1_ CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM1_ IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O

Table continues on the next page...

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11/ LLWU_P11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1/ LLWU_P0	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2/ LLWU_P13	PTD0/ LLWU_P12	VSS	PTE2/ LLWU_P1	PTC1/ LLWU_P6	PTB19	PTC3/ LLWU_P7	C
D	PTE5	PTE3	VDDIO_E	PTA0	PTA1	PTB18	PTB8	PTC0	D
E	USB0_DP	PTE4/ LLWU_P2	VSS	VDD	PTA2	PTB0/ LLWU_P5	PTB6	PTB7	E
F	USB0_DM	USB_VDD	VSS	VREF_OUT/ CMP0_IN5/ ADC0_SE22	RTC_WAKEUP_B	PTB5	PTB4	RESET_b	F
G	VSSA	VDDA	ADC0_DM1	DAC0_OUT/ ADC0_SE23	VBAT	PTA4/ LLWU_P3	VSS	PTA19	G
H	ADC0_DP1	VREFL	VREFH	XTAL32	EXTAL32	PTA3	VDD	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 8. KL82 64-pin MAPBGA pinout diagram

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very Low Power Run Wait current, core disabled, system at 2 MHz, bus and flash at 0.5 MHz, all peripheral clocks disabled, VDD = 3 V	25 °C	225	277.03	µA	6
I_{DD_VLPW}	Very Low Power Run Wait current, core disabled, system at 125 kHz, bus and flash at 31.25 kHz, all peripheral clocks disabled, VDD = 3 V	25 °C	31	61.00	µA	6
I_{IDD_PSTOP2}	Partial stop 2, core and system clock disabled, bus and flash at 12 MHz, VDD = 3 V	25 °C	2.9	4.26	mA	7
I_{DD_STOP}	Stop mode current at 3.0 V	25 °C and below	273	304.31	µA	
		50°C	306	384.47		
		85 °C	440	589.29		
		105 °C	625	925.33		
I_{DD_VLPS}	VLPS current, VDD= 3 V	25 °C and below	5.82	15.42	µA	
		50 °C	14.41	29.41		
		85 °C	56.47	99.67		
		105°C	121.54	223.54		
I_{DD_VLPS}	VLPS current, VDD= 1.8 V	25 °C and below	5.61	15.21	µA	
		50 °C	14.01	29.01		
		85 °C	55.8	99.00		
		105 °C	120.14	222.14		
I_{DD_LLS3}	LLS3 current, all peripheral disabled, VDD = 3 V	25 °C and below	3.68	7.88	µA	
		50 °C	8.28	15.48		
		70 °C	13.52	22.52		
		85 °C	20.91	39.55		
		105 °C	40.27	67.79		
I_{DD_LLS3}	LLS3 with RTC current, VDD = 3 V	25 °C and below	5.08	9.28	µA	
		50 °C	10.31	17.51		
		70 °C	15.76	24.76		
		85 °C	22.8	41.44		
		105 °C	43.5	71.02		
I_{DD_LLS3}	LLS3 with RTC current, VDD = 1.8 V	25 °C and below	5.02	9.22	µA	
		50 °C	10.06	17.26		

Table continues on the next page...

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
		70 °C	15.15	24.15		
		85 °C	21.88	40.52		
		105 °C	41.82	69.34		
I_{DD_LLS2}	LLS2 current, all peripheral disabled, VDD = 3 V	25 °C and below	3.37	6.67	µA	
		50 °C	6.82	13.42		
		70 °C	11.13	20.73		
		85 °C	16.84	31.46		
		105 °C	32.93	48.89		
I_{DD_LLS2}	LLS2 with RTC current, VDD = 3 V	25 °C and below	4.49	7.79	µA	
		50 °C	9.07	16.27		
		70 °C	12.98	22.58		
		85 °C	17.88	32.50		
		105 °C	35.98	51.94		
I_{DD_LLS2}	LLS2 with RTC current, VDD = 1.8 V	25 °C and below	4.47	7.77	µA	
		50 °C	8.79	15.99		
		70 °C	12.27	21.87		
		85 °C	17.77	32.39		
		105 °C	34.31	50.27		
I_{DD_VLLS3}	VLLS3 current, all peripheral disable, VDD = 3 V	25 °C and below	2	3.80	µA	
		50 °C	3.76	7.36		
		70 °C	7.19	12.82		
		85 °C	12.62	21.10		
		105 °C	27.61	42.33		
I_{DD_VLLS3}	VLLS3 with RTC current, VDD = 3 V	25 °C and below	2.83	4.63	µA	
		50 °C	4.62	8.22		
		70 °C	8.38	14.01		
		85 °C	14.06	21.54		
		105 °C	29.81	44.53		
I_{DD_VLLS3}	VLLS3 with RTC current, VDD = 1.8 V	25 °C and below	2.59	4.39	µA	
		50 °C	4.28	7.88		
		70 °C	7.89	13.52		
		85 °C	13.33	20.81		
		105 °C	28.34	43.06		

Table continues on the next page...

5.3.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for "EMC design"

5.3.2.8 Capacitance attributes

Table 48. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3.3 Switching specifications

5.3.3.1 Device clock specifications

Table 49. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	96	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	72	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FBUS}	Bus interface clock for QSPI	36	—	MHz	
f_{FLASH}	Flash clock	—	24	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FBUS}	Bus interface clock for QSPI	2	—	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	16	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

Board type	Symbol	Description	121 MAPBGA	80 LQFP	64 MAPBGA	Unit	Notes
		junction to package top outside center (natural convection)					
—	$R_{\theta JB\_CSB}$	Thermal characterization parameter, junction to package top outside center (natural convection)	14.6	—	19.5	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
5. Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

5.4 Peripheral operating requirements and behaviors

5.4.1 Core modules

5.4.1.1 Debug trace timing specifications

Table 52. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

Table 54. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		(DRS=01, DMX32=1) 1464 × f_{ints_ut}					
		Mid-high range (DRS=10, DMX32=1) 2197 × f_{ints_ut}	54.93	79.09	91.53		
		High range (DRS=11, DMX32=1) 2929 × f_{ints_ut}	73.23	105.44	122.02		
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f_{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency		180	—	360	MHz	
f_{vcoclk}	PLL output frequency		90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency		90	—	180	MHz	
I_{pll}	PLL operating current • VCO at 184 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 23)		—	2.8	—	mA	8
I_{pll}	PLL operating current • VCO at 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	3.6	—	mA	8

Table continues on the next page...

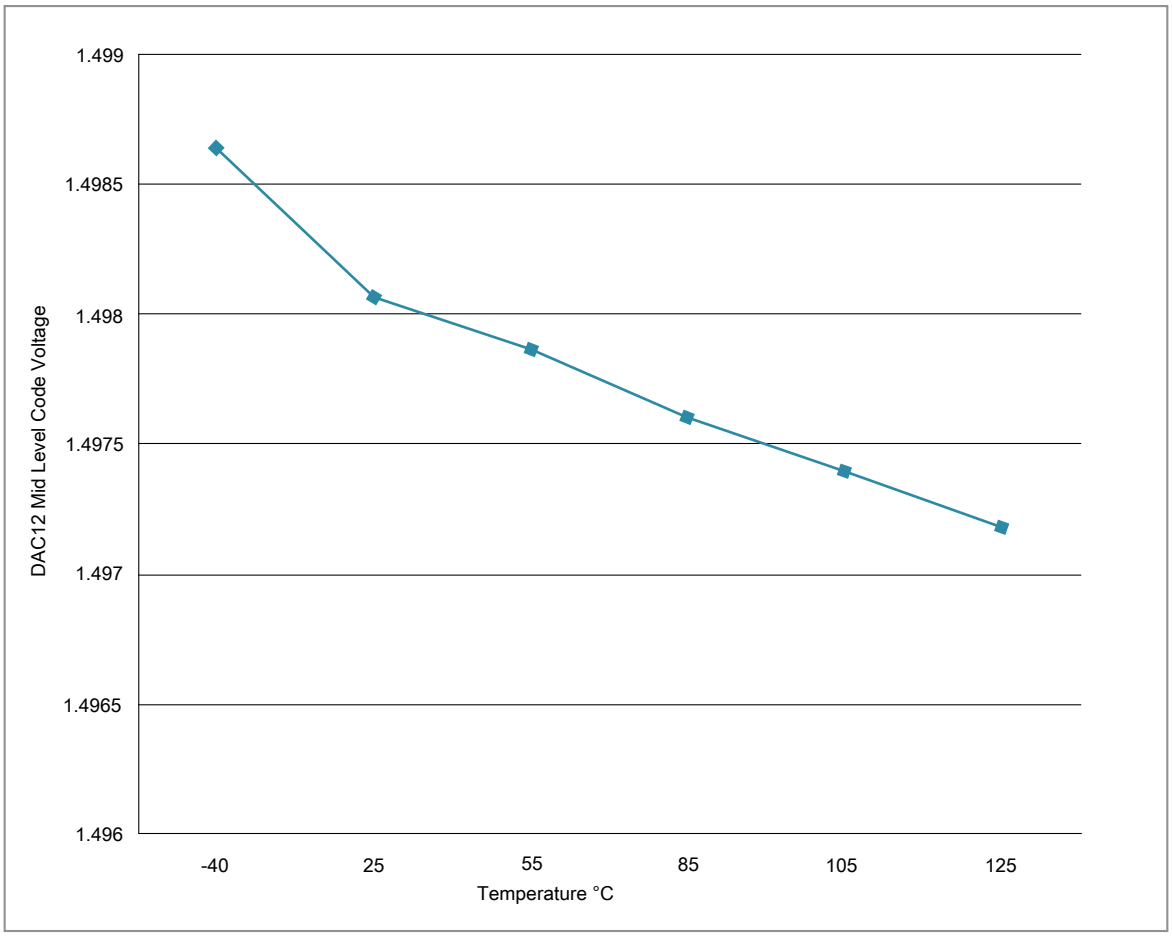

Figure 35. Offset at half scale vs. temperature

5.4.5.4 Voltage reference electrical specifications

Table 76. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

NOTE

The MCGPLLCLK meets the USB jitter and signaling rate specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The IRC48M meets the USB jitter and signaling rate specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB signaling rate specifications for certification in Host mode operation.

5.4.7.3 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 84. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	24	MHz	1
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	15.0	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	1.0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15.8	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The SPI can run at a maximum frequency of 24 MHz serial clocks on PORTE interface, and up to 18 MHz on other PORT interfaces
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 89. I ^{2}C 1Mbit/s timing (continued)

Characteristic	Symbol	Minimum	Maximum	Unit
Fall time of SDA and SCL signals	t_f	20 +0.1C_b[1]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. C_b = total capacitance of the one bus line in pF.

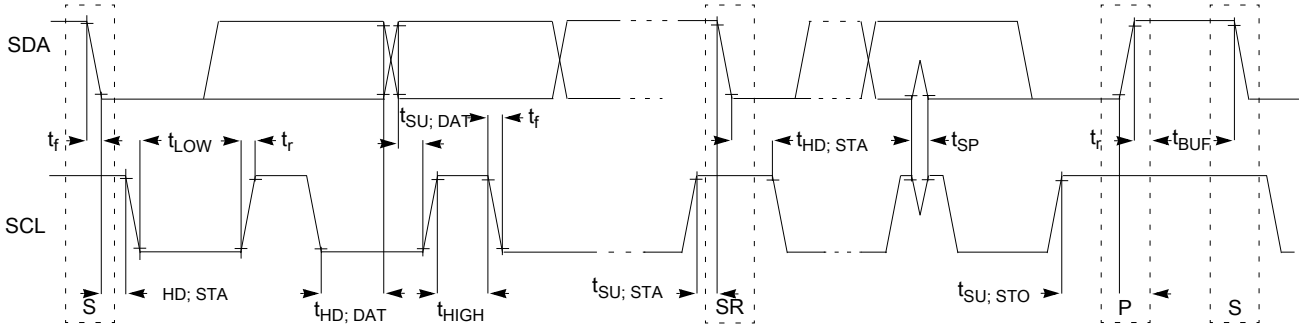

Figure 44. Timing definition for devices on the I^{2}C bus

5.4.7.6 LPUART switching specifications

See General switching specifications.

5.4.8 Human-machine interfaces (HMI)

5.4.8.1 TSI electrical specifications

Table 90. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	µA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	µA
TSI_EN	Power consumption in enable mode	—	100	—	µA
TSI_DIS	Power consumption in disable mode	—	1.2	—	µA
TSI_TEN	TSI analog enable time	—	66	—	µs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V