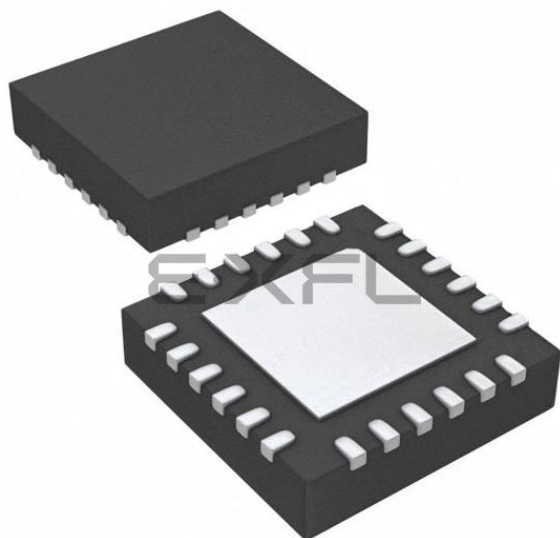




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg308f32g-b-qfn24

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG308 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32HG308F32G-B-QFN24	32	8	25	1.98 - 3.8	-40 - 85	QFN24
EFM32HG308F64G-B-QFN24	64	8	25	1.98 - 3.8	-40 - 85	QFN24

Adding the suffix 'R' to the part number (e.g. EFM32HG308F32G-B-QFN24R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150 ¹	$^{\circ}\text{C}$
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

¹Based on programmed devices tested for 10000 hours at 150°C . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

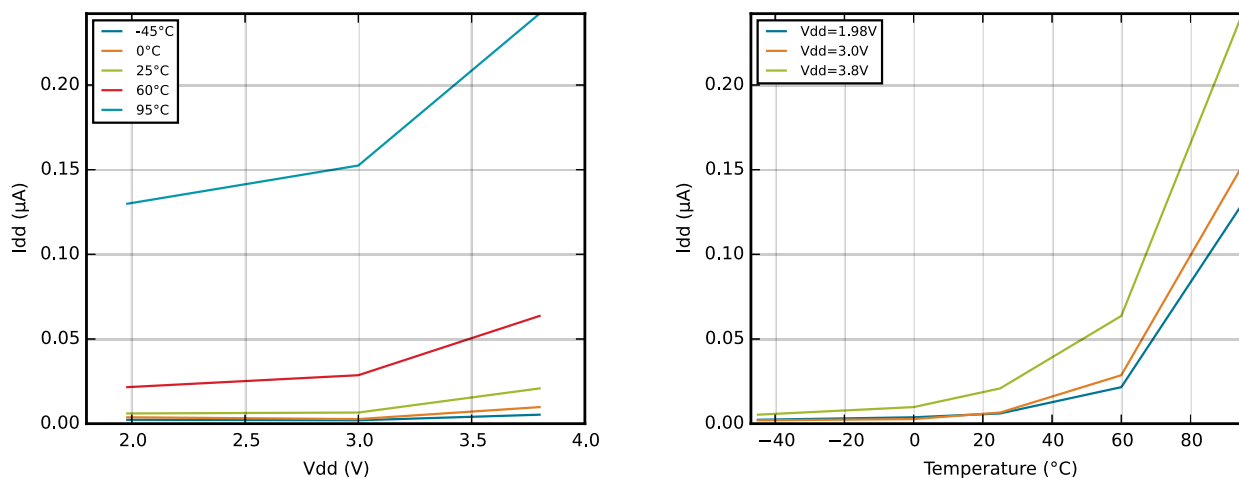
Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			25	MHz
f_{AHB}	Internal AHB clock frequency			25	MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	µA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		85	91	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		86	92	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		51	55	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		52	56	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		53	57	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		54	58	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		56	59	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		57	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		58	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		59	63	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		106	114	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		114	126	µA/ MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		0.9	1.35	µA

3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

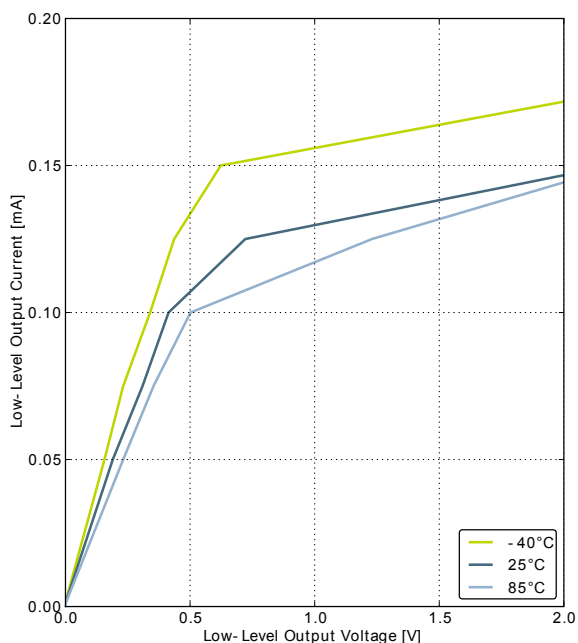
Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

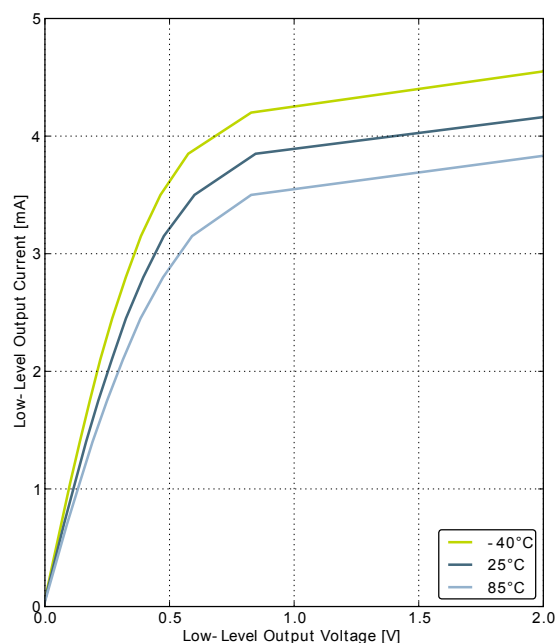
3.6 Power Management

The EFM32HG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

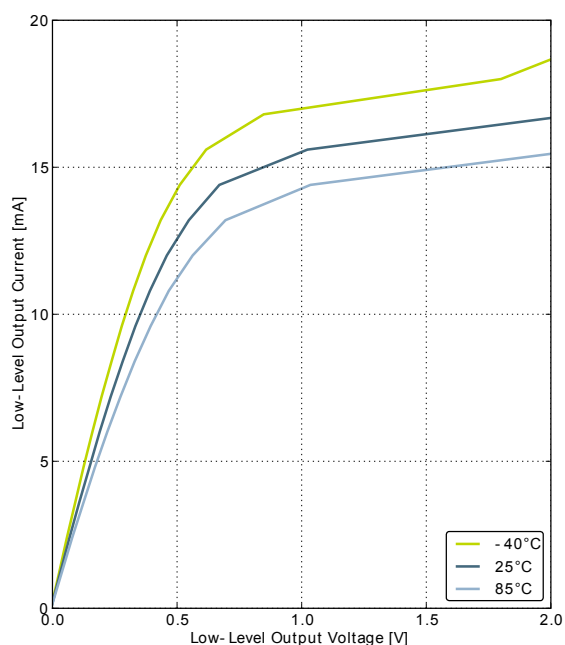
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



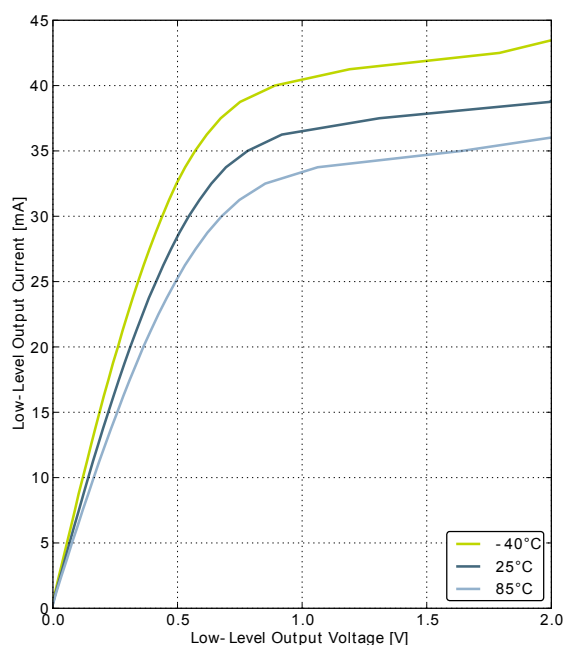
GPIO_Px_CTRL DRIVEMODE = LOWEST



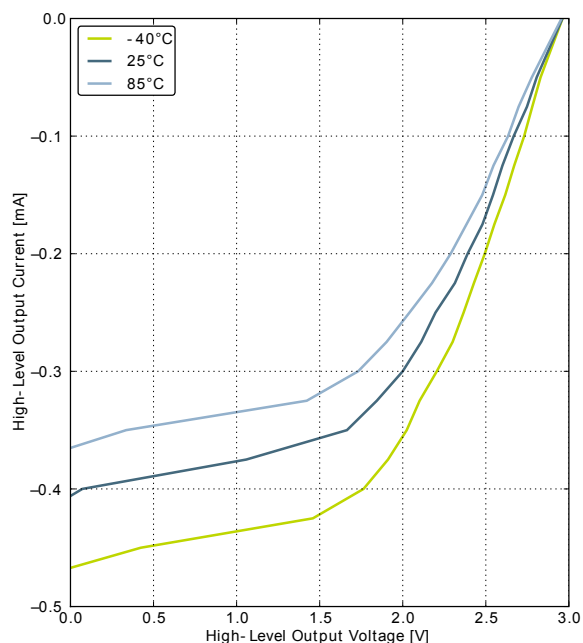
GPIO_Px_CTRL DRIVEMODE = LOW



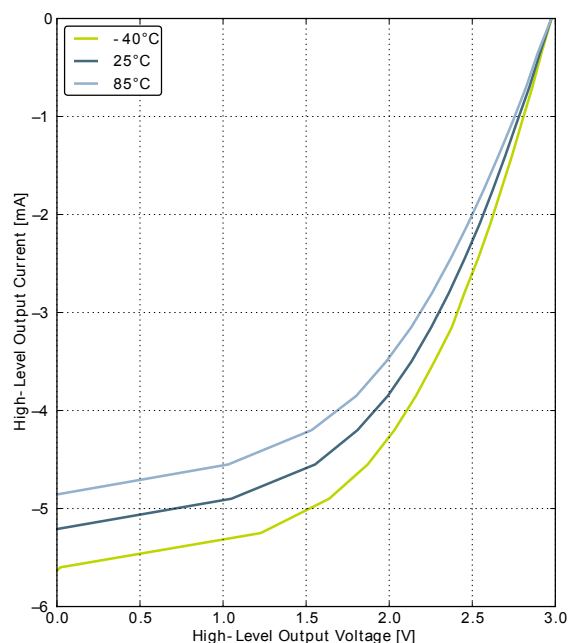
GPIO_Px_CTRL DRIVEMODE = STANDARD



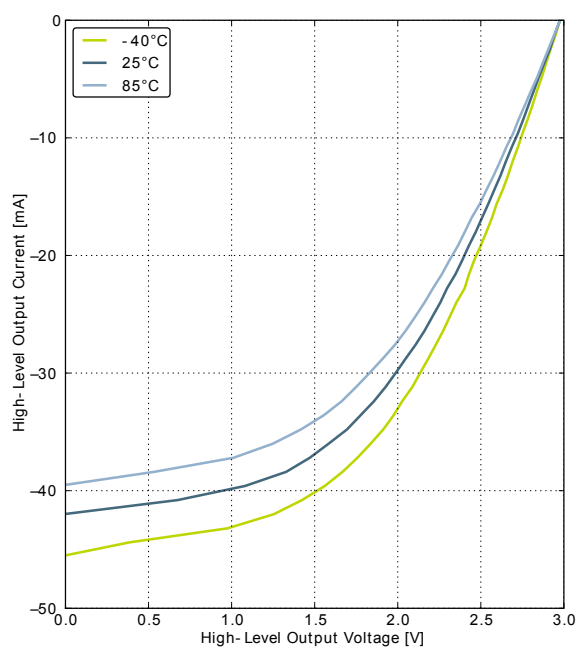
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage

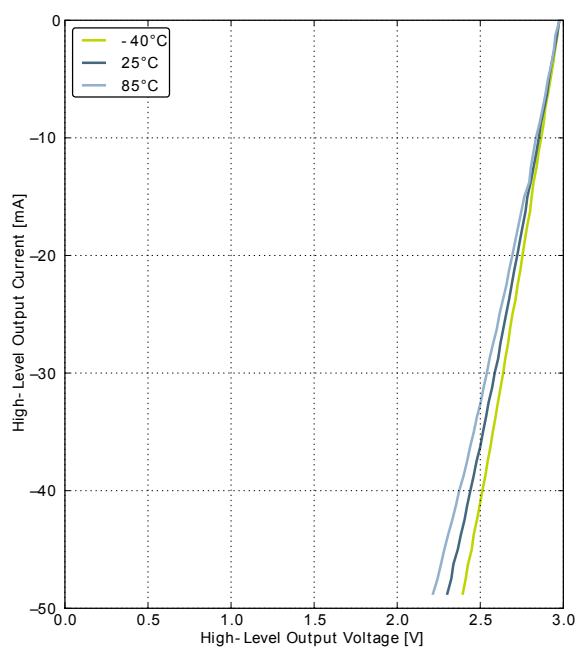
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



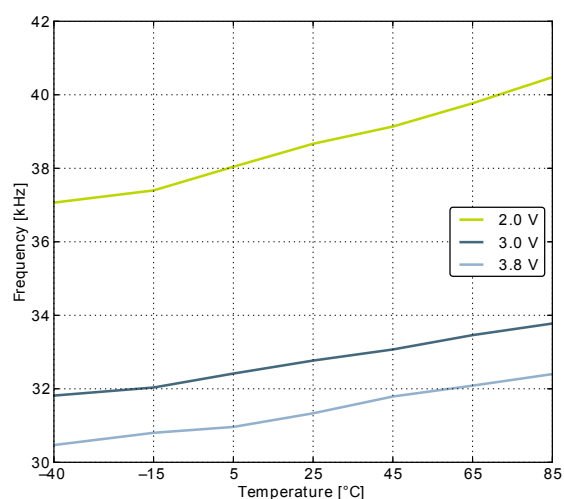
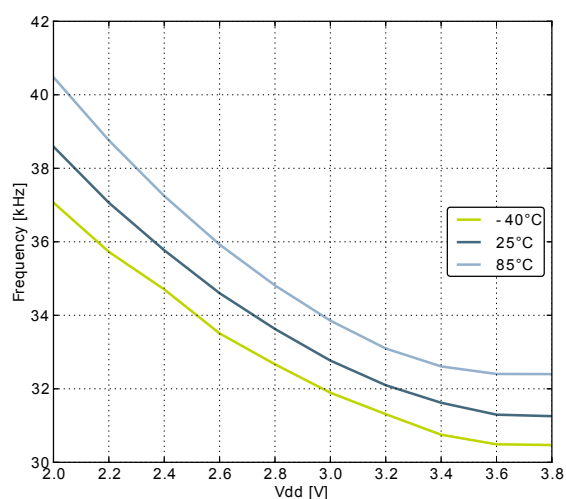
GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		31.3	32.768	34.3	kHz
t_{LFRCO}	Startup time not including software calibration			150		μs
I_{LFRCO}	Current consumption			361	492	nA
TUNESTEP _{LFRCO}	Frequency step for LSB change in TUNING value			202		Hz

Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.6 USHFRCO

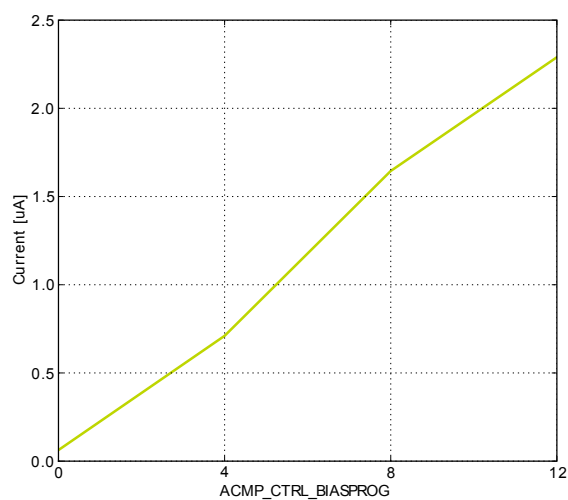
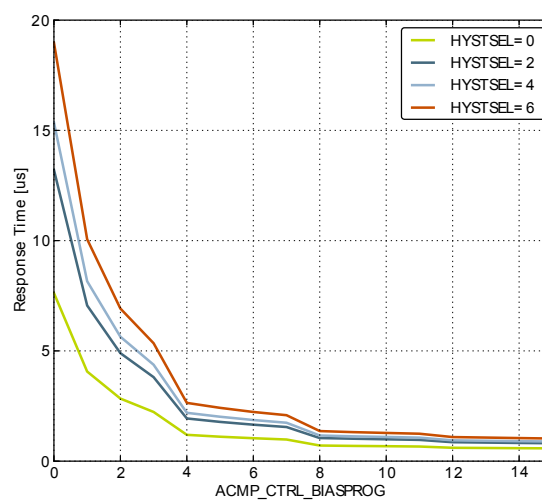
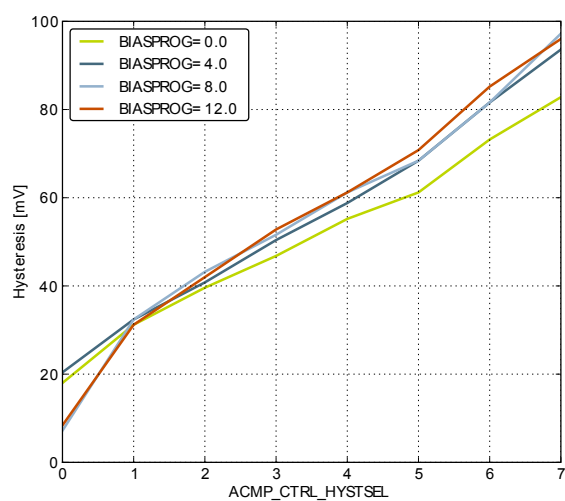
Table 3.13. USHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{USHFRCO}	Oscillation frequency	No Clock Recovery, Full Temperature and Supply Range, 48 MHz band	47.10	48.00	48.90	MHz
		No Clock Recovery, Full Temperature and Supply Range, 24 MHz band	23.73	24.00	24.32	MHz
		No Clock Recovery, 25°C, 3.3V, 48 MHz band	47.50	48.00	48.50	MHz
		No Clock Recovery, 25°C, 3.3V, 24 MHz band	23.86	24.00	24.16	MHz
		USB Active with Clock Recovery, Full Temperature and Supply Range	47.88	48.00	48.12	MHz
TC _{USHFRCO}	Temperature coefficient	3.3V		0.0175		%/°C
VC _{USHFRCO}	Supply voltage coefficient	25°C		0.0045		%/V
I _{USHFRCO}	Current consumption	f _{USHFRCO} = 48 MHz	1.21	1.36	1.48	mA
		f _{USHFRCO} = 24 MHz	0.81	0.92	1.02	mA

3.9.7 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{ULFRCO}	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
TC _{ULFRCO}	Temperature coefficient			0.05		%/°C
VC _{ULFRCO}	Supply voltage coefficient			-18.2		%/V

Figure 3.26. ACMP Characteristics, $V_{dd} = 3V$, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1**Current consumption, HYSTSEL = 4****Response time , $V_{cm} = 1.25V$, CP+ to CP- = 100mV****Hysteresis**

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 40). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13			PB11				Analog comparator ACMP0, digital output.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0				PF2				Clock Management Unit, clock output number 0.
CMU_CLK1			PE12	PB11				Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL					PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0				PC0	PF0	PE12	I2C0 Serial Data input / output.
LEU0_RX		PB14		PF1	PA0	PC15		LEUART0 Receive input.
LEU0_TX		PB13		PF0	PF2	PC14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0		PA0			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		PB11			Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0		PC14	PF2				Peripheral Reflex System PRS, channel 0.
PRS_CH1			PC15	PE12				Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0			PE13				Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1			PA0				Peripheral Reflex System PRS, channel 3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1	PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2					PC1	PF2	PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI1		PC14					PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15					PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0				PB7				Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8				Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0				PF2				Timer 2 Capture Compare input / output channel 0.
TIM2_CC1				PE12				Timer 2 Capture Compare input / output channel 1.
TIM2_CC2				PE13				Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12			PC15	PB13	PB13	PE12	USART0 clock input / output.
US0_CS	PE13			PC14	PB14	PB14	PE13	USART0 chip select input / output.
US0_RX				PE12	PB8	PC1	PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX				PE13	PB7	PC0	PC0	USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0	PC15	PB11			USART1 clock input / output.
US1_CS	PB8		PF1	PC14	PC14	PC0		USART1 chip select input / output.
US1_RX	PC1				PA0			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				PF2	PC1		USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PC14							USB D- pin.
USB_DMPU	PA0							USB D- Pullup control.
USB_DP	PC15							USB D+ pin.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

4.3 GPIO Pinout Overview

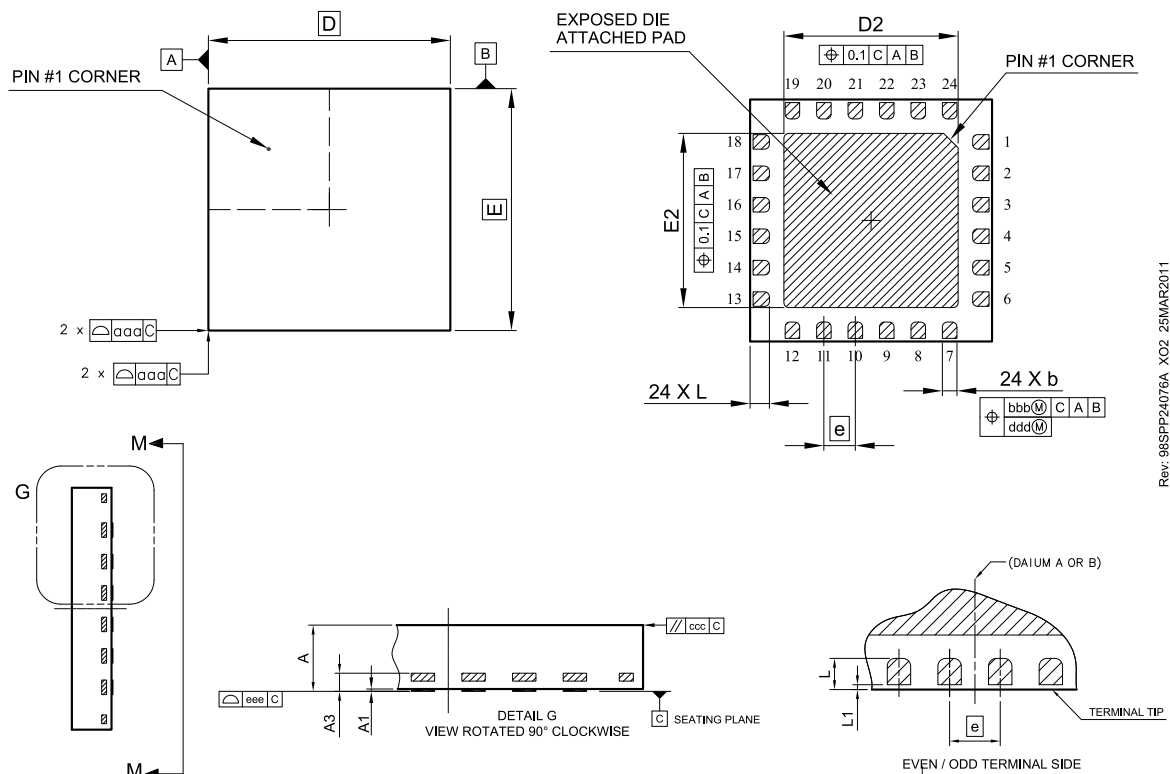
The specific GPIO pins available in *EFM32HG308* is shown in Table 4.3 (p. 42) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

4.4 QFN24 Package

Figure 4.2. QFN24



Rev: 98SP24076A_X02_25MAR2011

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN24 PCB Land Pattern

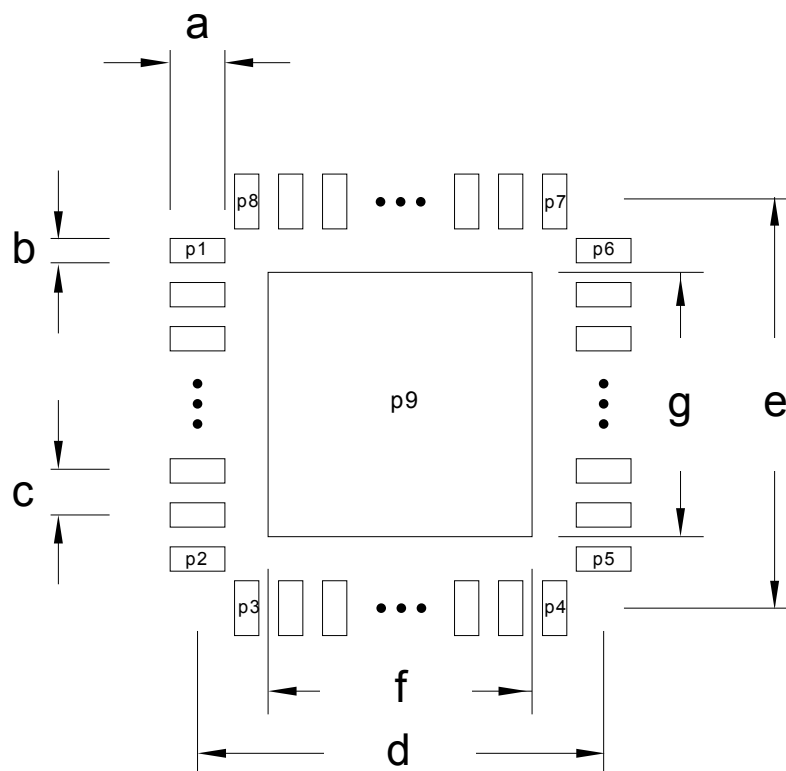
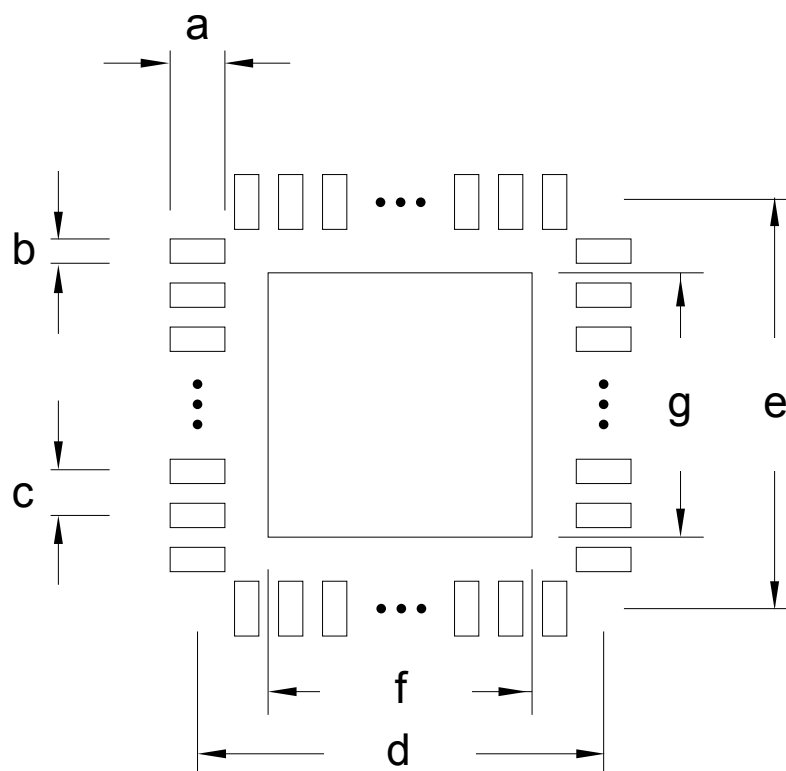


Table 5.1. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	0.80	P1	1	P8	24
b	0.30	P2	6	P9	25
c	0.65	P3	7	-	-
d	5.00	P4	12	-	-
e	5.00	P5	13	-	-
f	3.60	P6	18	-	-
g	3.60	P7	19	-	-

Figure 5.2. QFN24 PCB Solder Mask**Table 5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)**

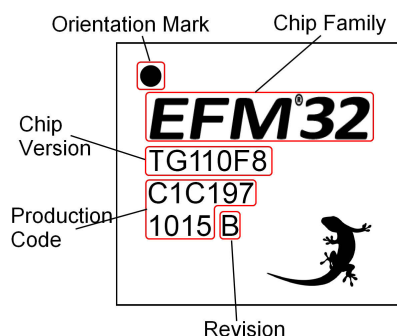
Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.92	e	5.00
b	0.42	f	3.72
c	0.65	g	3.72
d	5.00	-	-

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 47) .

6.3 Errata

Please see the errata document for EFM32HG308 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

7 Revision History

7.1 Revision 1.00

December 4th, 2015

Updated all specs with results of full characterization.

Updated part number to revision B.

Added the USB electrical specifications table.

7.2 Revision 0.91

May 6th, 2015

Updated current consumption table for energy modes.

Updated GPIO max leakage current.

Updated startup time for HFXO and LFXO.

Updated current consumption for HFRCO and LFRCO.

Updated ADC current consumption.

Updated IDAC characteristics tables.

Updated ACMP internal resistance.

Updated VCMP current consumption.

7.3 Revision 0.90

March 16th, 2015

Note

This datasheet revision applies to a product under development. It's characteristics and specifications are subject to change without notice.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Updated GPIO electrical characteristics.

Updated Max ESR_{HFXO} value for Crystal Frequency of 25 MHz.

Updated LFRCO plots.

Updated HFRCO table and plots.

Updated ADC table and temp sensor plot.

Added DMA current in Digital Peripherals section.

Updated block diagram.

Updated Package dimensions table.

Corrected leadframe type to matte-Sn.

7.4 Revision 0.20

December 11th, 2014

Preliminary Release.

B Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:

<http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.

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