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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

·XF

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg308f32g-b-qfn24r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG308 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32HG308F32G-B-QFN24	32	8	25	1.98 - 3.8	-40 - 85	QFN24
EFM32HG308F64G-B-QFN24	64	8	25	1.98 - 3.8	-40 - 85	QFN24

Adding the suffix 'R' to the part number (e.g. EFM32HG308F32G-B-QFN24R) denotes tape and reel.

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2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32HG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32HG308 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32HG Reference Manual*.

A block diagram of the EFM32HG308 is shown in Figure 2.1 (p. 3) .



Figure 2.1. Block Diagram

2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and a Micro Trace Buffer (MTB) for data/instruction tracing.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is

2.1.11 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (US-ART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.13 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0042 is pre-programmed in the device at factory. The bootloader enables users to program the EFM32 through a UART or a USB CDC class virtual UART without the need for a debugger. The autobaud feature, interface and commands are described further in the application note.

2.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

2.1.18 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB} =25°C and V_{DD} =3.0 V, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
T _{STG}	Storage tempera- ture range		-40		150 ¹	°C
Τ _S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V _{DDMAX}	External main sup- ply voltage		0		3.8	V
VIOPIN	Voltage on any I/O pin		-0.3		V _{DD} +0.3	V

¹Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Тур	Мах	Unit
T _{AMB}	Ambient temperature range	-40		85	°C
V _{DDOP}	Operating supply voltage	1.98		3.8	V
f _{APB}	Internal APB clock frequency			25	MHz
f _{AHB}	Internal AHB clock frequency			25	MHz

Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz



3.4.2 EM1 Current Consumption

Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz



3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.





3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.



3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Тур	Мах	Unit
t _{EM10}	Transition time from EM1 to EM0		0		HF- CORE- CLK cycles
t _{EM20}	Transition time from EM2 to EM0		2		μs
t _{EM30}	Transition time from EM3 to EM0		2		μs
t _{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

The EFM32HG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
	BOD threshold on	EMO	1.74		1.96	V
VBODextthr-	ply voltage	EM2	1.71	1.86	1.98	V
V _{BODextthr+}	BOD threshold on rising external sup- ply voltage			1.85		V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capaci- tor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF
C _{USB_VREGO}	USB voltage regu- lator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		μF
C _{USB_VREGI}	USB voltage regula- tor in decoupling ca- pacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		μF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Тур	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
		T _{AMB} <150°C	10000			h
RET _{FLASH}	Flash data retention	T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
tw_prog	Word (32-bit) pro- gramming time		20			μs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage dur- ing flash erase and write		1.98		3.8	V

¹Measured at 25°C

3.8 General Purpose Input Output

Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
Vices	Output high volt- age (Production test	Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
VIOOH	DRIVEMODE = STANDARD)	Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V
		Sourcing 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V _{DD}			V
		Sourcing 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V _{DD}			V
		Sinking 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V _{DD}		V
		Sinking 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V _{DD}		V
		Sinking 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V _{DD}		V
Vice	Output low voltage (Production test	Sinking 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V _{DD}		V
VIOOL	DRIVEMODE = STANDARD)	Sinking 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V _{DD}	V
		Sinking 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V _{DD}	V
		Sinking 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V _{DD}	V
		Sinking 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V _{DD}	V
I _{IOLEAK}	Input leakage cur- rent	High Impedance IO connected to GROUND or Vdd		±0.1	±40	nA
R _{PU}	I/O pin pull-up resis- tor			40		kOhm



Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = STANDARD



Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = HIGH



Figure 3.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature



3.9.5 AUXHFRCO

Table 3.12. AUXHFRCO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		21 MHz frequency band	20.37	21.0	21.63	MHz
	Oscillation frequen-	14 MHz frequency band	13.58	14.0	14.42	MHz
f _{AUXHFRCO}	cy, V_{DD} = 3.0 V,	11 MHz frequency band	10.67	11.0	11.33	MHz
	T _{AMB} =25°C	7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
t _{AUXHFRCO_settlir}	_g Settling time after start-up	f _{AUXHFRCO} = 14 MHz		0.6		Cycles
		21 MHz frequency band		52.8		kHz
	Frequency step	14 MHz frequency band		36.9		kHz
TUNESTEP _{AUX} HFRCO	for LSB change in	11 MHz frequency band		30.1		kHz
	I UNING value	7 MHz frequency band		18.0		kHz
		1 MHz frequency band		3.4		kHz

3.10 Analog Comparator (ACMP)

Table 3.15. ACMP

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V _{ACMPIN}	Input voltage range		0		V _{DD}	V
V _{ACMPCM}	ACMP Common Mode voltage range		0		V _{DD}	V
		BIASPROG=0b0000, FULL- BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	μA
I _{ACMP}	Active current	BIASPROG=0b1111, FULL- BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	μA
		BIASPROG=0b1111, FULL- BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
IACMPREF	Current consump- tion of internal volt-	Internal voltage reference off. Using external voltage refer- ence		0		μA
	age reference	Internal voltage reference		5		μA
VACMPOFFSET	Offset voltage	BIASPROG= 0b1010, FULL- BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
V _{ACMPHYST}	ACMP hysteresis	Programmable		17		mV
		CSRESSEL=0b00 in ACMPn_INPUTSEL		40		kOhm
D	Capacitive Sense	CSRESSEL=0b01 in ACMPn_INPUTSEL		70		kOhm
RCSRES	Internal Resistance	CSRESSEL=0b10 in ACMPn_INPUTSEL		101		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		132		kOhm
t _{acmpstart}	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 33). $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

 $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$

(3.1)

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Alternate			LOC	ATION	N			
Functionality	0	1	2	3	4	5	6	Description
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1	PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2					PC1	PF2	PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI1		PC14					PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15					PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0				PB7				Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8				Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0				PF2				Timer 2 Capture Compare input / output channel 0.
TIM2_CC1				PE12				Timer 2 Capture Compare input / output channel 1.
TIM2_CC2				PE13				Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12			PC15	PB13	PB13	PE12	USART0 clock input / output.
US0_CS	PE13			PC14	PB14	PB14	PE13	USART0 chip select input / output.
								USART0 Asynchronous Receive.
US0_RX				PE12	PB8	PC1	PC1	USART0 Synchronous mode Master Input / Slave Output (MISO).
US0 TX				PE13	PB7	PC0	PC0	USART0 Asynchronous Transmit.Also used as receive in- put in half duplex communication.
								USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0	PC15	PB11			USART1 clock input / output.
US1_CS	PB8		PF1	PC14	PC14	PC0		USART1 chip select input / output.
								USART1 Asynchronous Receive.
US1_RX	PC1				PA0			USART1 Synchronous mode Master Input / Slave Output (MISO).
US1 TX	PC0				PF2	PC1		USART1 Asynchronous Transmit.Also used as receive in- put in half duplex communication.
								USART1 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PC14							USB D- pin.
USB_DMPU	PA0							USB D- Pullup control.
USB_DP	PC15							USB D+ pin.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and reg- ulator output

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32HG308* is shown in Table 4.3 (p. 42). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.



Table 4.4. QFN24 (Dimensions in mm)

Symbol	A	A1	A 3	b	D	E	D2	E2	е	L	L1	aaa	bbb	ссс	ddd	eee
Min	0.80	0.00		0.25			3.50	3.50		0.35	0.00					
Nom	0.85	-	0.203 REF	0.30	5.00 BSC	5.00 BSC	3.60	3.60	0.65 BSC	0.40		0.10	0.10	0.10	0.05	0.08
Max	0.90	0.05		0.35			3.70	3.70		0.45	0.10					

The QFN24 package uses matte-Sn post plated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx



Figure 5.2. QFN24 PCB Solder Mask



Table 5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
а	0.92	е	5.00
b	0.42	f	3.72
С	0.65	g	3.72
d	5.00	-	-

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 47).

6.3 Errata

Please see the errata document for EFM32HG308 for description and resolution of device erratas. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

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