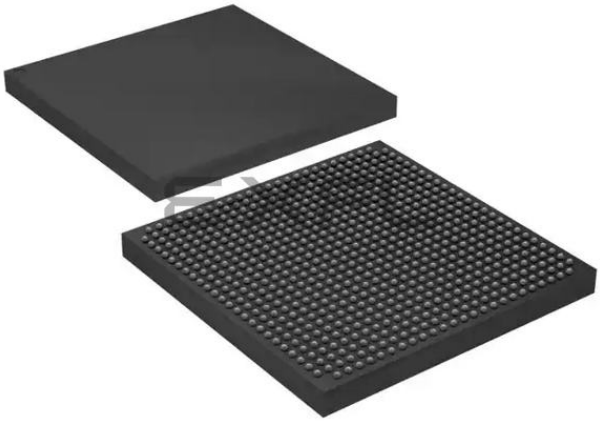

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	-
Number of Gates	-
Voltage - Supply	-
Mounting Type	Surface Mount
Operating Temperature	-
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k250efi672-3

- Software design support and automatic place-and-route provided by the Altera MAX+PLUS® II development system for 486- and Pentium-based PCs, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-compatibility (with other FLEX 10KE devices) across device densities and pin counts
- Additional design entry and simulation support provided by electronic design interchange format (EDIF) 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular electronic design automation (EDA) tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2), (3)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			
EPF10K50E	102	147	189	191		254			
EPF10K100B		147	189	191					
EPF10K100E		147	189	191	274	338			
EPF10K130E			186			369			413
EPF10K200E							470	470	470
EPF10K250E							470	470	470

Notes:

(1) Contact Altera Customer Marketing for up-to-date information on package availability.

(2) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), pin-grid array (PGA), and ball-grid array (BGA).

(3) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices. MAX+PLUS II software versions 9.1 and higher provide features to help use only the common pins.

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm^2)	484	936	1,197	289	1,225	529	3,904	2,025	729

Table 6 shows FLEX 10KE performance for more complex designs. These designs are available as Altera MegaCore™ functions.

Table 6. FLEX 10KE Performance for Complex Designs

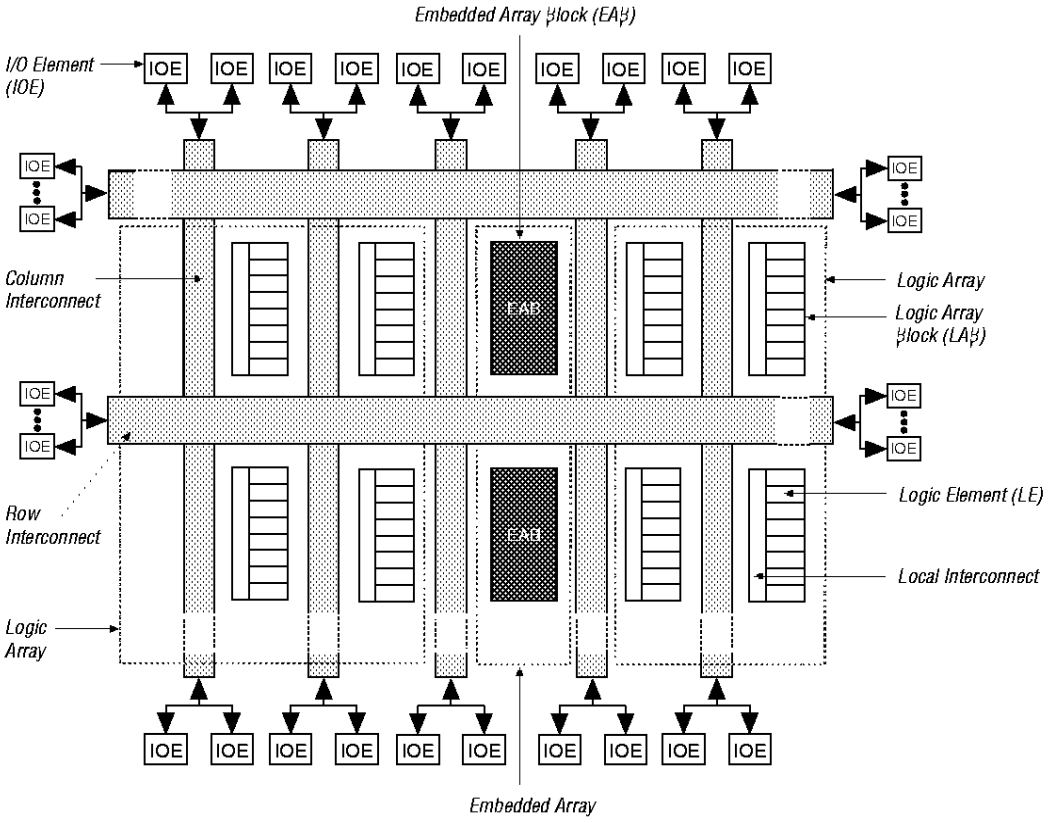
Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit, 8-tap parallel finite impulse response (FIR) filter	592	138	128	103	MSPS
8-bit, 512-point fast Fourier transform (FFT) function	1,845	60	72	83	µs
		76	66	56	MHz
a16450 universal asynchronous receiver/transmitter (UART)	479	42	39	34	MHz

The FLEX 10KE architecture is similar to that of embedded gate arrays, which is the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

Figure 1 shows a block diagram of the FLEX 10KE architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Figure 1. FLEX 10KE Device Block Diagram



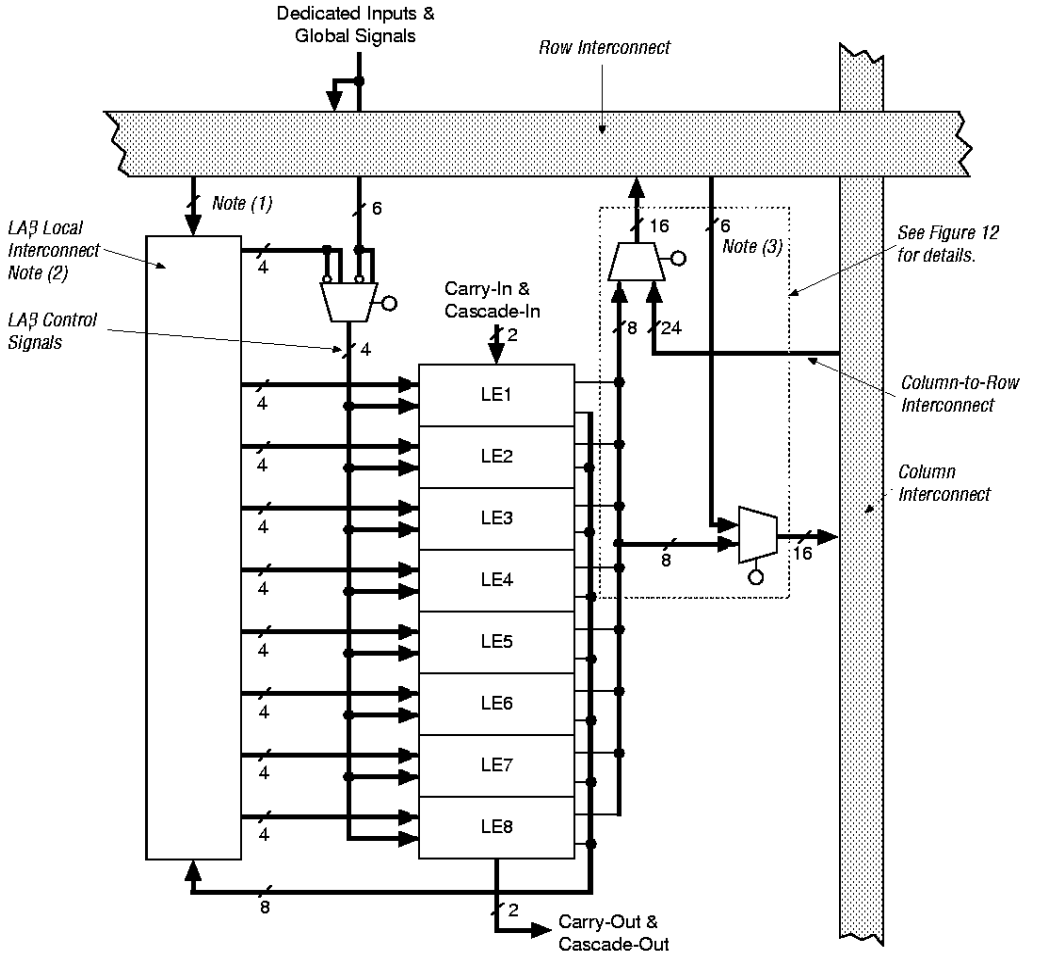
FLEX 10KE devices provide six dedicated inputs that drive the control inputs of the flipflops to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 3). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

A LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 6).

Figure 6. FLEX 10KE LAβ



Notes:

(1) EPF10K30E and EPF10K50E devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 26.

(2) EPF10K30E and EPF10K50E devices have 30 LAB local interconnect channels; EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 34.

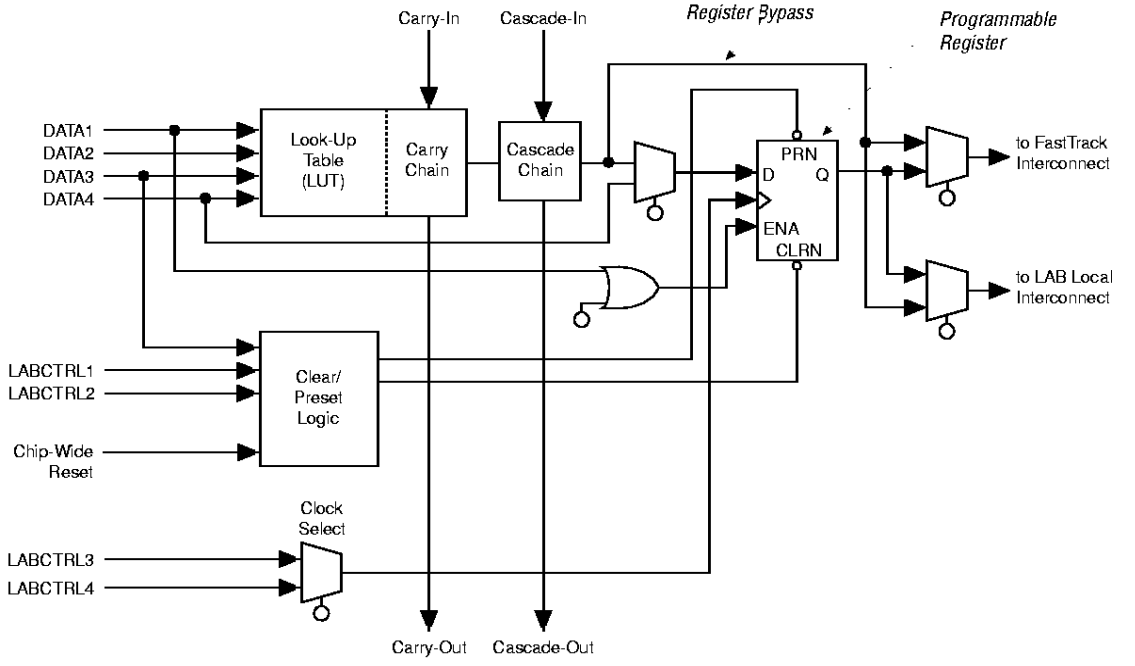
(3) In EPF10K100B devices, four row channels can drive column channels at each intersection.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see Figure 7).

Figure 7. FLEX 10KE Logic Element



In addition to the six clear and preset modes, FLEX 10KE devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 11 shows examples of how to enter a design for the desired functionality.

Figure 11. FLEX 10KE LE Clear & Preset Modes

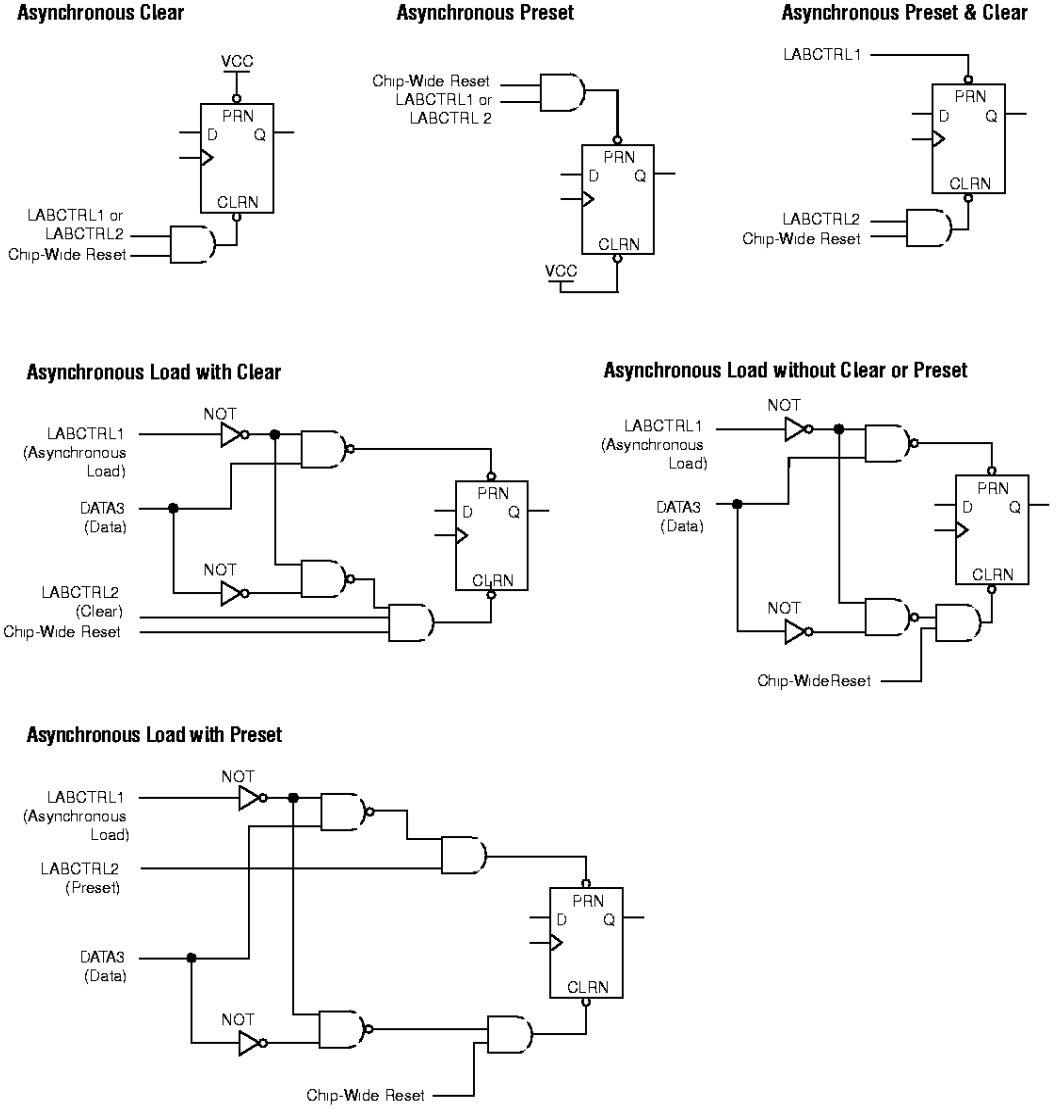


Table 9. EPF10K100β, EPF10K100E, EPF10K130E, EPF10K200E & EPF10K250E Peripheral βus Sources

Peripheral Control Signal	EPF10K100β EPF10K100E	EPF10K130E	EPF10K200E	EPF10K250E
OE0	Row A	Row C	Row G	Row E
OE1	Row C	Row E	Row I	Row G
OE2	Row E	Row G	Row K	Row I
OE3	Row L	Row N	Row R	Row P
OE4	Row I	Row K	Row O	Row M
OE5	Row K	Row M	Row Q	Row O
CLKENA0/CLK0/GLOBAL0	Row F	Row H	Row L	Row J
CLKENA1/OE6/GLOBAL1	Row D	Row F	Row J	Row H
CLKENA2/CLR0	Row B	Row D	Row H	Row F
CLKENA3/OE7/GLOBAL2	Row H	Row J	Row N	Row L
CLKENA4/CLR1	Row J	Row L	Row P	Row N
CLKENA5/CLK1/GLOBAL3	Row G	Row I	Row M	Row K

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals.

The chip-wide output enable pin is an active-low pin that can be used to tri-state all pins on the device. This option can be set in the MAX+PLUS II software. The registers in the IOE can also be reset by the chip-wide reset pin.

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 16).

Figure 16. FLEX 10KE Column-to-IOE Connections

The values for m and n are provided in Table 11.

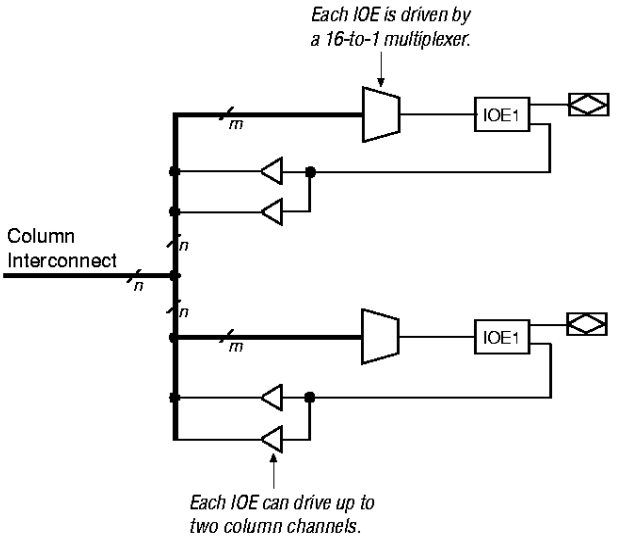


Table 11 lists the FLEX 10KE column-to-IOE interconnect resources.

Table 11. FLEX 10KE Column-to-IOE Interconnect Resources

Device	Channels per Column *(n)*	Column Channels per Pin *(m)*
EPF10K30E	24	16
EPF10K50E	24	16
EPF10K100B EPF10K100E	24	16
EPF10K130E	32	24
EPF10K200E	48	40
EPF10K250E	40	32

ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. ClockBoost allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

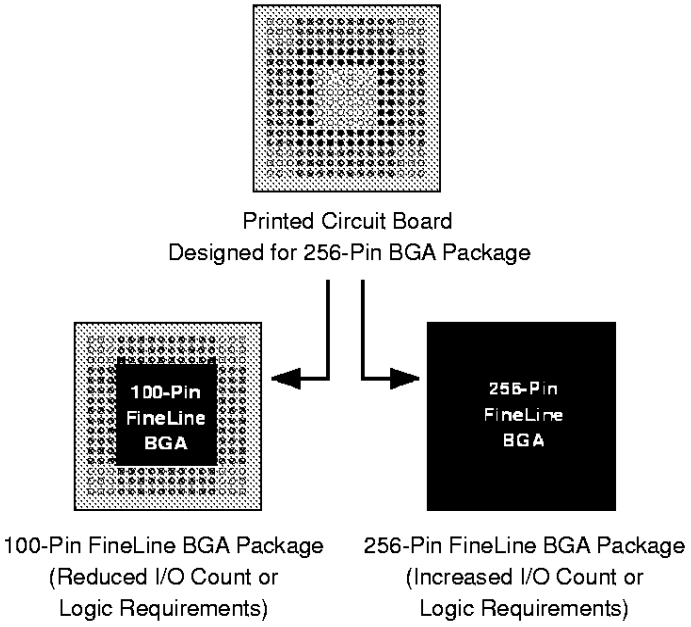
The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the MAX+PLUS II software. External devices are not required to use these features.

SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. SameFrame pin-out is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support anything from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K250E device in a 672-pin FineLine BGA package.

The MAX+PLUS II software versions 9.1 and higher provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use, and MAX+PLUS II software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 17).

Figure 17. SameFrame Pin-Out Example



Output Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for FLEX 10KE devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via MAX+PLUS II logic options. The MultiVolt I/O interface is controlled by connecting VCCIO to a different voltage. Its effect can be simulated in the MAX+PLUS II software via a **Global Project Device Options** command (Assign menu).

PCI Pull-up Clamping Diode Option

FLEX 10KE devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the V_{CCIO} value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled pin-by-pin. When V_{CCIO} is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When V_{CCIO} is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which would allow a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

Table 12 describes FLEX 10KE MultiVolt I/O support.

Table 12. FLEX 10KE MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled to drive an input with signals higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

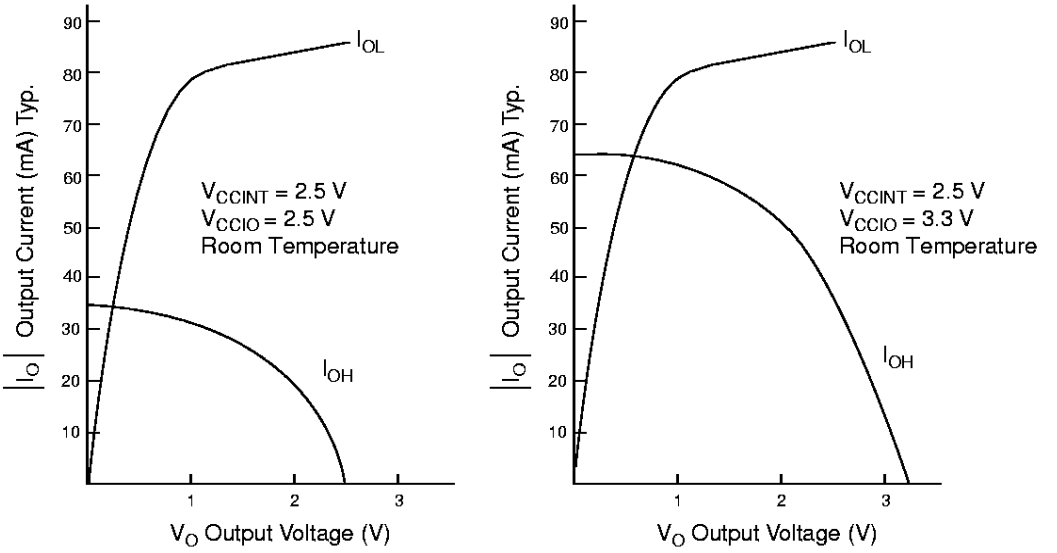
Output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. VCCIO should be connected to 3.3 V. When the I/O pin drives high, it will actively drive to VCCIO. The resistor will then pull the signal to 5.0 V. Because the FLEX 10KE device is 5.0-V tolerant, this operation will not affect the device. The PCI pull-up clamping diode must be disabled for any pin with a pull-up resistor to 5.0 V. The signal rise time is dependent on the value of the pull-up resistor and load impedance. When selecting a pull-up resistor, consider the I_{OL} current specification.

FLEX 10KE 2.5-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	2.30 (2.30)	2.70 (2.70)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*Notes (3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*Notes (3), (4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*Note (5)*	0	5.3	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Figure 21 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification, Revision 2.1*** (with 3.3-V V_{CCIO}).

Figure 21. Output Drive Characteristics of FLEX 10KE Devices



Timing Model

Table 15 shows the external timing parameters of FLEX 10KE devices. Detailed timing information for these devices will be released as it is available.

Table 15. FLEX 10KE External Timing Parameters

Symbol	Parameter	Device	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	EPF10K30E		8.5		10.0		13.5	ns
		EPF10K50E		8.5		10.0		13.5	ns
		EPF10K100B		11.0		12.0		14.5	ns
		EPF10K100E		10.0		12.0		16.0	ns
		EPF10K130E		10.0		12.0		16.0	ns
		EPF10K200E		10.0		12.0		16.0	ns
		EPF10K250E		11.0		13.5		17.0	ns

Power Consumption

The supply power (P) for FLEX 10KE devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in the ***1998 Data Book***.

☞ Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

Where:

$\mathbf{f_{MAX}}$	=	Maximum operating frequency in MHz
N	=	Total number of LEs used in the device
$\mathbf{tog_{LC}}$	=	Average percent of LEs toggling at each clock (typically 12.5%)
K	=	Constant

Table 16 provides the constant (K) values for EPF10K50E, EPF10K100B, and EPF10K200E devices. K factors for other FLEX 10KE devices will be released as they become available.

Table 16. FLEX 10KE K Constant Values

Device	K Value
EPF10K50E	14
EPF10K100B	19
EPF10K200E	19

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assume that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assume that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 22 shows the relationship between the current and operating frequency of EPF10K50E, EPF10K100B, and EPF10K200E devices. For other FLEX 10KE devices, contact Altera Applications at (800) 800-EPLD.

Figure 22. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency

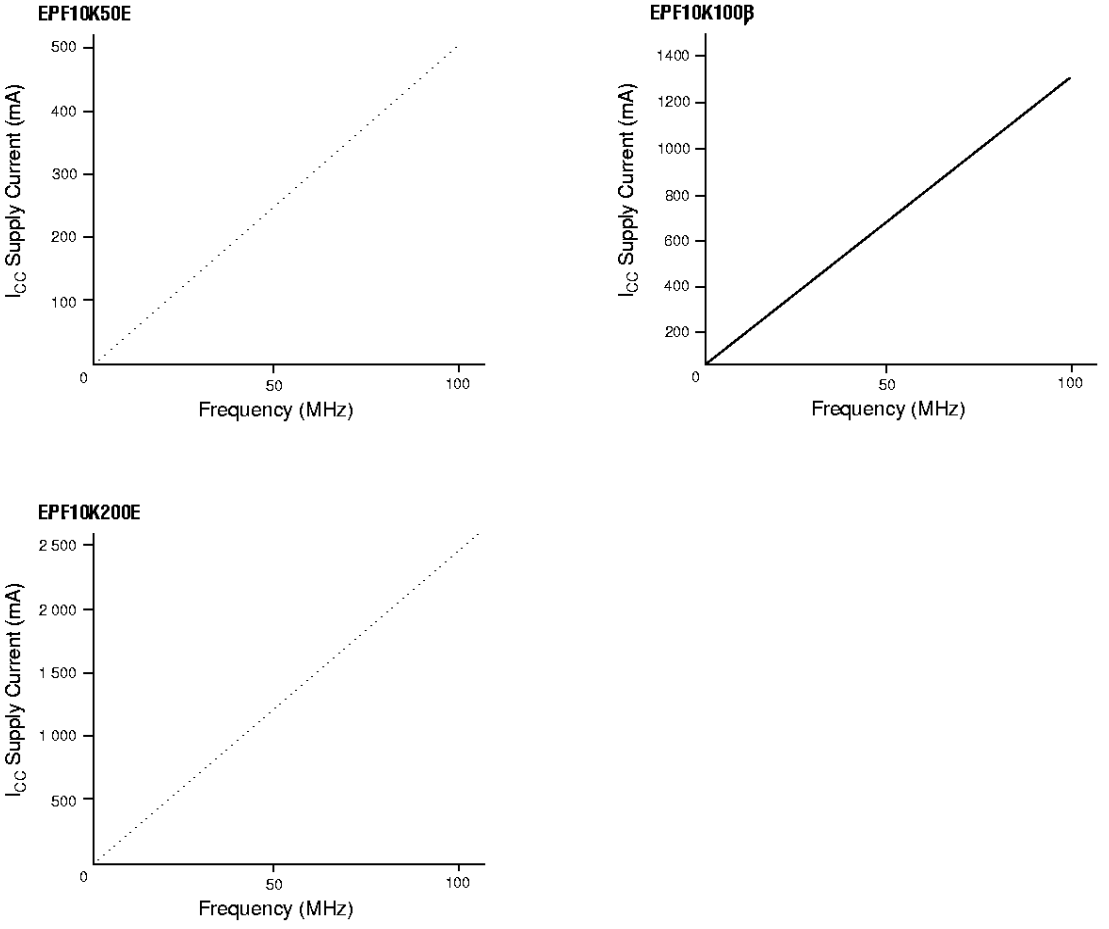


Table 19. FLEX 10KE Device Pin-Outs (Part 2 of 4) *Note (1)*

Pin Name	144-Pin TQFP EPF10K30E EPF10K50E	208-Pin PQFP EPF10K30E EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K130E	356-Pin βGA EPF10K100E	599-Pin PGA EPF10K200E EPF10K250E	600-Pin βGA EPF10K200E EPF10K250E
nCS *(4)*	144	208	240	240	AD24	AY38	AL29
CS *(4)*	143	207	239	239	AD23	BA39	AN29
RDYnBSY *(4)*	11	16	23	23	U22	AW47	AG35
CLKUSR *(4)*	7	10	11	11	AA24	AY42	AM34
DATA7 *(4)*	116	166	190	190	AF4	BD14	AM13
DATA6 *(4)*	114	164	188	188	AD8	BA17	AR12
DATA5 *(4)*	113	162	186	186	AE5	BB16	AN12
DATA4 *(4)*	112	161	185	185	AD6	BF12	AP11
DATA3 *(4)*	111	159	183	183	AF2	BG11	AM11
DATA2 *(4)*	110	158	182	182	AD5	BG9	AR10
DATA1 *(4)*	109	157	181	181	AD4	BF10	AN10
DATA0 *(2)*, *(5)*	108	156	180	180	AD3	BC5	AM4
TDI *(2)*	105	153	177	177	AC3	BF4	AN1
TDO *(2)*	4	4	4	4	AC23	BB42	AN34
TCK *(2)*	1	1	1	1	AD25	BE43	AL31
TMS *(2)*	34	50	58	58	D22	F42	C35
TRST *(2)*	*Note (6)*	51	59	59	D23	B46	C34
Dedicated Inputs	54, 56, 124, 126	78, 80, 182, 184	90, 92, 210, 212	90, 92, 210, 212	A13, B14, AF14, AE13	B24, C25, BG25, BG23	C18, D18, AM18, AN18
Dedicated Clock Pins	55, 125	79, 183	91, 211	91, 211	A14, AF13	BF24, A25	AL18, E18
DEV_CLRn *(3)*	122	180	209	209	AD13	–	–
DEV_OE *(3)*	128	186	213	213	AE14	–	–
VCCINT (2.5 V)	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 27, 47, 89, 96, 122, 130, 150, 170	5, 20, 27, 47, 76, 89, 96, 122, 130, 150, 159, 170	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	BE23	AR17

Table 19. FLEX 10KE Device Pin-Outs (Part 4 of 4) *Note (1)*

Pin Name	144-Pin TQFP EPF10K30E EPF10K50E	208-Pin PQFP EPF10K30E EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K130E	356-Pin βGA EPF10K100E	599-Pin PGA EPF10K200E EPF10K250E	600-Pin βGA EPF10K200E EPF10K250E
GNDIO	15, 40, 50, 66, 85, 104, 129, 139	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–	–	–	D24, E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AD4, AD44, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39, BD24	C8, E12, C15, A20, C23, A27, AM26, AR23, AM19, AN15, AL12, AN8, C2, C3, C4, D5, E5, C33, C32, D31, E31, AL5, AM5, AN4, AN3, AM31, AN32, AN33, AP34
Total User I/O Pins *(7)*	102	147	189	186	274	470	470

Notes:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(7) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 2 of 5) *Note (1)*				
Pin Name	**484-Pin FineLine βGA EPF10K30E**	**484-Pin FineLine βGA EPF10K50E**	**484-Pin FineLine βGA EPF10K100E**	**484-Pin FineLine βGA EPF10K130E**
DATA5 *(4)*	D7	D7	D7	D7
DATA4 *(4)*	E7	E7	E7	E7
DATA3 *(4)*	F6	F6	F6	F6
DATA2 *(4)*	D5	D5	D5	D5
DATA1 *(4)*	E6	E6	E6	E6
DATA0 *(2)*, *(5)*	D4	D4	D4	D4
TDI *(2)*	F5	F5	F5	F5
TDO *(2)*	F19	F19	F19	F19
TCK *(2)*	E18	E18	E18	E18
TMS *(2)*	U18	U18	U18	U18
TRST *(2)*	V19	V19	V19	V19
Dedicated Inputs	E12, H11, R12, V11	E12, H11, R12, V11	E12, H11, R12, V11	E12, H11, R12, V11
Dedicated Clock Pins	D12, P11	D12, P11	D12, P11	D12, P11
DEV_CLRn *(3)*	G11	G11	G11	G11
DEV_OE *(3)*	F12	F12	F12	F12
VCCINT (2.5 V)	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12
VCCIO (2.5 or 3.3 V)	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13

Table 23 shows the FLEX 10KE device/package combinations that support SameFrame pin-outs. All FineLine BGA packages support SameFrame pin-outs providing the flexibility to migrate not only from device to device within the same package, but also from one package to another. The I/O count will vary, and MAX+PLUS II software versions 9.1 and higher provide features to help use only the common pins.

Table 23. FLEX 10KE SameFrame Pin-Out Support

Device	256-Pin FineLine BGA	484-Pin FineLine BGA	672-Pin FineLine BGA
EPF10K30E	✓	✓	
EPF10K50E	✓	✓	
EPF10K100B	✓		
EPF10K100E	✓	✓	
EPF10K130E		✓	✓
EPF10K200E			✓
EPF10K250E			✓

Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Family Data Sheet* version 1.01 supersedes information published in previous versions.

The *FLEX 10KE Embedded Programmable Logic Family Data Sheet* version 1.01 contains the following change:

- Updated Table 15 (FLEX 10KE external timing parameters).