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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	-
Number of Gates	-
Voltage - Supply	-
Mounting Type	Through Hole
Operating Temperature	-
Package / Case	599-BCPGA
Supplier Device Package	599-PGA (62.5x62.5)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k250egc599-1

- Software design support and automatic place-and-route provided by the Altera MAX+PLUS® II development system for 486- and Pentium-based PCs, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-compatibility (with other FLEX 10KE devices) across device densities and pin counts
- Additional design entry and simulation support provided by electronic design interchange format (EDIF) 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular electronic design automation (EDA) tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2), (3)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			
EPF10K50E	102	147	189	191		254			
EPF10K100B		147	189	191					
EPF10K100E		147	189	191	274	338			
EPF10K130E			186			369			413
EPF10K200E							470	470	470
EPF10K250E							470	470	470

Notes:

(1) Contact Altera Customer Marketing for up-to-date information on package availability.

(2) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), pin-grid array (PGA), and ball-grid array (BGA).

(3) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices. MAX+PLUS II software versions 9.1 and higher provide features to help use only the common pins.

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm^2)	484	936	1,197	289	1,225	529	3,904	2,025	729

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC1441 Configuration EPROMs, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or from the Altera BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, or ByteBlasterMV™ parallel port download cable. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 330 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an optimized interface that permits microprocessors to configure FLEX 10KE devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

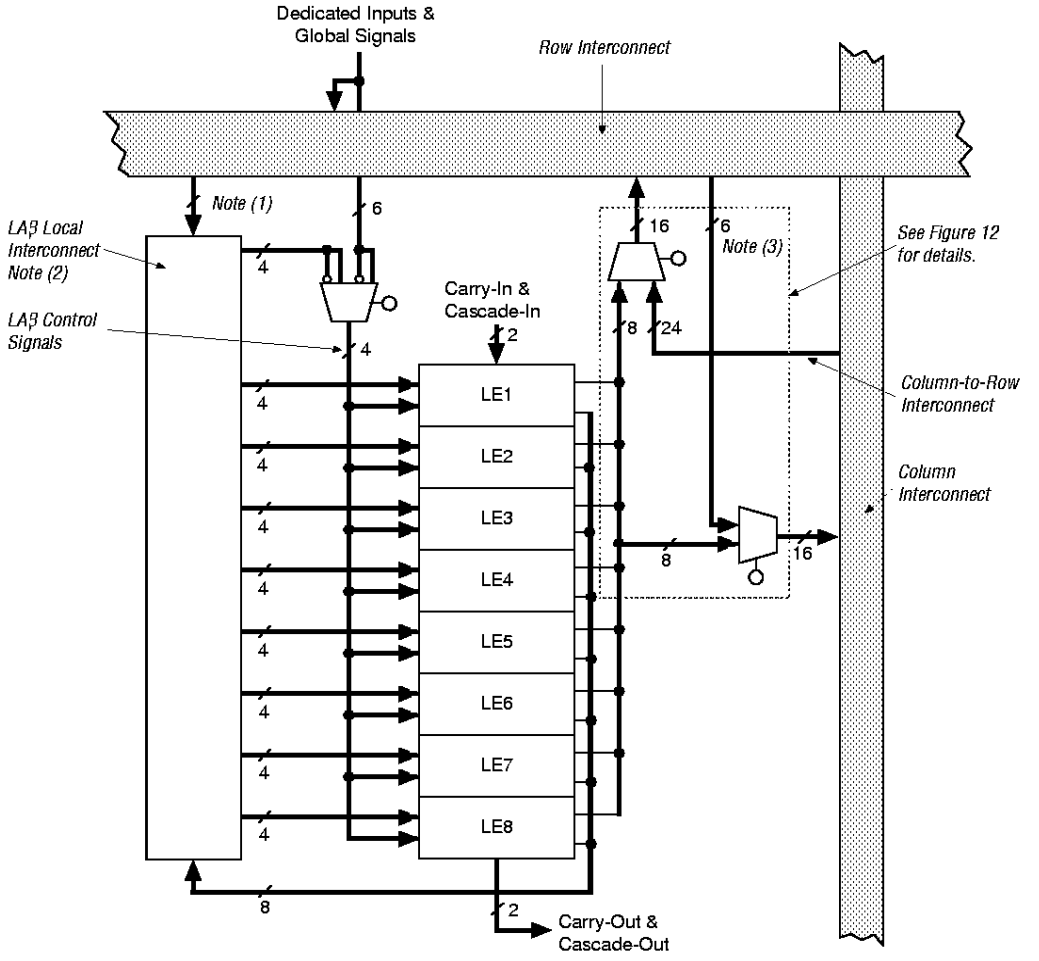
For more information, go to the following documents:

- *Configuration EPROMs for FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*

FLEX 10KE devices are supported by the Altera MAX+PLUS II development system, a single, integrated package that offers schematic, text—including AHDL—and waveform design entry; compilation and logic synthesis; full simulation and worst-case timing analysis; and device configuration. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The MAX+PLUS II software works easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

Figure 6. FLEX 10KE LAβ



Notes:

(1) EPF10K30E and EPF10K50E devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 26.

(2) EPF10K30E and EPF10K50E devices have 30 LAB local interconnect channels; EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 34.

(3) In EPF10K100B devices, four row channels can drive column channels at each intersection.

The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect routing structure. The two outputs can be controlled independently; for example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

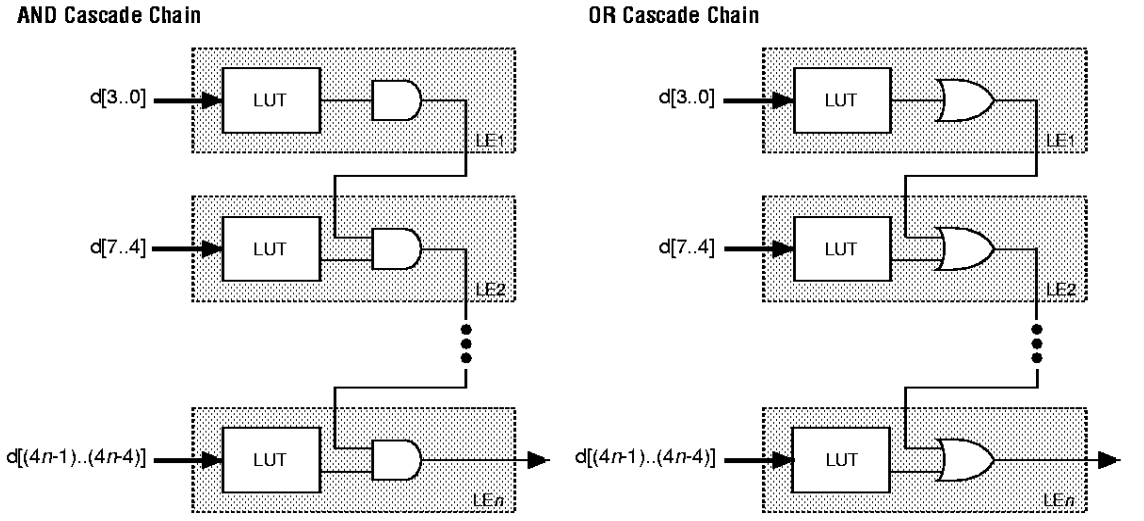
The FLEX 10KE architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in a LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10KE architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50E device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 9. FLEX 10KE Cascade Chain Operation



LE Operating Modes

The FLEX 10KE LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

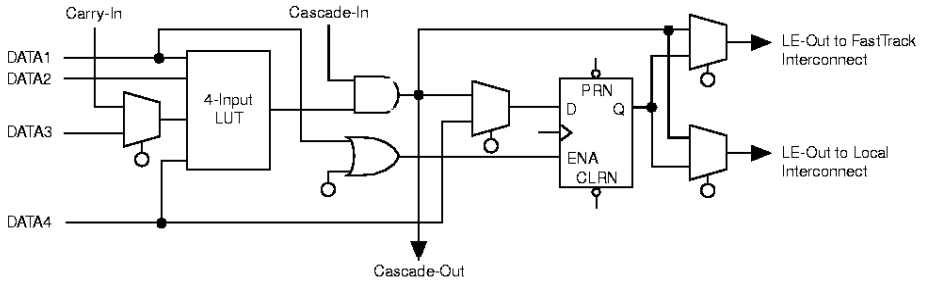
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions to use an LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The MAX+PLUS II software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

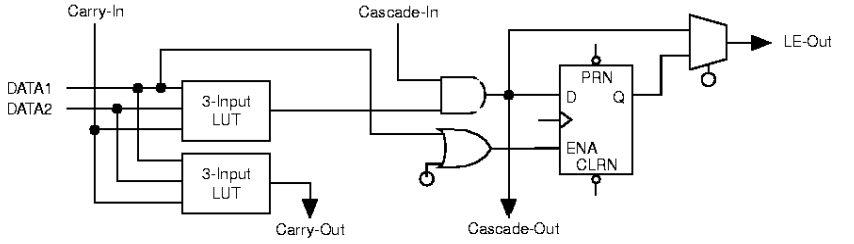
Figure 10 shows the LE operating modes.

Figure 10. FLEX 10KE LE Operating Modes

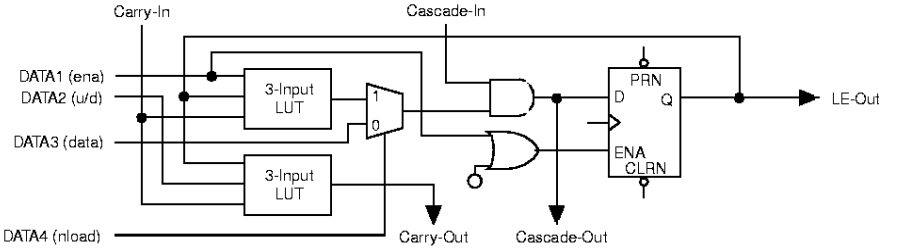
Normal Mode



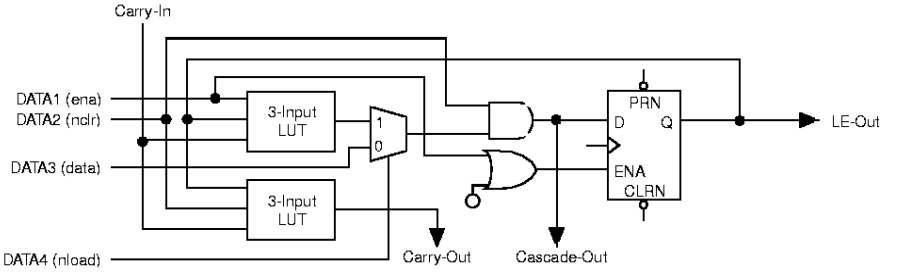
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect routing structure resources available in each FLEX 10KE device.

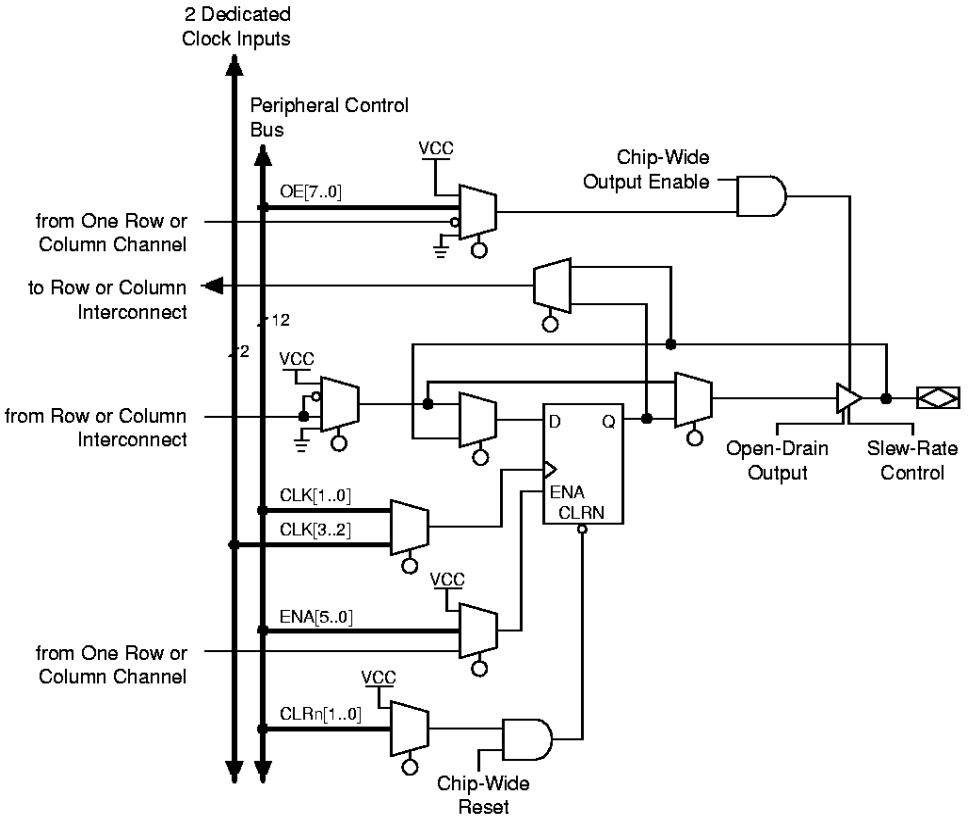
Table 7. FLEX 10KE FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K30E	6	216	36	24
EPF10K50E	10	216	36	24
EPF10K100B EPF10K100E	12	312	52	24
EPF10K130E	16	312	52	32
EPF10K200E	24	312	52	48
EPF10K250E	20	456	76	40

In addition to general-purpose I/O pins, FLEX 10KE devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 13 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Figure 14. FLEX 10KE I/O Element



Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. To use the true and complement of a clock to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, then two signals on the peripheral control bus are consumed, one for each sense of the clock.

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 15).

Figure 15. FLEX 10KE Row-to-IOE Connections

The values for m and n are provided in Table 10.

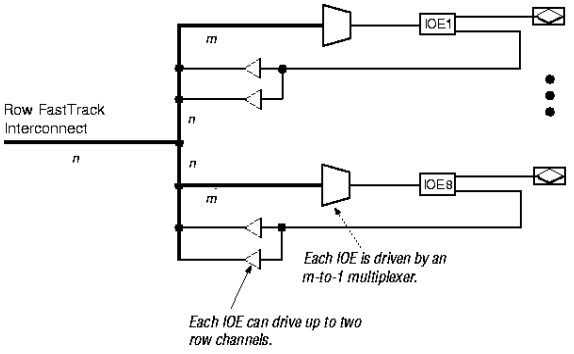


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

Table 10. FLEX 10KE Row-to-IOE Interconnect Resources

Device	Channels per Row *(n)*	Row Channels per Pin *(m)*
EPF10K30E	216	27
EPF10K50E	216	27
EPF10K100B EPF10K100E	312	39
EPF10K130E	312	39
EPF10K200E	312	39
EPF10K250E	456	57

ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. ClockBoost allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the MAX+PLUS II software. External devices are not required to use these features.

SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. SameFrame pin-out is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support anything from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K250E device in a 672-pin FineLine BGA package.

The MAX+PLUS II software versions 9.1 and higher provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use, and MAX+PLUS II software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 17).

Table 12 describes FLEX 10KE MultiVolt I/O support.

Table 12. FLEX 10KE MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled to drive an input with signals higher than V_{CCIO}.

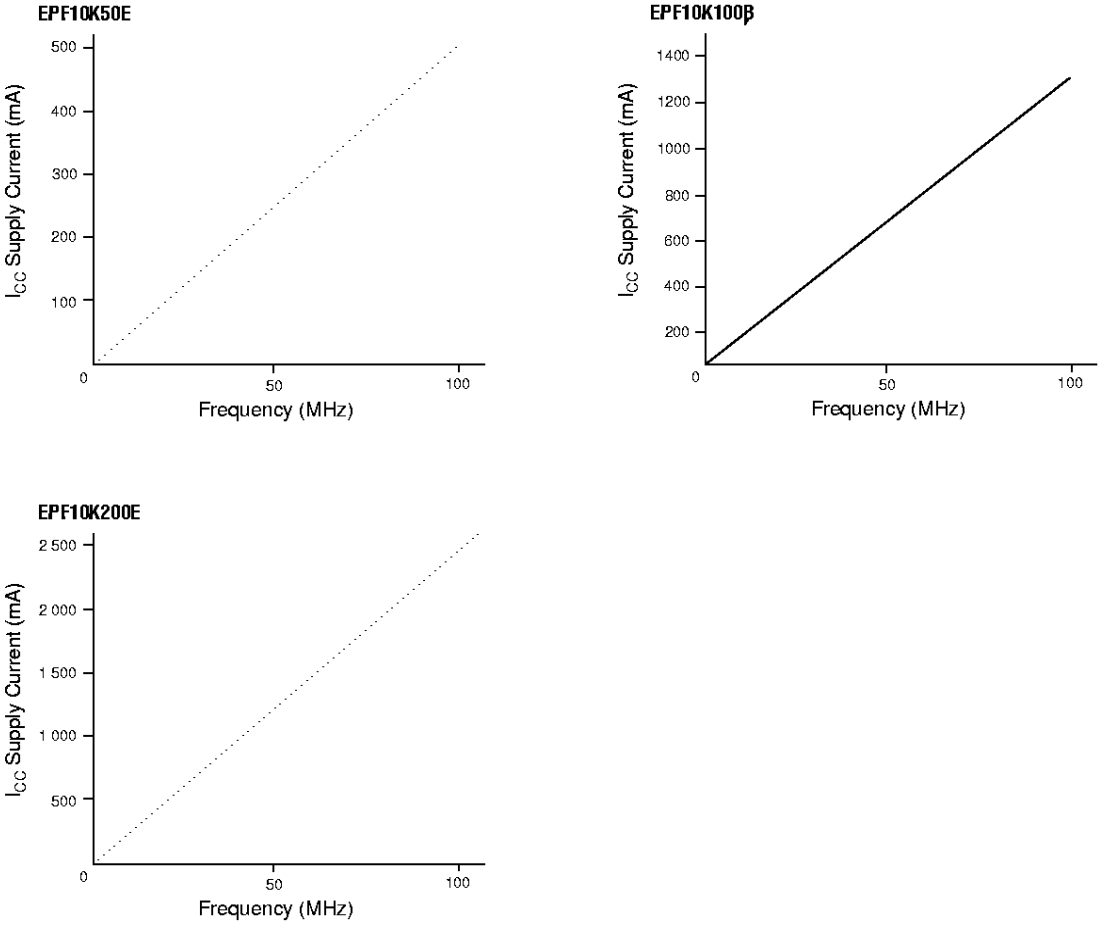
(2) When V_{CCIO} = 3.3 V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. VCCIO should be connected to 3.3 V. When the I/O pin drives high, it will actively drive to VCCIO. The resistor will then pull the signal to 5.0 V. Because the FLEX 10KE device is 5.0-V tolerant, this operation will not affect the device. The PCI pull-up clamping diode must be disabled for any pin with a pull-up resistor to 5.0 V. The signal rise time is dependent on the value of the pull-up resistor and load impedance. When selecting a pull-up resistor, consider the I_{OL} current specification.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assume that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assume that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 22 shows the relationship between the current and operating frequency of EPF10K50E, EPF10K100B, and EPF10K200E devices. For other FLEX 10KE devices, contact Altera Applications at (800) 800-EPLD.

Figure 22. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency



FLEX 10KE devices are generally pin-compatible with the equivalent FLEX 10KA device. In some cases, FLEX 10KE devices have fewer I/O pins than FLEX 10KA devices. Table 17 shows which FLEX 10KE devices have fewer I/Os. However, power, ground, JTAG, and configuration pins are the same on FLEX 10KA and FLEX 10KE devices, enabling migration from a FLEX 10KA design to a FLEX 10KE design.

Table 17. I/O Count on FLEX 10KA & FLEX 10KE Devices

FLEX 10KA		FLEX 10KE	
Device	**I/O Count**	**Device**	**I/O Count**
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	244	EPF10K30EF484	218
EPF10K30AB356	246	EPF10K30EB356	220
EPF10K50VF484	300	EPF10K50EF484	254
EPF10K50VB356	274	EPF10K50EB356	256
EPF10K100AF484	366	EPF10K100EF484	337
EPF10K130VB600	470	EPF10K130EB600	426

Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see Table 18), chosen on the basis of the target application. An EPC2, EPC1, or EPC1441 Configuration EPROM, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Table 19. FLEX 10KE Device Pin-Outs (Part 2 of 4) *Note (1)*

Pin Name	144-Pin TQFP EPF10K30E EPF10K50E	208-Pin PQFP EPF10K30E EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K130E	356-Pin βGA EPF10K100E	599-Pin PGA EPF10K200E EPF10K250E	600-Pin βGA EPF10K200E EPF10K250E
nCS *(4)*	144	208	240	240	AD24	AY38	AL29
CS *(4)*	143	207	239	239	AD23	BA39	AN29
RDYnBSY *(4)*	11	16	23	23	U22	AW47	AG35
CLKUSR *(4)*	7	10	11	11	AA24	AY42	AM34
DATA7 *(4)*	116	166	190	190	AF4	BD14	AM13
DATA6 *(4)*	114	164	188	188	AD8	BA17	AR12
DATA5 *(4)*	113	162	186	186	AE5	BB16	AN12
DATA4 *(4)*	112	161	185	185	AD6	BF12	AP11
DATA3 *(4)*	111	159	183	183	AF2	BG11	AM11
DATA2 *(4)*	110	158	182	182	AD5	BG9	AR10
DATA1 *(4)*	109	157	181	181	AD4	BF10	AN10
DATA0 *(2)*, *(5)*	108	156	180	180	AD3	BC5	AM4
TDI *(2)*	105	153	177	177	AC3	BF4	AN1
TDO *(2)*	4	4	4	4	AC23	BB42	AN34
TCK *(2)*	1	1	1	1	AD25	BE43	AL31
TMS *(2)*	34	50	58	58	D22	F42	C35
TRST *(2)*	*Note (6)*	51	59	59	D23	B46	C34
Dedicated Inputs	54, 56, 124, 126	78, 80, 182, 184	90, 92, 210, 212	90, 92, 210, 212	A13, B14, AF14, AE13	B24, C25, BG25, BG23	C18, D18, AM18, AN18
Dedicated Clock Pins	55, 125	79, 183	91, 211	91, 211	A14, AF13	BF24, A25	AL18, E18
DEV_CLRn *(3)*	122	180	209	209	AD13	–	–
DEV_OE *(3)*	128	186	213	213	AE14	–	–
VCCINT (2.5 V)	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 27, 47, 89, 96, 122, 130, 150, 170	5, 20, 27, 47, 76, 89, 96, 122, 130, 150, 159, 170	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	BE23	AR17

Table 20. FLEX 10KE FineLine βGA Device Pin-Outs (Part 4 of 4) *Note (1)*

Pin Name	256-Pin FineLine βGA EPF10K30E	256-Pin FineLine βGA EPF10K50E EPF10K100E EPF10K100β	672-Pin FineLine βGA EPF10K130E	672-Pin FineLine βGA EPF10K200E EPF10K250E
Total User I/O Pins *(7)*	176	191	413	470

Notes:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(7) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 21 shows the dedicated pin-outs for FLEX 10KE devices in 484-pin FineLine BGA packages.

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 1 of 5) *Note (1)*

Pin Name	484-Pin FineLine βGA EPF10K30E	484-Pin FineLine βGA EPF10K50E	484-Pin FineLine βGA EPF10K100E	484-Pin FineLine βGA EPF10K130E
MSEL0 *(2)*	U4	U4	U4	U4
MSEL1 *(2)*	V4	V4	V4	V4
nSTATUS *(2)*	W19	W19	W19	W19
nCONFIG *(2)*	T7	T7	T7	T7
DCLK *(2)*	E5	E5	E5	E5
CONF_DONE *(2)*	F18	F18	F18	F18
INIT_DONE *(3)*	K19	K19	K19	K19
nCE *(2)*	E4	E4	E4	E4
nCEO *(6)*	E19	E19	E19	E19
nWS *(4)*	E17	E17	E17	E17
nRS *(4)*	F17	F17	F17	F17
nCS *(4)*	D19	D19	D19	D19
CS *(4)*	D18	D18	D18	D18
RDYnBSY *(4)*	K17	K17	K17	K17
CLKUSR *(4)*	G18	G18	G18	G18
DATA7 *(4)*	E8	E8	E8	E8
DATA6 *(4)*	G7	G7	G7	G7

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 2 of 5) *Note (1)*				
Pin Name	**484-Pin FineLine βGA EPF10K30E**	**484-Pin FineLine βGA EPF10K50E**	**484-Pin FineLine βGA EPF10K100E**	**484-Pin FineLine βGA EPF10K130E**
DATA5 *(4)*	D7	D7	D7	D7
DATA4 *(4)*	E7	E7	E7	E7
DATA3 *(4)*	F6	F6	F6	F6
DATA2 *(4)*	D5	D5	D5	D5
DATA1 *(4)*	E6	E6	E6	E6
DATA0 *(2), (5)*	D4	D4	D4	D4
TDI *(2)*	F5	F5	F5	F5
TDO *(2)*	F19	F19	F19	F19
TCK *(2)*	E18	E18	E18	E18
TMS *(2)*	U18	U18	U18	U18
TRST *(2)*	V19	V19	V19	V19
Dedicated Inputs	E12, H11, R12, V11	E12, H11, R12, V11	E12, H11, R12, V11	E12, H11, R12, V11
Dedicated Clock Pins	D12, P11	D12, P11	D12, P11	D12, P11
DEV_CLRn *(3)*	G11	G11	G11	G11
DEV_OE *(3)*	F12	F12	F12	F12
VCCINT (2.5 V)	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12
VCCIO (2.5 or 3.3 V)	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 4 of 5) *Note (1)*

Pin Name	484-Pin FineLine βGA EPF10K30E	484-Pin FineLine βGA EPF10K50E	484-Pin FineLine βGA EPF10K100E	484-Pin FineLine βGA EPF10K130E
No Connect (N.C.)	A2, A3, A4, A5, A7, A9, A11, A12, A14, A15, A20, A21, B3, B4, B9, B10, B12, B16, B19, B20, C1, C6, C9, C10, C12, C13, C14, C16, C17, C22, D1, D2, D3, D20, D21, D22, E2, E3, E20, E22, F1, F2, F3, F20, F21, F22, G2, G4, G20, G22, H1, H3, H6, H19, H21, H22, J1, J2, J3, J21, J22, K1, K2, K6, K21, K22, L1, L2, L3, L4, L19, L20, L21, L22, M1, M2, M3, M4, M21, M22, N1, N2, N21, N22, N6, N17, N19, P1, P2, P3, P5, P7, P20, P21, P22, R2, R3, R17, R19, R20, R21, T2, T18, T20, T21, U1, U2, U3, U20, U21, U22, V1, V2, V20, V21, W1, W2, W22, Y4, Y9, Y12, Y13, Y16, Y19, Y20, AA2, AA3, AA4, AA9, AA11, AA13, AA15, AA21, AB1, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB12, AB15, AB17, AB18, AB19, AB20, AB21, AB22	A2, A3, A4, A5, A7, A9, A11, A12, A14, A15, A20, A21, B3, B4, B9, B10, B12, B16, B19, B20, C1, C6, C9, C10, C12, C13, C14, C16, C17, C22, D1, D2, D3, D20, D21, E2, E3, E20, E22, F1, F2, F20, F21, G2, G20, G22, J1, J2, J3, J21, K2, K22, L1, L2, L20, L22, M2, M3, M22, N1, N2, N21, N22, P3, P20, P21, P22, R2, R3, R21, T2, T20, T21, U1, U2, U3, U20, U21, U22, V2, V20, W1, W2, W22, Y4, Y9, Y12, Y13, Y16, Y19, Y20, AA2, AA3, AA4, AA9, AA11, AA13, AA15, AA21, AB1, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB12, AB15, AB17, AB18, AB19, AB20, AB21, AB22	A2, A3, A4, A5, B3, B4, B10, C17, F2, J2, K2, L2, N1, P20, P22, R3, T20, T21, U1, W22, Y16, AA15, AB3, AB4, AB5, AB7, AB15, AB17, AB18, AB19, AB20	–
GNDINT	–	–	–	–

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 5 of 5) *Note (1)*

Pin Name	484-Pin FineLine βGA EPF10K30E	484-Pin FineLine βGA EPF10K50E	484-Pin FineLine βGA EPF10K100E	484-Pin FineLine βGA EPF10K130E
GNDIO	–	–	–	–
Total User I/O Pins *(7)*	220	254	338	369

Notes to Tables:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(7) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 22 shows pin compatibility between FLEX 10KE devices.

Table 22. FLEX 10KE Device Pin Compatibility

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine βGA	484-Pin FineLine βGA	599-Pin PGA	600-Pin βGA	672-Pin FineLine βGA
EPF10K30E	*Note (1)*	*Note (1)*		*Note (2)*	*Note (2)*			
EPF10K50E	*Note (1)*	*Note (1)*	*Note (2)*	*Note (2)*	*Note (2)*			
EPF10K100B		*Note (1)*	*Note (2)*	*Note (2)*				
EPF10K100E		*Note (1)*	*Note (2)*	*Note (2)*	*Note (2)*			
EPF10K130E			*Note (2)*		*Note (2)*			*Note (2)*
EPF10K200E						*Note (1)*	*Note (1)*	*Note (2)*
EPF10K250E						*Note (1)*	*Note (1)*	*Note (2)*

Notes:
(1) Devices in the same package are pin-compatible and have the same number of I/O pins.
(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices. MAX+PLUS II software versions 9.1 and higher provide features to help use only the common pins.

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