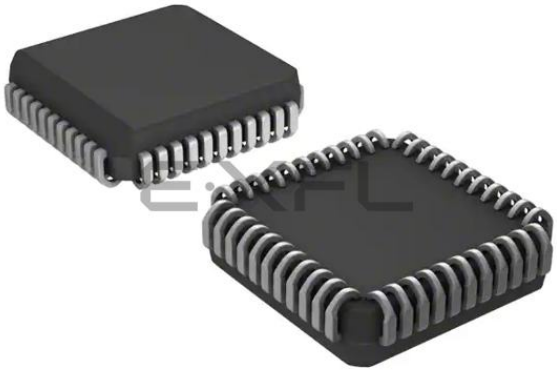

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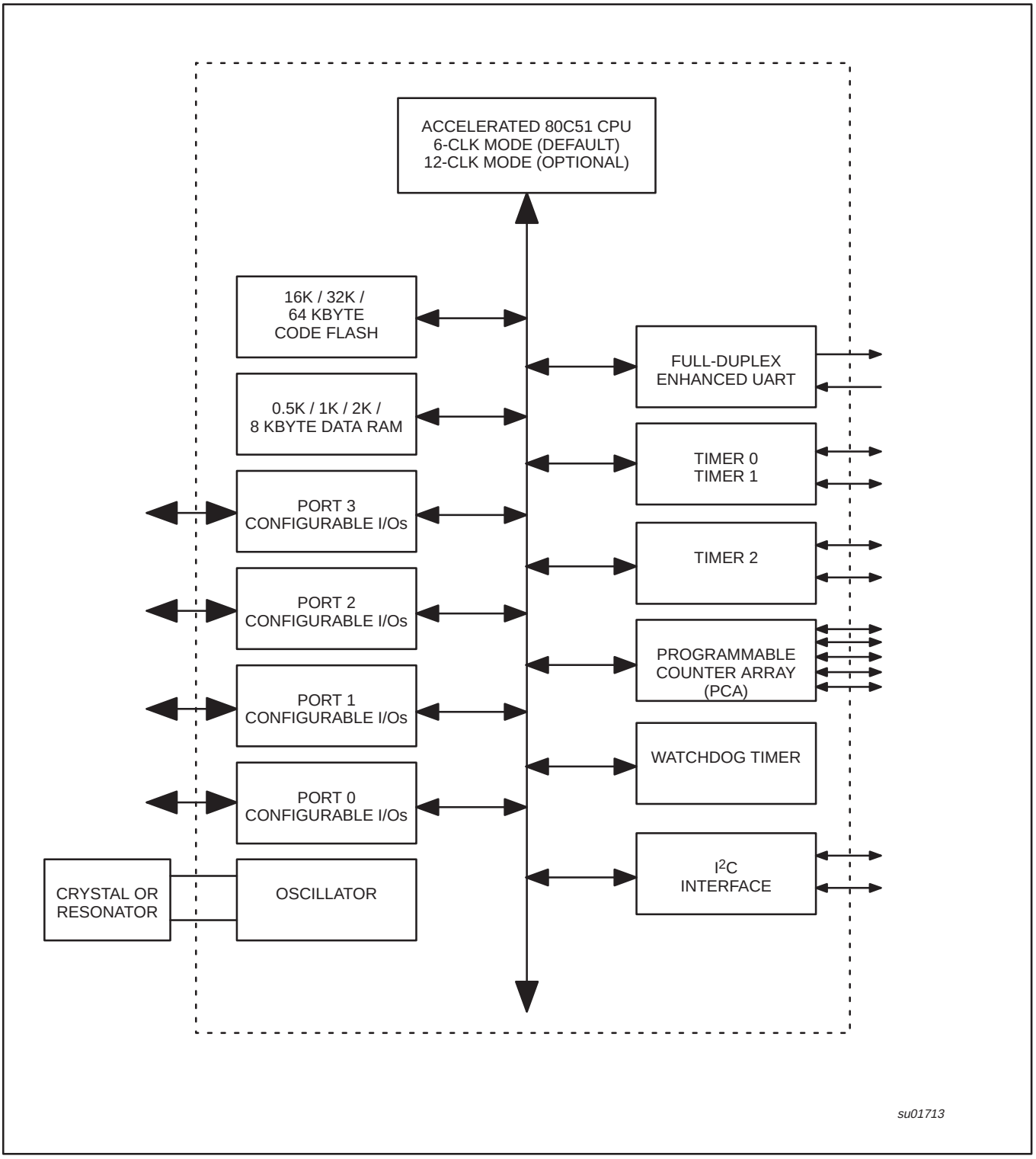
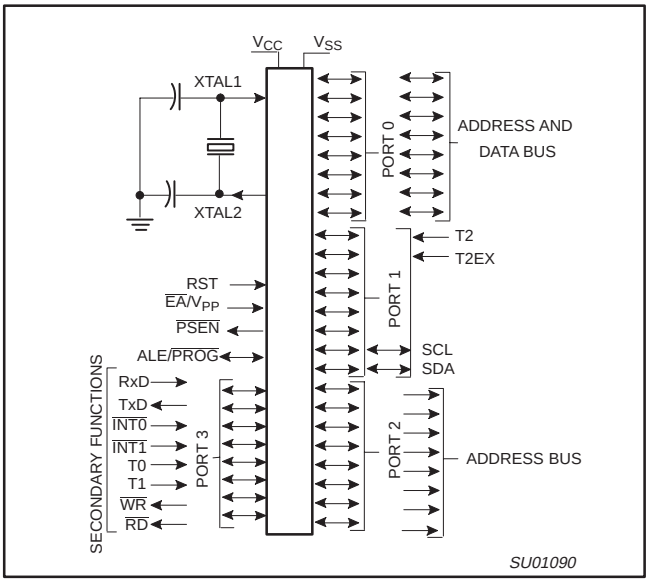
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89c660hfa-00-512

BLOCK DIAGRAM 1

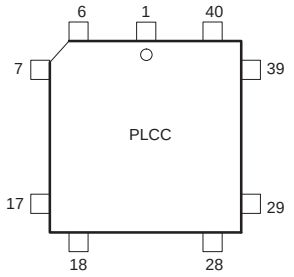


LOGIC SYMBOL



PINNING

Plastic Leaded Chip Carrier

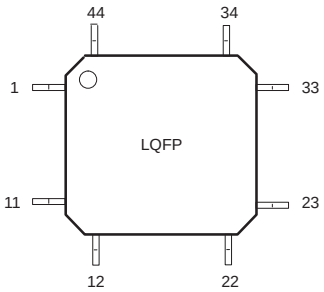


Pin	Function	Pin	Function	Pin	Function
1	NIC*	16	P3.4/T0/CEX3	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1/CEX4	32	$\overline{PSEN}$
3	P1.1/T2EX	18	P3.6/$\overline{WR}$	33	ALE
4	P1.2/ECI	19	P3.7/$\overline{RD}$	34	NIC*
5	P1.3/CEX0	20	XTAL2	35	$\overline{EA}$/V_{PP}
6	P1.4/CEX1	21	XTAL1	36	P0.7/AD7
7	P1.5/CEX2	22	V_{SS}	37	P0.6/AD6
8	P1.6/SCL	23	NIC*	38	P0.5/AD5
9	P1.7/SDA	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/$\overline{INT0}$	29	P2.5/A13	44	V_{CC}
15	P3.3/$\overline{INT1}$	30	P2.6/A14		

* NO INTERNAL CONNECTION

SU01091

Low Quad Flat Pack



Pin	Function	Pin	Function	Pin	Function
1	P1.5/CEX2	16	V_{SS}	31	P0.6/AD6
2	P1.6/SCL	17	NIC*	32	P0.5/AD5
3	P1.7/SDA	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NIC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/$\overline{INT0}$	23	P2.5/A13	38	V_{CC}
9	P3.3/$\overline{INT1}$	24	P2.6/A14	39	NIC*
10	P3.4/T0/CEX3	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1/CEX4	26	$\overline{PSEN}$	41	P1.1/T2EX
12	P3.6/$\overline{WR}$	27	ALE	42	P1.2/ECI
13	P3.7/$\overline{RD}$	28	NIC*	43	P1.3/CEX0
14	XTAL2	29	$\overline{EA}$/V_{PP}	44	P1.4/CEX1
15	XTAL1	30	P0.7/AD7		

* NO INTERNAL CONNECTION

SU01401

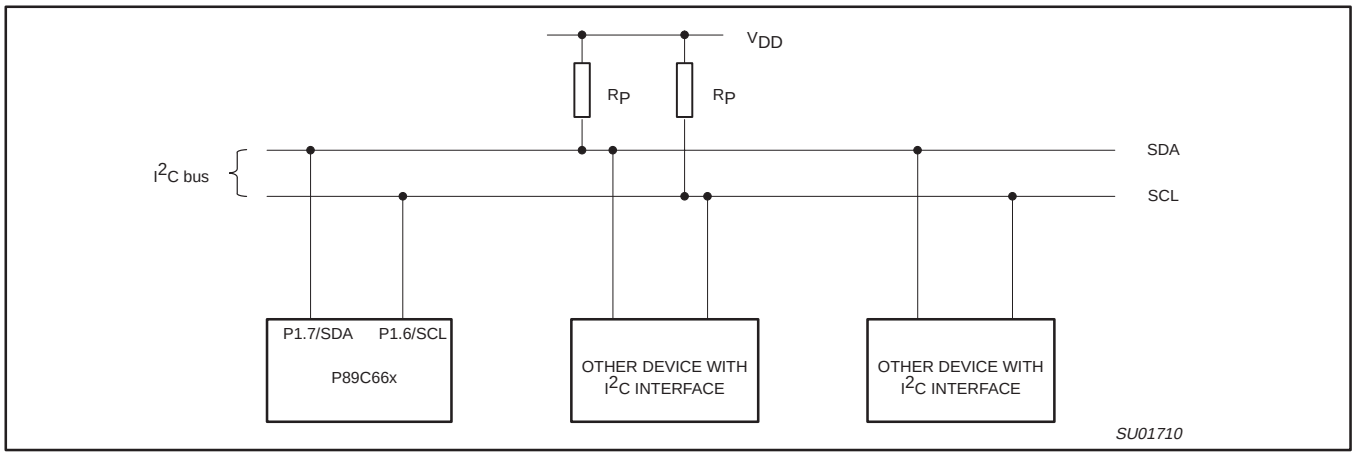


Figure 1. Typical I²C Bus Configuration

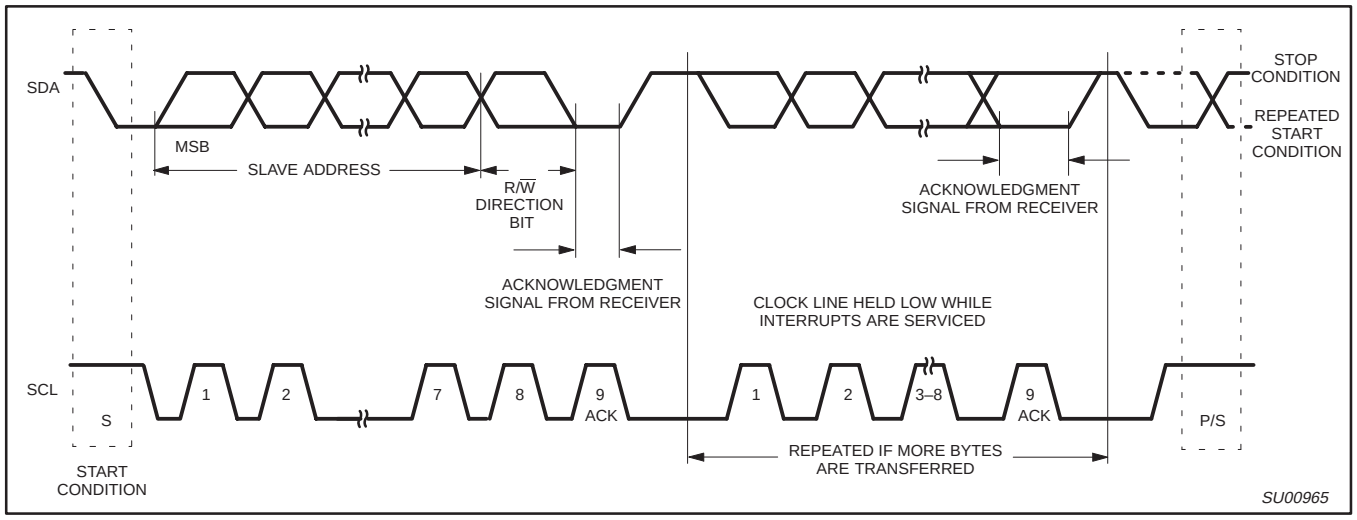


Figure 2. Data Transfer on the I²C Bus

SIO1 Implementation and Operation

Figure 3 shows how the on-chip I²C bus interface is implemented, and the following text describes the individual blocks.

Input Filters and Output Stages

The input filters have I²C compatible input levels. If the input voltage is less than 1.5 V, the input logic level is interpreted as 0; if the input voltage is greater than 3.0 V, the input logic level is interpreted as 1. Input signals are synchronized with the internal clock ($f_{OSC}/4$), and spikes shorter than three oscillator periods are filtered out.

The output stages consist of open drain transistors that can sink 3mA at V_{OUT} < 0.4 V. These open drain outputs do not have clamping diodes to V_{DD}. Thus, if the device is connected to the I²C bus and V_{DD} is switched off, the I²C bus is not affected.

Address Register, S1ADR

This 8-bit special function register may be loaded with the 7-bit slave address (7 most significant bits) to which SIO1 will respond when programmed as a slave transmitter or receiver. The LSB (GC) is used to enable general call address (00H) recognition.

Comparator

The comparator compares the received 7-bit slave address with its own slave address (7 most significant bits in S1ADR). It also compares the first received 8-bit byte with the general call address (00H). If an equality is found, the appropriate status bits are set and an interrupt is requested.

Shift Register, S1DAT

This 8-bit special function register contains a byte of serial data to be transmitted or a byte which has just been received. Data in S1DAT is always shifted from right to left; the first bit to be transmitted is the MSB (bit 7) and, after a byte has been received, the first bit of received data is located at the MSB of S1DAT. While data is being shifted out, data on the bus is simultaneously being shifted in; S1DAT always contains the last byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in S1DAT.

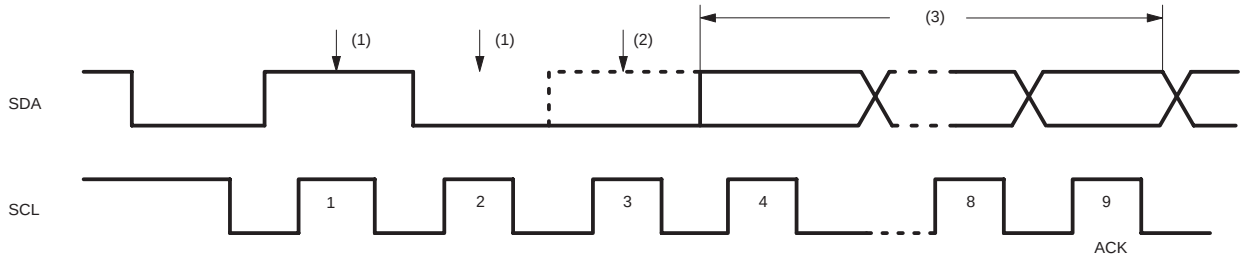
Arbitration and Synchronization Logic

In the Master Transmitter mode, the arbitration logic checks that every transmitted logic 1 actually appears as a logic 1 on the I^2C bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, arbitration is lost, and SIO1 immediately changes from master transmitter to slave receiver. SIO1 will continue to output clock pulses (on SCL) until transmission of the current serial byte is complete.

Arbitration may also be lost in the Master Receiver mode. Loss of arbitration in this mode can only occur while SIO1 is returning a “not acknowledge: (logic 1) to the bus. Arbitration is lost when another device on the bus pulls this signal LOW. Since this can occur only at the end of a serial byte, SIO1 generates no further clock pulses. Figure 4 shows the arbitration procedure.

The synchronization logic will synchronize the serial clock generator with the clock pulses on the SCL line from another device. If two or more master devices generate clock pulses, the “mark” duration is determined by the device that generates the shortest “marks,” and the “space” duration is determined by the device that generates the longest “spaces.” Figure 5 shows the synchronization procedure.

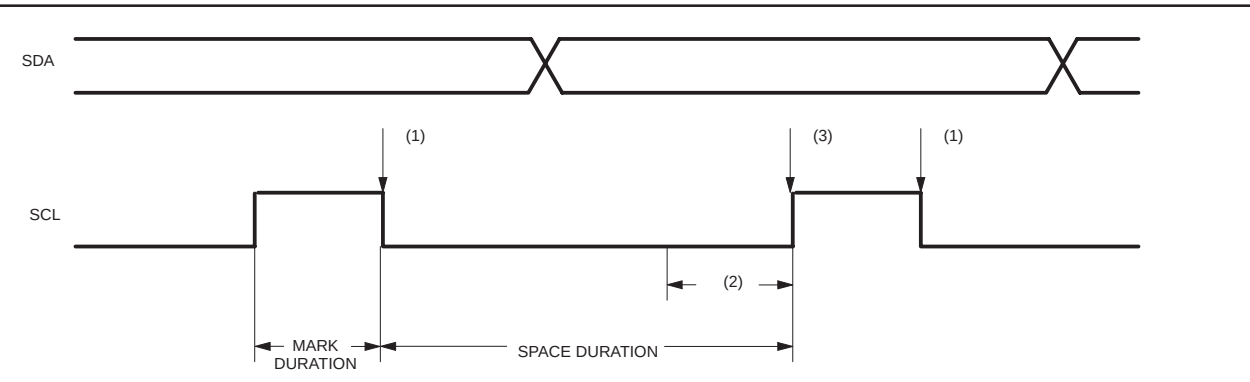
A slave may stretch the space duration to slow down the bus master. The space duration may also be stretched for handshaking purposes. This can be done after each bit or after a complete byte transfer. SIO1 will stretch the SCL space duration after a byte has been transmitted or received and the acknowledge bit has been transferred. The serial interrupt flag (SI) is set, and the stretching continues until the serial interrupt flag is cleared.



1. Another device transmits identical serial data.
2. Another device overrules a logic 1 (dotted line) transmitted by SIO1 (master) by pulling the SDA line low. Arbitration is lost, and SIO1 enters the slave receiver mode.
3. SIO1 is in the slave receiver mode but still generates clock pulses until the current byte has been transmitted. SIO1 will not generate clock pulses for the next byte. Data on SDA originates from the new master once it has won arbitration.

SU00967

Figure 4. Arbitration Procedure



1. Another service pulls the SCL line low before the SIO1 “mark” duration is complete. The serial clock generator is immediately reset and commences with the “space” duration by pulling SCL low.
2. Another device still pulls the SCL line low after SIO1 releases SCL. The serial clock generator is forced into the wait state until the SCL line is released.
3. The SCL line is released, and the serial clock generator commences with the mark duration.

SU00968

Figure 5. Serial Clock Synchronization

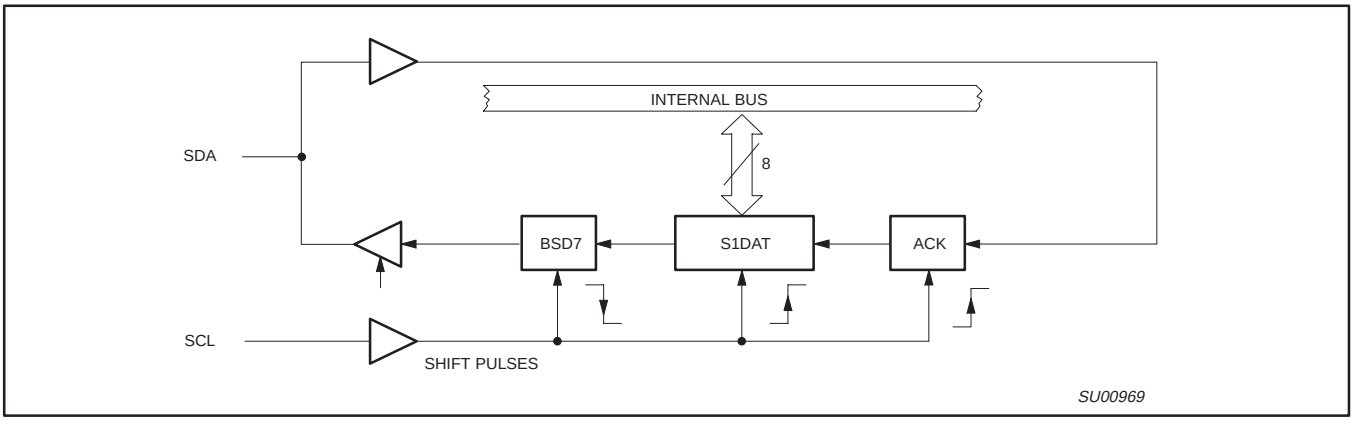


Figure 6. Serial Input/Output Configuration

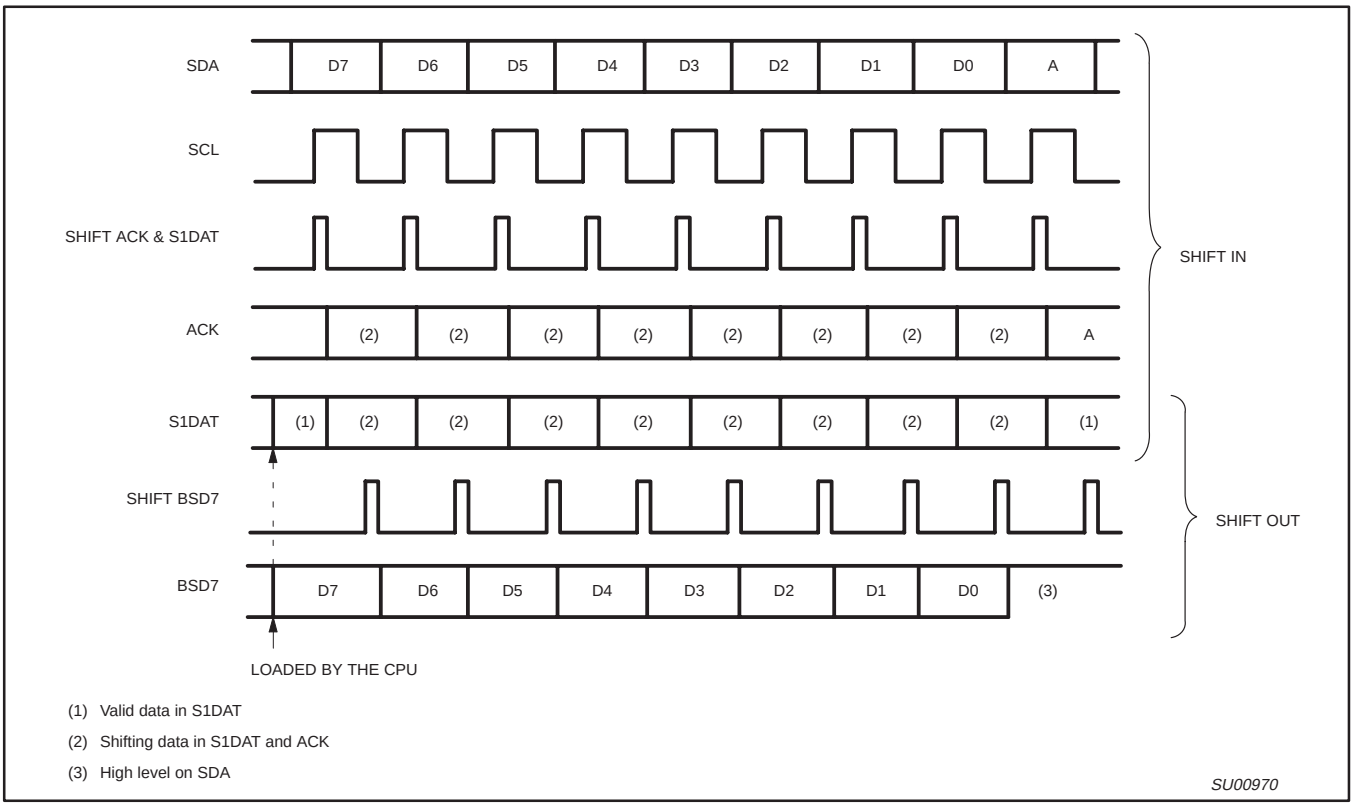


Figure 7. Shift-in and Shift-out Timing

In the following text, it is assumed that ENS1 = “1”.

The “START” Flag, STA: STA = “1”: When the STA bit is set to enter a Master mode, the SIO1 hardware checks the status of the I2C bus and generates a START condition if the bus is free. If the bus is not free, then SIO1 waits for a STOP condition (which will free the bus) and generates a START condition after a delay of half a clock period of the internal serial clock generator.

If STA is set while SIO1 is already in a Master mode and one or more bytes are transmitted or received, SIO1 transmits a repeated START condition. STA may be set at any time. STA may also be set when SIO1 is an addressed slave.

STA = “0”: When the STA bit is reset, no START condition or repeated START condition will be generated.

The STOP Flag, STO: STO = “1”: When the STO bit is set while SIO1 is in a Master mode, a STOP condition is transmitted to the I^2C bus. When the STOP condition is detected on the bus, the SIO1 hardware clears the STO flag. In a Slave mode, the STO flag may be set to recover from an error condition. In this case, no STOP condition is transmitted to the I^2C bus. However, the SIO1 hardware behaves as if a STOP condition has been received and switches to the defined “not addressed” Slave Receiver mode. The STO flag is automatically cleared by hardware.

Table 3. Serial Clock Rates

6-clock mode

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{OSC} 3 MHz	6 MHz	8 MHz	12 MHz[2]	15 MHz[2]	f_{OSC} DIVIDED BY
0	0	0	23	47	62.5	94	117[1]	128
0	0	1	27	54	71	107[1]	134[1]	112
0	1	0	31	63	83.3	125[1]	156[1]	96
0	1	1	37	75	100	150[1]	188[1]	80
1	0	0	6.25	12.5	17	25	31	480
1	0	1	50	100	133[1]	200[1]	250[1]	60
1	1	0	100	200	267[1]	400[1]	500[1]	30
1	1	1	0.24 < 62.5 0 < 255	0.49 < 62.5 0 < 254	0.65 < 55.6 0 < 253	0.98 < 50.0 0 < 251	1.22 < 52.1 0 < 250	48 × (256 – (reload value Timer 1)) Reload value Timer 1 in Mode 2.

12-clock mode

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{OSC} 6 MHz	12 MHz	16 MHz	24 MHz[3]	30 MHz[3]	f_{OSC} DIVIDED BY
0	0	0	23	47	62.5	94	117[1]	256
0	0	1	27	54	71	107[1]	134[1]	224
0	1	0	31	63	83.3	125[1]	156[1]	192
0	1	1	37	75	100	150[1]	188[1]	160
1	0	0	6.25	12.5	17	25	31	960
1	0	1	50	100	133[1]	200[1]	250[1]	120
1	1	0	100	200	267[1]	400[1]	500[1]	60
1	1	1	0.24 < 62.5 0 < 255	0.49 < 62.5 0 < 254	0.65 < 55.6 0 < 253	0.98 < 50.0 0 < 251	1.22 < 52.1 0 < 250	96 × (256 – (reload value Timer 1)) Reload value Timer 1 in Mode 2.

NOTES:
1. These frequencies exceed the upper limit of 100 kHz of the I^2C-bus specification and cannot be used in an I^2C-bus application.
2. At f_{OSC} = 12 MHz/15 MHz the maximum I^2C bus rate of 100 kHz cannot be realized due to the fixed divider rates.
3. At f_{OSC} = 24 MHz/30 MHz the maximum I^2C bus rate of 100 kHz cannot be realized due to the fixed divider rates.

Table 6. Slave Receiver mode

STATUS CODE (S1STA)	STATUS OF THE I^2C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
60H	Own SLA+W has been received; ACK has been returned	No S1DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		no S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
68H	Arbitration lost in SLA+R/$\overline{W}$ as master; Own SLA+W has been received, ACK returned	No S1DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		no S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
70H	General call address (00H) has been received; ACK has been returned	No S1DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		no S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
78H	Arbitration lost in SLA+R/$\overline{W}$ as master; General call address has been received, ACK has been returned	No S1DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		no S1DAT action	X	0	0	1	Data byte will be received and ACK will be returned
80H	Previously addressed with own SLV address; DATA has been received; ACK has been returned	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		read data byte	X	0	0	1	Data byte will be received and ACK will be returned
88H	Previously addressed with own SLA; DATA byte has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		read data byte or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.
90H	Previously addressed with General Call; DATA byte has been received; ACK has been returned	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		read data byte	X	0	0	1	Data byte will be received and ACK will be returned
98H	Previously addressed with General Call; DATA byte has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		read data byte or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

TIMER 0 AND TIMER 1 OPERATION

Timer 0 and Timer 1

The "Timer" or "Counter" function is selected by control bits C/$\overline{T}$ in the Special Function Register TMOD (see Figure 15). These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Mode 0

Putting either Timer into Mode 0 makes it behave as an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 16 shows the Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The counted input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. TRn is a control bit in the Special Function Register TCON (Figure 17). (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements).

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

Mode 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 18. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which is preset by software. The reload leaves THn unchanged.

Mode 2 operation is the same for Timer 0 as for Timer 1.

Mode 3

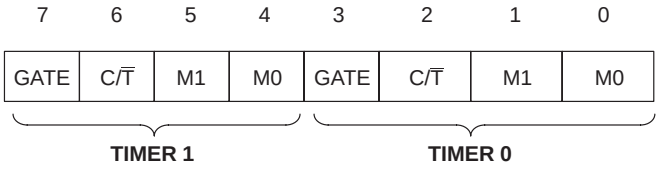
Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 19. TL0 uses the Timer 0 control bits: C/$\overline{T}$, GATE, TR0, and TF0 as well as pin $\overline{INT0}$. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the "Timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer on the counter. Putting Timer 0 in Mode 3 allows an 80C51 to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

TMOD Address = 89H Reset Value = 00H

Not Bit Addressable



BIT	SYMBOL	FUNCTION
TMOD.3/ TMOD.7	GATE	Gating control when set. Timer/Counter "n" is enabled only while "$\overline{INTn}$" pin is high and "TRn" control pin is set. when cleared Timer "n" is enabled whenever "TRn" control bit is set.
TMOD.2/ TMOD.6	C/$\overline{T}$	Timer or Counter Selector cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from "Tn" input pin).

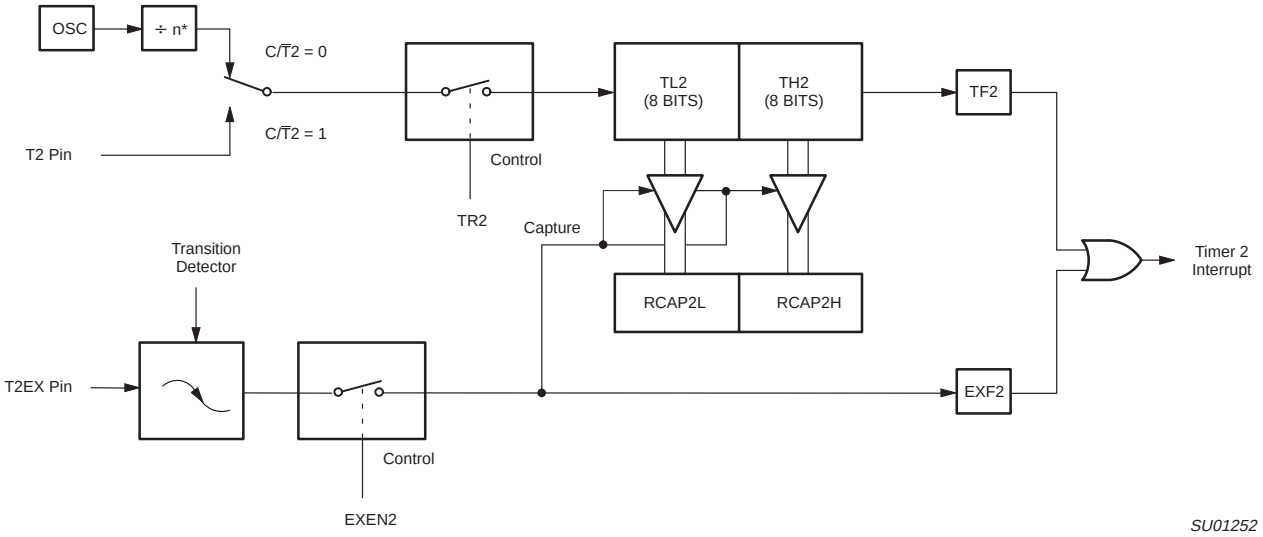
M1	M0	OPERATING
0	0	8048 Timer: "TLn" serves as 5-bit prescaler.
0	1	16-bit Timer/Counter: "THn" and "TLn" are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter: "THn" holds a value which is to be reloaded into "TLn" each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped.

SU01580

Figure 15. Timer/Counter 0/1 Mode Control (TMOD) Register

Table 9. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)



* n = 6 in 6-clock mode, or 12 in 12-clock mode.

Figure 21. Timer 2 in Capture Mode

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T2OE	DCEN
Bit 7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.*
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter depending on the value of the T2EX pin.

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU01714

Figure 22. Timer 2 Mode (T2MOD) Control Register

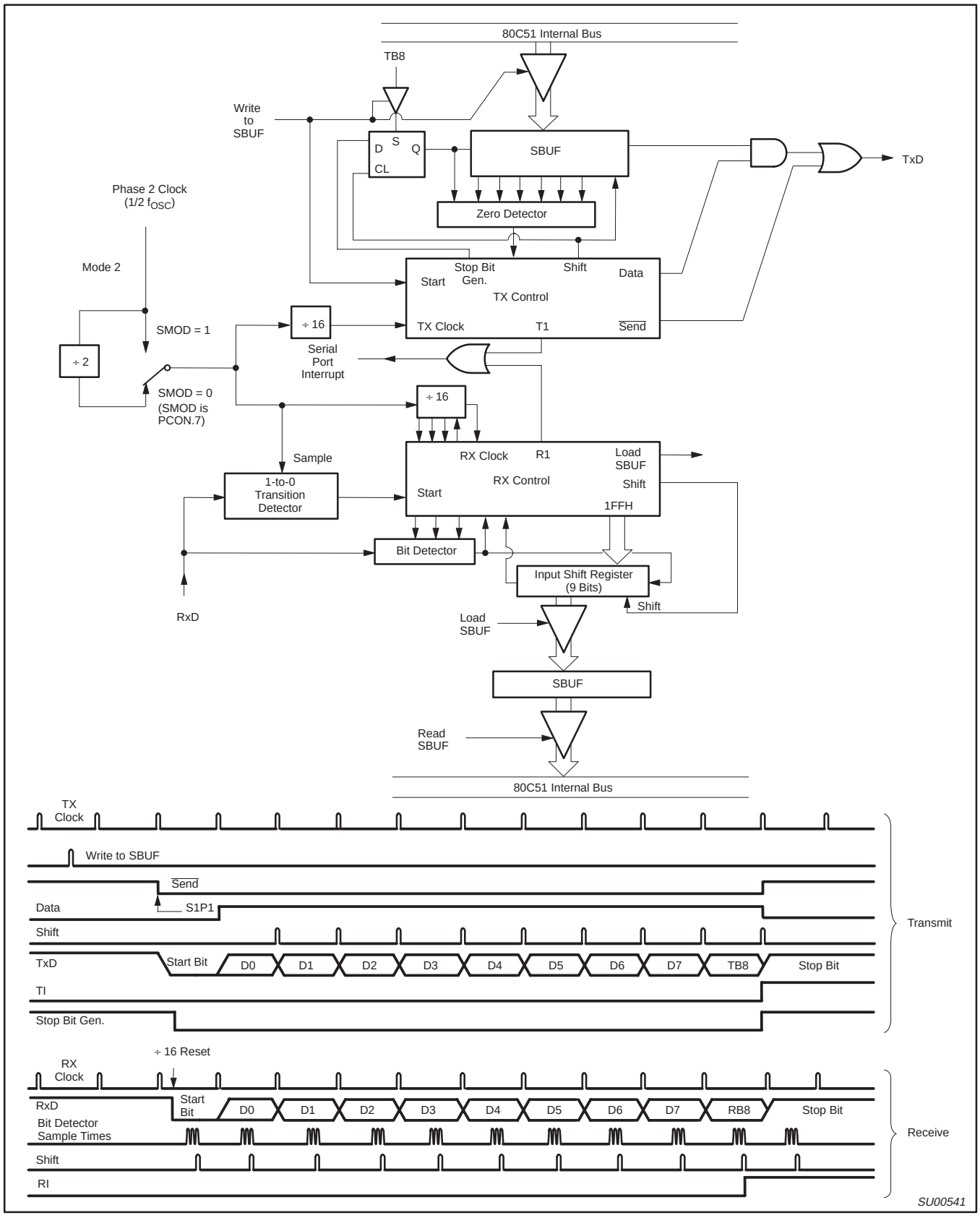


Figure 30. Serial Port Mode 2

Interrupt Priority Structure

The P89C660/662/664/668 has an 8 source four-level interrupt structure (see Table 13).

There are 4 SFRs associated with the four-level interrupt. They are the IE, IP, IEN1, and IPH (see Figures 35, 36, 37, and 38). The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 37.

The function of the IPH SFR, when combined with the IP SFR, determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The priority scheme for servicing the interrupts is the same as that for the 80C51, except that there are four interrupt levels rather than two (as on the 80C51). An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 13. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L)[1] Y (T)[2]	03H
SI01 (I^2C)	2	—	N	2BH
T0	3	TP0	Y	0BH
X1	4	IE1	N (L) Y (T)	13H
T1	5	TF1	Y	1BH
SP	6	RI, TI	N	23H
T2	7	TF2, EXF2	N	3BH
PCA	8	CF, CCFn n = 0–4	N	33H

NOTES:
1. L = Level activated
2. T = Transition activated

	7	6	5	4	3	2	1	0
IEN0 (0A8H)	EA	EC	ES1	ES0	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

BIT	SYMBOL	FUNCTION
IEN0.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
IEN0.6	EC	PCA interrupt enable bit
IEN0.5	ES1	I^2C interrupt enable bit.
IEN0.4	ES0	Serial Port interrupt enable bit.
IEN0.3	ET1	Timer 1 interrupt enable bit.
IEN0.2	EX1	External interrupt 1 enable bit.
IEN0.1	ET0	Timer 0 interrupt enable bit.
IEN0.0	EX0	External interrupt 0 enable bit.

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Figure 35. IE Registers

Programmable Counter Array (PCA)

The Programmable Counter Array available on the 89C66x is a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3(CEX0), module 1 to P1.4(CEX1), etc. The basic PCA configuration is shown in Figure 40.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 43):

CPS1	CPS0	PCA Timer Count Source
0	0	1/6 oscillator frequency (6 clock mode); 1/12 oscillator frequency (12 clock mode)
0	1	1/2 oscillator frequency (6 clock mode); 1/4 oscillator frequency (12 clock mode)
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR, there are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which, when set, causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 41.

The watchdog timer function is implemented in module 4 (see Figure 50).

The CCON SFR contains the run control bit for the PCA, and the flags for the PCA timer (CF) and each module (refer to Figure 44). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system is shown in Figure 42.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 45). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2), when set, causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3), when set, will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set, both edges will be enabled and a capture will occur for either transition. The last bit ECOM (CCAPMn.6), when set, enables the comparator function. Figure 46 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

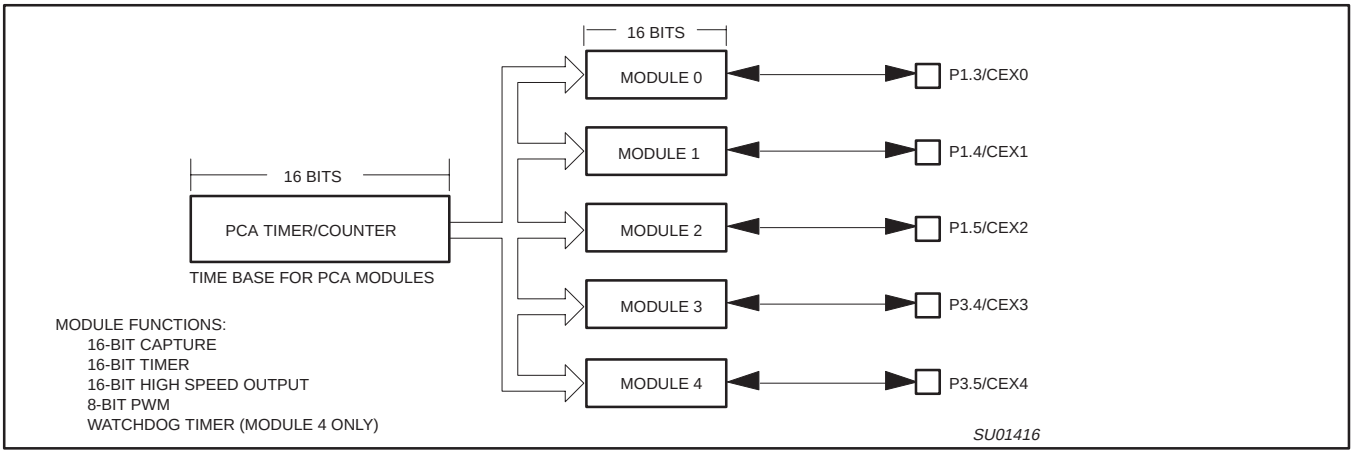

Figure 40. Programmable Counter Array (PCA)

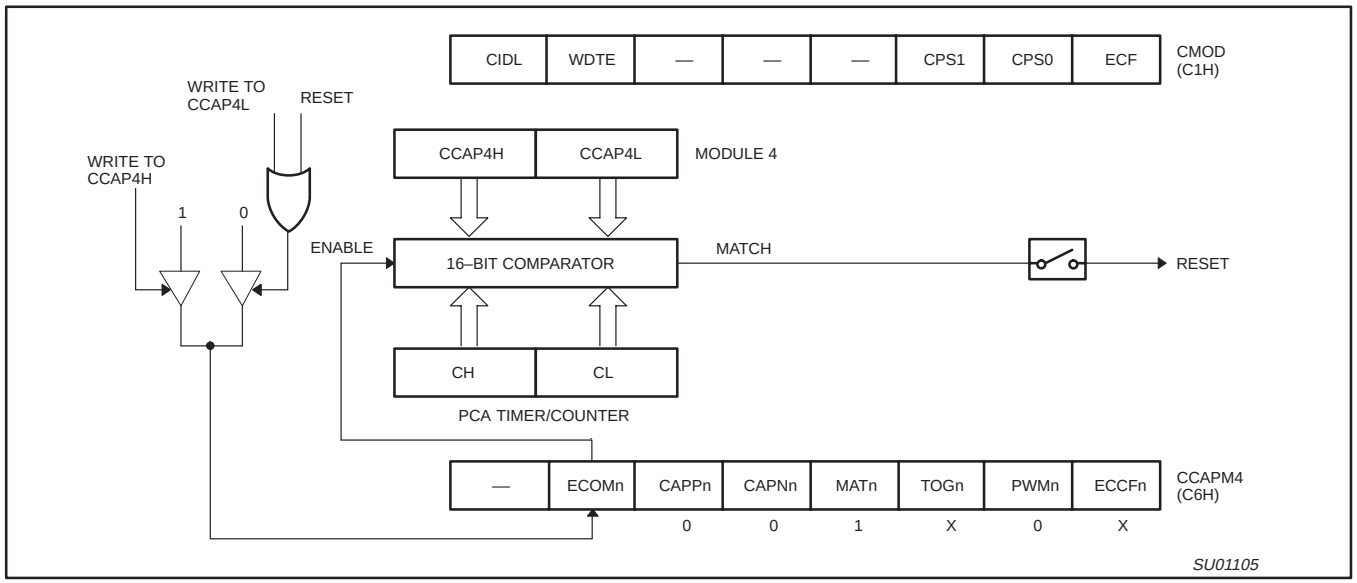

Figure 51. PCA Watchdog Timer m(Module 4 only)

PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed.

Figure 51 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

Figure 52 shows the code for initializing the watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software must periodically change (CCAP4H,CCAP4L) to keep a match from occurring with the PCA timer (CH,CL). This code is given in the WATCHDOG routine in Figure 52.

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within 2^{16} count of the PCA timer.

Expanded Data RAM Addressing

The P89C660/662/664/668 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes expanded RAM (ERAM) (256 bytes for the '660; 768 bytes for the '662; 1792 bytes for the '664; 7936 bytes for the '668).

The four segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
4. The 256/768/1792/7936-bytes expanded RAM (ERAM, 00H – XFFH/2FFH/6FFH/1FFFH) are indirectly accessed by move external instruction, MOVX, and with the EXTRAM bit cleared, see Figure 53.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM, or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing, access SFR space. For example:

MOV 0A0H,A

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing, access the Upper 128 bytes of data RAM. For example:

MOV @R0,A

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

The ERAM can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 256 bytes (660), 768 (662), 1792 (664), 7936 (668) of external data memory.

With EXTRAM = 0, the ERAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ERAM will not affect ports P0, P3.6 (WR#) and P3.7 (RD#). P2 SFR is in output state during external addressing. For example, with EXTRAM = 0,

MOVX @R0,A

where R0 contains 0A0H, access the ERAM at address 0A0H rather than external memory. An access to external data memory locations higher than the ERAM will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51 (with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 54).

With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an 8-bit address multiplexed with data on Port 0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the high-order eight address bits (the contents of DPH) while Port 0 multiplexes the low-order eight address bits (the contents of DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the ERAM.

AUXR Address = 8EH Reset Value = xxxx xx10B

Not Bit Addressable

	—	—	—	—	—	—	**EXTRAM**	**AO**
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
AO	Disable/Enable ALE
	AO **Operating Mode**
	0 ALE is emitted at a constant rate of $^1/_3$ the oscillator frequency (6 clock mode; $^1/_6$ f_{OSC} in 12 clock mode)
	1 ALE is active only during off-chip memory access.
EXTRAM	Internal/External RAM access using MOVX @Ri/@DPTR
	EXTRAM **Operating Mode**
	0 Internal ERAM access using MOVX @Ri/@DPTR
	1 External data memory access.
—	Not implemented, reserved for future use*.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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Figure 53. AUXR: Auxiliary Register

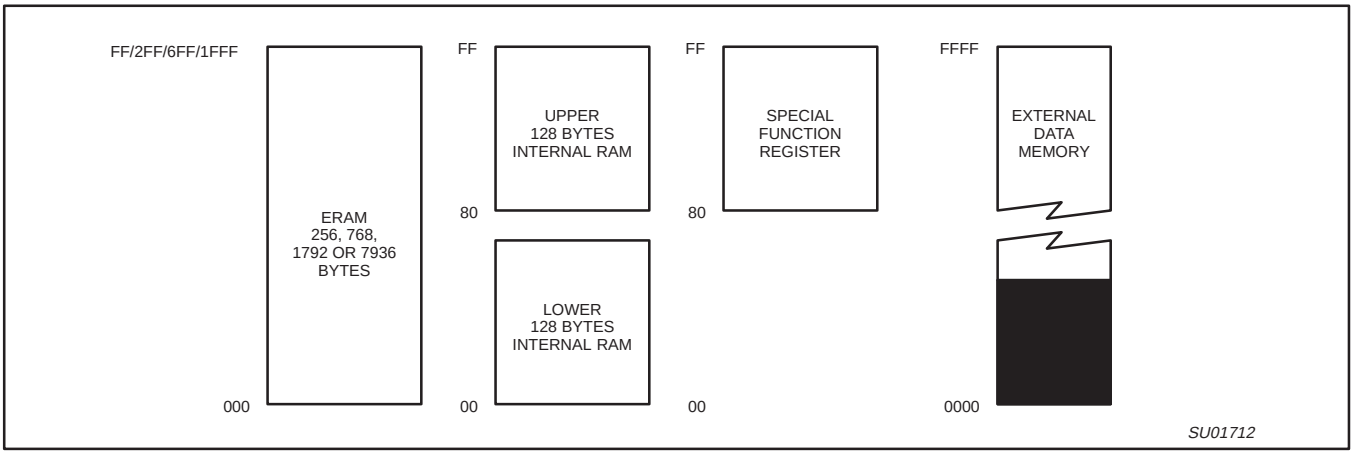

Figure 54. Internal and External Data Memory Address Space with EXTRAM = 0

Hardware WatchDog Timer (One-Time Enabled with Reset-Out for P89C660/662/664/668)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST (SFR location 0A6H). When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output reset HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST (SFR location 0A6H). When WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When the WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $98 \times T_{OSC}$ (6 clock mode; 196 in 12 clock mode), where $T_{OSC} = 1/f_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

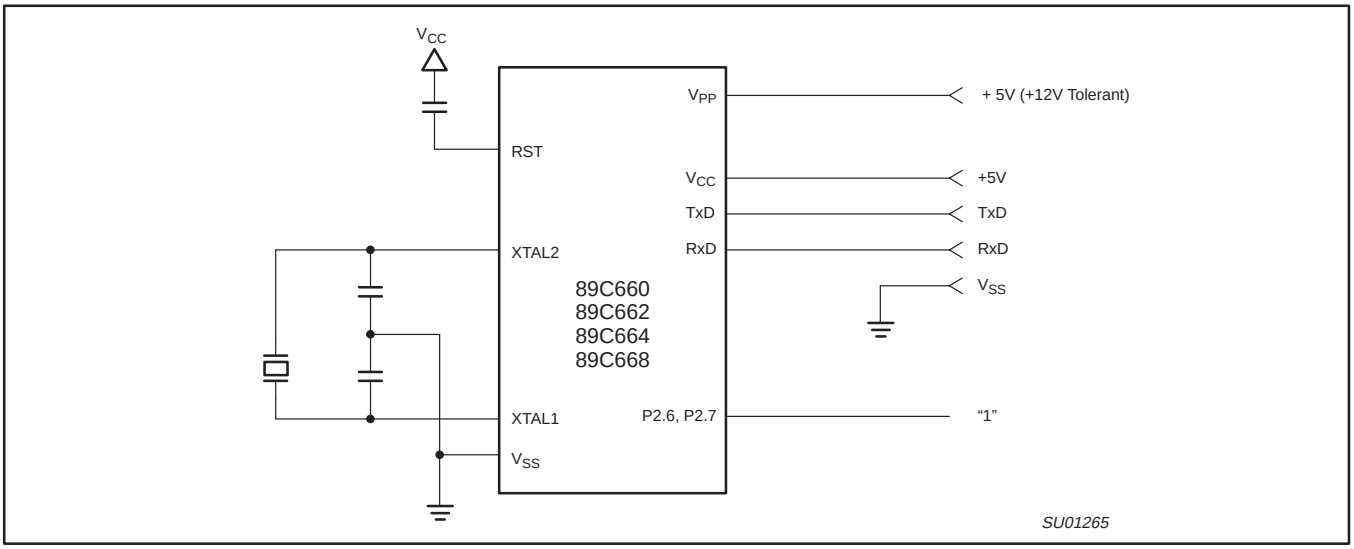

Figure 56. In-System Programming with a Minimum of Pins

In-System Programming (ISP)

The In-System Programming (ISP) is performed without removing the microcontroller from the system. The In-System Programming (ISP) facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89C660/662/664/668 through the serial port. This firmware is provided by Philips and embedded within each P89C660/662/664/668 device.

The Philips In-System Programming (ISP) facility has made in-circuit programming in an embedded application possible with a minimum of additional expense in components and circuit board area.

The ISP function uses five pins: TxD, RxD, V_{SS}, V_{CC}, and V_{PP} (see Figure 56). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature. The V_{PP} supply should be adequately decoupled and V_{PP} not allowed to exceed datasheet limits.

Free ISP software is available on the Philips web site: "WinISP"

1. Direct your browser to the following page: **http://www.semiconductors.philips.com/products/standard/microcontrollers/download/80c51/flash/**
2. Download "WinISP.exe"
3. Execute WinISP.exe to install the software

Free ISP software is also available from the Embedded Systems Academy: "FlashMagic"

1. Direct your browser to the following page: **http://www.esacademy.com/software/flashmagic/**
2. Download Flashmagic
3. Execute "flashmagic.exe" to install the software

Using the In-System Programming (ISP)

The ISP feature allows for a wide range of baud rates to be used in your application, independent of the oscillator frequency. It is also adaptable to a wide range of oscillator frequencies. This is accomplished by measuring the bit-time of a single bit in a received character. This information is then used to program the baud rate in terms of timer counts based on the oscillator frequency. The ISP feature requires that an initial character (an uppercase U) be sent to the P89C660/662/664/668 to establish the baud rate. The ISP firmware provides auto-echo of received characters.

Once baud rate initialization has been performed, the ISP firmware will only accept Intel Hex-type records. Intel Hex records consist of ASCII characters used to represent hexadecimal values and are summarized below:

:NNAAAARRDD..DDCC<crlf>

In the Intel Hex record, the "NN" represents the number of data bytes in the record. The P89C660/662/664/668 will accept up to 16 (10H) data bytes. The "AAAA" string represents the address of the first byte in the record. If there are zero bytes in the record, this field is often set to 0000. The "RR" string indicates the record type. A record type of "00" is a data record. A record type of "01" indicates the end-of-file mark. In this application, additional record types will be added to indicate either commands or data for the ISP facility. The maximum number of data bytes in a record is limited to 16 (decimal). ISP commands are summarized in Table 14.

As a record is received by the P89C660/662/664/668, the information in the record is stored internally and a checksum calculation is performed. The operation indicated by the record type is not performed until the entire record has been received. Should an error occur in the checksum, the P89C660/662/664/668 will send an "X" out the serial port indicating a checksum error. If the checksum calculation is found to match the checksum in the record, then the command will be executed. In most cases, successful reception of the record will be indicated by transmitting a "." character out the serial port (displaying the contents of the internal program memory is an exceptions).

In the case of a Data Record (record type 00), an additional check is made. A "." character will NOT be sent unless the record checksum matched the calculated checksum and all of the bytes in the record were successfully programmed. For a data record, an "X" indicates that the checksum failed to match, and an "R" indicates that one of the bytes did not properly program. It is necessary to send a type 02 record (specify oscillator frequency) to the P89C660/662/664/668 before programming data.

The ISP facility was designed so that specific crystal frequencies were not required in order to generate baud rates or time the programming pulses. The user thus needs to provide the P89C660/662/664/668 with information required to generate the proper timing. Record type 02 is provided for this purpose.

Table 14. Intel-Hex Records Used by In-System Programming

RECORD TYPE	COMMAND/DATA FUNCTION

00	Program Data
	`:nnaaaa00dd....ddcc`
	Where:
	`Nn = number of bytes (hex) in record`
	`Aaaa = memory address of first byte in record`
	`dd....dd = data bytes`
	`cc = checksum`
	Example:
	`:10008000AF5F67F0602703E0322CFA92007780C3FD`

01	End of File (EOF), no operation
	`:xxxxxx01cc`
	Where:
	`xxxxxx = required field, but value is a “don’t care”`
	`cc = checksum`
	Example:
	`:00000001FF`

02	Specify Oscillator Frequency
	`:01xxxx02ddcc`
	Where:
	`xxxx = required field, but value is a “don’t care”`
	`dd = integer oscillator frequency rounded down to nearest MHz`
	`cc = checksum`
	Example:
	`:0100000210ED (dd = 10h = 16, used for 16.0–16.9 MHz)`

IAP CALL	PARAMETER

ERASE BOOT VECTOR & STATUS BYTE	Input Parameters:
	R0 = osc freq (integer)
	R1 = 04h
	R1 = 84h (WDT feed, Rx2 & 66x only)
	DPH = 00h
	DPL = don't care
	Return Parameter
	none
	Sample routine:
	;***** Erase Boot Vector (BV) & Status Byte (SB) *****
	;***** Note: This command erases BOTH the SB & BV
	
	ERSBBV;
	MOV AUXR1,#20H ;set the ENBOOT bit
	MOV R0, #11 ;FOSC
	MOV R1,#04H ;erase status byte & boot vector
	MOV DPH,#00h ;we don't care about DPL
	CALL PGM_MTP ;execute the function
	RET

PROGRAM SECURITY BIT	Input Parameters:
	R0 = osc freq (integer)
	R1 = 05h
	R1 = 85h (WDT feed, Rx2 & 66x only)
	DPH = 00h
	DPL = 00h – security bit # 1 (inhibit writing to Flash)
	01h – security bit # 2 (inhibit Flash verify)
	02h – security bit # 3 (disable external memory)
	Return Parameter
	none
	Sample routines:
	;***** Program Security Bit1 *****
	;***** DPTR indicates security bit to program *****
	
	WRSB1:
	MOV AUXR1,#20H ;set the ENBOOT bit
	MOV R0,#11 ;FOSC
	MOV R1,#05H ;program security bit function
	MOV DPTR,#0000h ;specify security bit 1
	CALL PGM_MTP ;execute the function
	RET
	;***** Program Security Bit2 *****
	;***** DPTR indicates security bit to program *****
	
	WRSB2:
	MOV AUXR1,#20H ;set the ENBOOT bit
	MOV R0,#11 ;FOSC
	MOV R1,#05H ;program security bit function
	MOV DPTR,#0001h ;specify security bit 2
	CALL PGM_MTP ;execute the function
	RET
	;***** Program Security Bit3 *****
	;***** DPTR indicates security bit to program *****
	
	WRSB3:
	MOV AUXR1,#20H ;set the ENBOOT bit
	MOV R0,#11 ;FOSC
	MOV R1,#05H ;program security bit function
	MOV DPTR,#0002h ;specify security bit 3
	CALL PGM_MTP ;execute the function
	RET

AC ELECTRICAL CHARACTERISTICS (6 CLOCK MODE) (Continued)

T_{amb} = 0 °C to +70 °C, V_{CC} = 5 V ± 10% or –40 °C to +85 °C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V[1, 2]

SYMBOL	PARAMETER	INPUT	OUTPUT
I²C Interface			
$t_{HD;STA}$	START condition hold time	≥ 7 t_{CLCL}	> 4.0 µs [4]
t_{LOW}	SCL low time	≥ 8 t_{CLCL}	> 4.7 µs [46]
t_{HIGH}	SCL high time	≥ 7 t_{CLCL}	> 4.0 µs [4]
t_{RC}	SCL rise time	≤ 1 µs	– [5]
t_{FC}	SCL fall time	≤ 0.3 µs	< 0.3 µs [6]
$t_{SU;DAT1}$	Data set-up time	≥ 250 ns	> 10 t_{CLCL} – t_{RD}
$t_{SU;DAT2}$	SDA set-up time (before rep. START cond.)	≥ 250 ns	> 1 µs [4]
$t_{SU;DAT3}$	SDA set-up time (before STOP cond.)	≥ 250 ns	> 4 t_{CLCL}
$t_{HD;DAT}$	Data hold time	≥ 0 ns	> 4 t_{CLCL} – t_{FC}
$t_{SU;STA}$	Repeated START set-up time	≥ 7 t_{CLCL} [4]	> 4.7 µs [4]
$t_{SU;STO}$	STOP condition set-up time	≥ 7 t_{CLCL} [4]	> 4.0 µs [4]
t_{BUF}	Bus free time	≥ 7 t_{CLCL} [4]	> 4.7 µs [4]
t_{RD}	SDA rise time	≤ 1 µs[7]	– [5]
t_{FD}	SDA fall time	≤ 300 ns[7]	< 0.3 µs [6]

NOTES:
1. Parameters are valid over operating temperature range and voltage range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
3. These values are characterized but not 100% production tested.
4. At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
5. Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1 µs.
6. Spikes on the SDA and SCL lines with a duration of less than 3 t_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
7. $t_{CLCL} = 1/f_{OSC}$ = one oscillator clock period at pin XTAL1.

REVISION HISTORY

Rev	Date	Description
_4	20021028	**Product data (9397 750 10403); replaces P89C660/P89C662/P89C664 of 2001 Jul 19 (9397 750 08584) and P89C668 of 2001 Jul 27 (9397 750 08651)** Engineering Change Notice 853–2392 29118 (date: 20021028) Modifications: ● Integrated 89C668 in 89C66x datasheet ● Added more description on I^2C, Timer 0 and Timer 1, and Enhanced UART ● P2.6 must be high to activate the boot loader by hardware (ISP section).