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Details

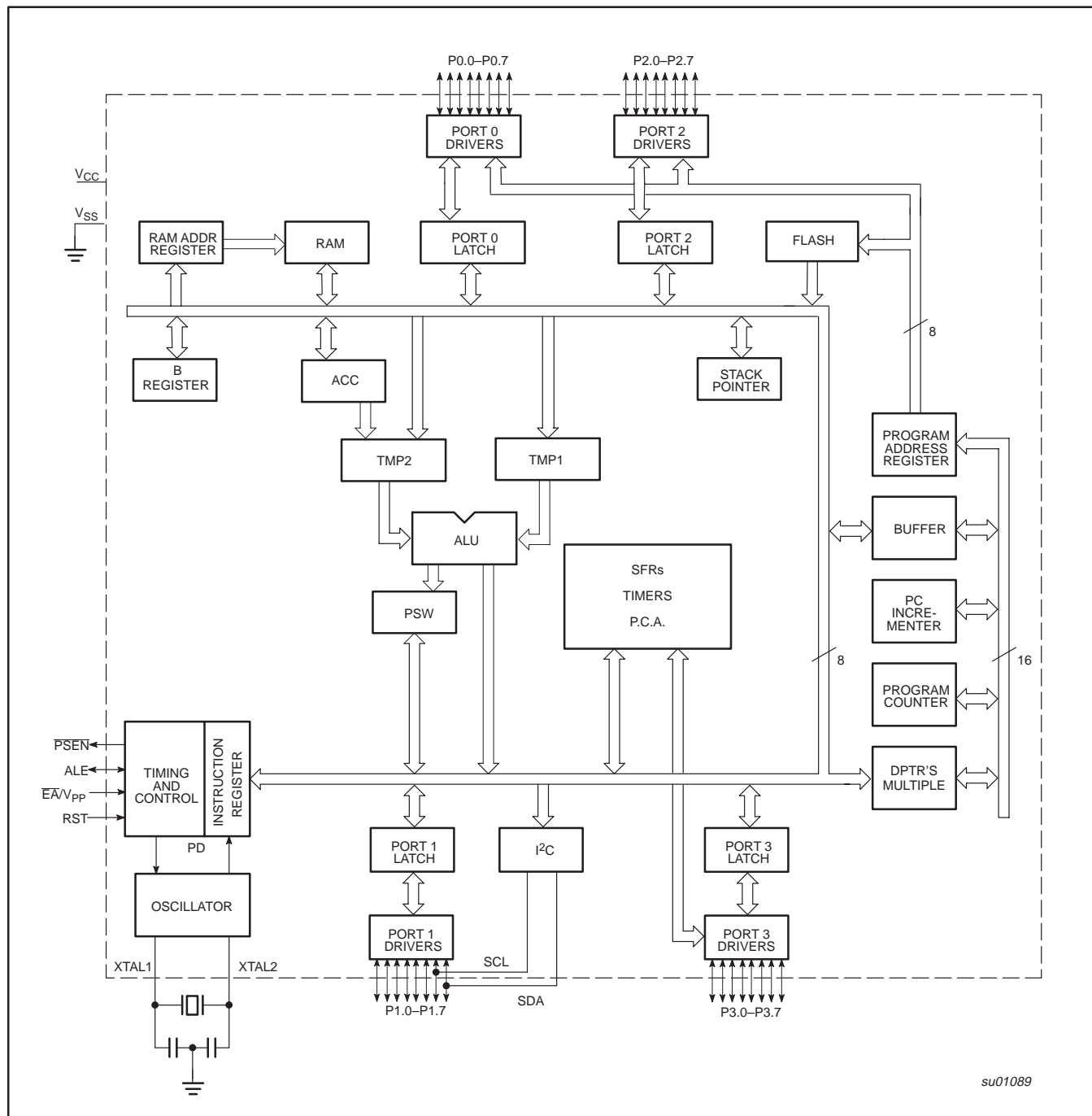
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	I ² C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89c662hfa-00-512

80C51 8-bit Flash microcontroller family

16KB/32KB/64KB ISP/IAP Flash with 512B/1KB/2KB/8KB RAM

P89C660/P89C662/P89C664/
P89C668

BLOCK DIAGRAM (CPU-ORIENTED)

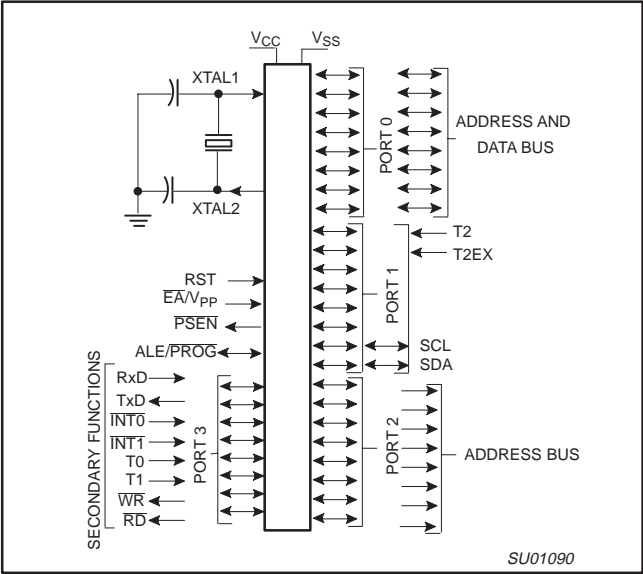


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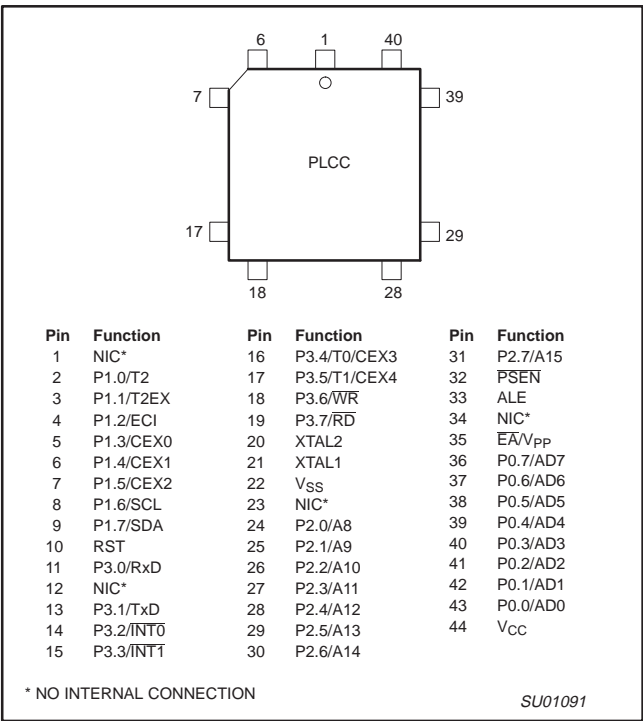
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LOGIC SYMBOL

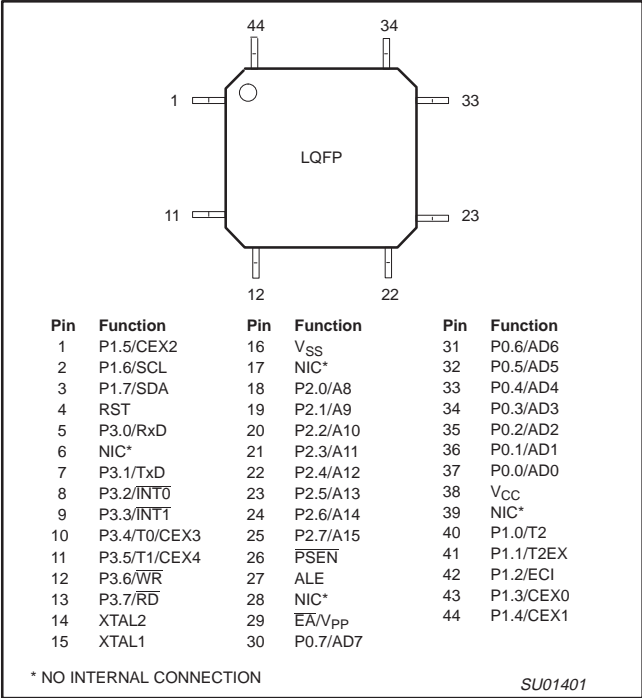


PINNING

Plastic Lead Chip Carrier



Low Quad Flat Pack



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MNEMONIC	PIN NUMBER		TYPE	NAME AND FUNCTION
	PLCC	LQFP		
\overline{EA}/V_{PP}	35	29	I	External Access Enable/Programming Supply Voltage: \overline{EA} must be externally held low to enable the device to fetch code from external program memory locations. If \overline{EA} is held high, the device executes from internal program memory. The value on the \overline{EA} pin is latched when RST is released and any subsequent changes have no effect. This pin also receives the programming supply voltage (V_{PP}) during Flash programming.
XTAL1	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	20	14	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin (other than V_{PP}) must not be higher than $V_{CC} + 0.5$ V or less than $V_{SS} - 0.5$ V.

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LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and reduces system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power-Down mode is suggested.

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power-Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power-Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power-Down mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power-Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power-Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator, but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power-Down.

POWER-ON FLAG

The Power-On Flag (POF) is set by on-chip circuitry when the V_{CC} level on the P89C660/662/664/668 rises from 0 to 5 V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after Power-Down. The V_{CC} level must remain above 3 V for the POF to remain unaffected by the V_{CC} level.

Design Consideration

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, however, access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when the idle mode is terminated by reset, the instruction following the one that invokes the idle mode should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE mode is invoked by:

1. Pulling ALE low while the device is in reset and \overline{PSEN} is high;
2. Holding ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins go into a float state, and the other port pins and ALE and \overline{PSEN} are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency (61 Hz to 4 MHz in 12 clock mode).

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$n \times \left(\frac{\text{Oscillator Frequency}}{65536} - \frac{\text{RCAP2H, RCAP2L}}{2^{16}} \right)$$

n = $\begin{matrix} 2 & \text{in 6 clock mode} \\ 4 & \text{in 12 clock mode} \end{matrix}$

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 2. External Pin Status During Idle and Power-Down mode

MODE	PROGRAM MEMORY	ALE	\overline{PSEN}	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-Down	Internal	0	0	Data	Data	Data	Data
Power-Down	External	0	0	Float	Data	Data	Data

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If the STA and STO bits are both set, the a STOP condition is transmitted to the I²C bus if SIO1 is in a Master mode (in a Slave mode, SIO1 generates an internal STOP condition which is not transmitted). SIO1 then transmits a START condition.

STO = "0": When the STO bit is reset, no STOP condition will be generated.

The Serial Interrupt Flag, SI: SI = "1": When the SI flag is set, then, if the EA and ES1 (interrupt enable register) bits are also set, a serial interrupt is requested. SI is set by hardware when one of 25 of the 26 possible SIO1 states is entered. The only state that does not cause SI to be set is state F8H, which indicates that no relevant state information is available.

While SI is set, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. A high level on the SCL line is unaffected by the serial interrupt flag. SI must be reset by software.

SI = "0": When the SI flag is reset, no serial interrupt is requested, and there is no stretching of the serial clock on the SCL line.

The Assert Acknowledge Flag, AA: AA = "1": If the AA flag is set, an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when:

- The "own slave address" has been received
- The general call address has been received while the general call bit (GC) in S1ADR is set
- A data byte has been received while SIO1 is in the Master Receiver mode
- A data byte has been received while SIO1 is in the addressed Slave Receiver mode

AA = "0": if the AA flag is reset, a not acknowledge (high level to SDA) will be returned during the acknowledge clock pulse on SCL when:

- A data has been received while SIO1 is in the Master Receiver mode
- A data byte has been received while SIO1 is in the addressed Slave Receiver mode

When SIO1 is in the addressed Slave Transmitter mode, state C8H will be entered after the last serial is transmitted (see Figure 11).

When SI is cleared, SIO1 leaves state C8H, enters the not addressed Slave Receiver mode, and the SDA line remains at a high level. In state C8H, the AA flag can be set again for future address recognition.

When SIO1 is in the not addressed Slave mode, its own slave address and the general call address are ignored. Consequently, no acknowledge is returned, and a serial interrupt is not requested. Thus, SIO1 can be temporarily released from the I²C bus while the bus status is monitored. While SIO1 is released from the bus, START and STOP conditions are detected, and serial data is shifted in. Address recognition can be resumed at any time by setting the AA flag. If the AA flag is set when the part's own Slave address or the general call address has been partly received, the address will be recognized at the end of the byte transmission.

The Clock Rate Bits CR0, CR1, and CR2: These three bits determine the serial clock frequency when SIO1 is in a Master mode. The various serial rates are shown in Table 3.

A 12.5 kHz bit rate may be used by devices that interface to the I²C bus via standard I/O port lines which are software driven and slow. 100 kHz is usually the maximum bit rate and can be derived from a 16 MHz, 12 MHz, or a 6 MHz oscillator. A variable bit rate (0.5 kHz to 62.5 kHz) may also be used if Timer 1 is not required for any other purpose while SIO1 is in a Master mode.

The frequencies shown in Table 3 are unimportant when SIO1 is in a Slave mode. In the Slave modes, SIO1 will automatically synchronize with any clock frequency up to 100 kHz.

The Status Register, S1STA

S1STA is an 8-bit read-only special function register. The three least significant bits are always zero. The five most significant bits contain the status code. There are 26 possible status codes. When S1STA contains F8H, no relevant state information is available and no serial interrupt is requested. All other S1STA values correspond to defined SIO1 states. When each of these states is entered, a serial interrupt is requested (SI = "1"). A valid status code is present in S1STA one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software.

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Table 3. Serial Clock Rates

6-clock mode								
CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{osc}					f_{osc} DIVIDED BY
			3 MHz	6 MHz	8 MHz	12 MHz ²	15 MHz ²	
0	0	0	23	47	62.5	94	117 ¹	128
0	0	1	27	54	71	107 ¹	134 ¹	112
0	1	0	31	63	83.3	125 ¹	156 ¹	96
0	1	1	37	75	100	150 ¹	188 ¹	80
1	0	0	6.25	12.5	17	25	31	480
1	0	1	50	100	133 ¹	200 ¹	250 ¹	60
1	1	0	100	200	267 ¹	400 ¹	500 ¹	30
1	1	1	0.24 < 62.5 0 < 255	0.49 < 62.5 0 < 254	0.65 < 55.6 0 < 253	0.98 < 50.0 0 < 251	1.22 < 52.1 0 < 250	48 × (256 – (reload value Timer 1)) Reload value Timer 1 in Mode 2.
12-clock mode								
CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{osc}					f_{osc} DIVIDED BY
			6 MHz	12 MHz	16 MHz	24 MHz ³	30 MHz ³	
0	0	0	23	47	62.5	94	117 ¹	256
0	0	1	27	54	71	107 ¹	134 ¹	224
0	1	0	31	63	83.3	125 ¹	156 ¹	192
0	1	1	37	75	100	150 ¹	188 ¹	160
1	0	0	6.25	12.5	17	25	31	960
1	0	1	50	100	133 ¹	200 ¹	250 ¹	120
1	1	0	100	200	267 ¹	400 ¹	500 ¹	60
1	1	1	0.24 < 62.5 0 < 255	0.49 < 62.5 0 < 254	0.65 < 55.6 0 < 253	0.98 < 50.0 0 < 251	1.22 < 52.1 0 < 250	96 × (256 – (reload value Timer 1)) Reload value Timer 1 in Mode 2.

NOTES:

1. These frequencies exceed the upper limit of 100 kHz of the I²C-bus specification and cannot be used in an I²C-bus application.
2. At f_{osc} = 12 MHz/15 MHz the maximum I²C bus rate of 100 kHz cannot be realized due to the fixed divider rates.
3. At f_{osc} = 24 MHz/30 MHz the maximum I²C bus rate of 100 kHz cannot be realized due to the fixed divider rates.

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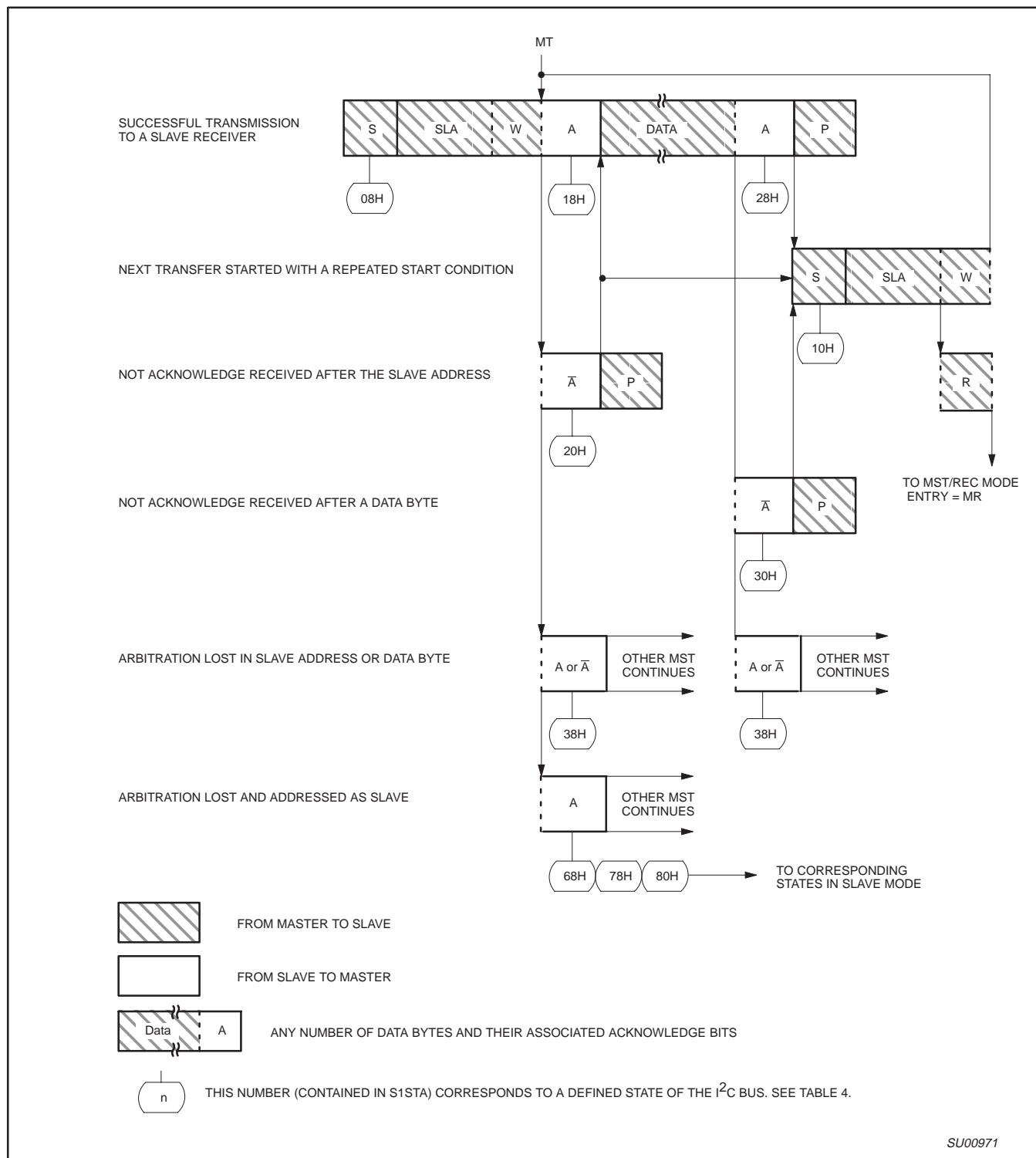


Figure 8. Format and States in the Master Transmitter mode

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SCON Address = 98H		Reset Value = 00H							
Bit Addressable		7	6	5	4	3	2	1	0
		SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	$f_{OSC}/12$ (12-clock mode) or $f_{OSC}/6$ (6-clock mode)
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$ (12-clock mode) or $f_{OSC}/32$ or $f_{OSC}/16$ (6-clock mode)
1	1	3	9-bit UART	variable

SM2 Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.

REN Enables serial reception. Set by software to enable reception. Clear by software to disable reception.

TB8 The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

RB8 In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, if SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.

RI Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

SU01626

Figure 26. Serial Port Control (SCON) Register

Baud Rate			f_{osc}	SMOD	Timer 1		
Mode	12-clock mode	6-clock mode			C/T	Mode	Reload Value
Mode 0 Max	1.67 MHz	3.34 MHz	20 MHz	X	X	X	X
Mode 2 Max	625 k	1250 k	20 MHz	1	X	X	X
Mode 1, 3 Max	104.2 k	208.4 k	20 MHz	1	0	2	FFH
Mode 1, 3	19.2 k	38.4 k	11.059 MHz	1	0	2	FDH
	9.6 k	19.2 k	11.059 MHz	0	0	2	FDH
	4.8 k	9.6 k	11.059 MHz	0	0	2	FAH
	2.4 k	4.8 k	11.059 MHz	0	0	2	F4H
	1.2 k	2.4 k	11.059 MHz	0	0	2	E8H
	137.5	275	11.986 MHz	0	0	2	1DH
	110	220	6 MHz	0	0	2	72H
	110	220	12 MHz	0	0	1	FE8BH

Figure 27. Timer 1 Generated Commonly Used Baud Rates

More About Mode 0

Serial data enters and exits through Rx/D. Tx/D outputs the shift clock. Eight data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency (12-clock mode) or 1/6 the oscillator frequency (6-clock mode).

Figure 28 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between "write to SBUF" and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At

S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after "write to SBUF."

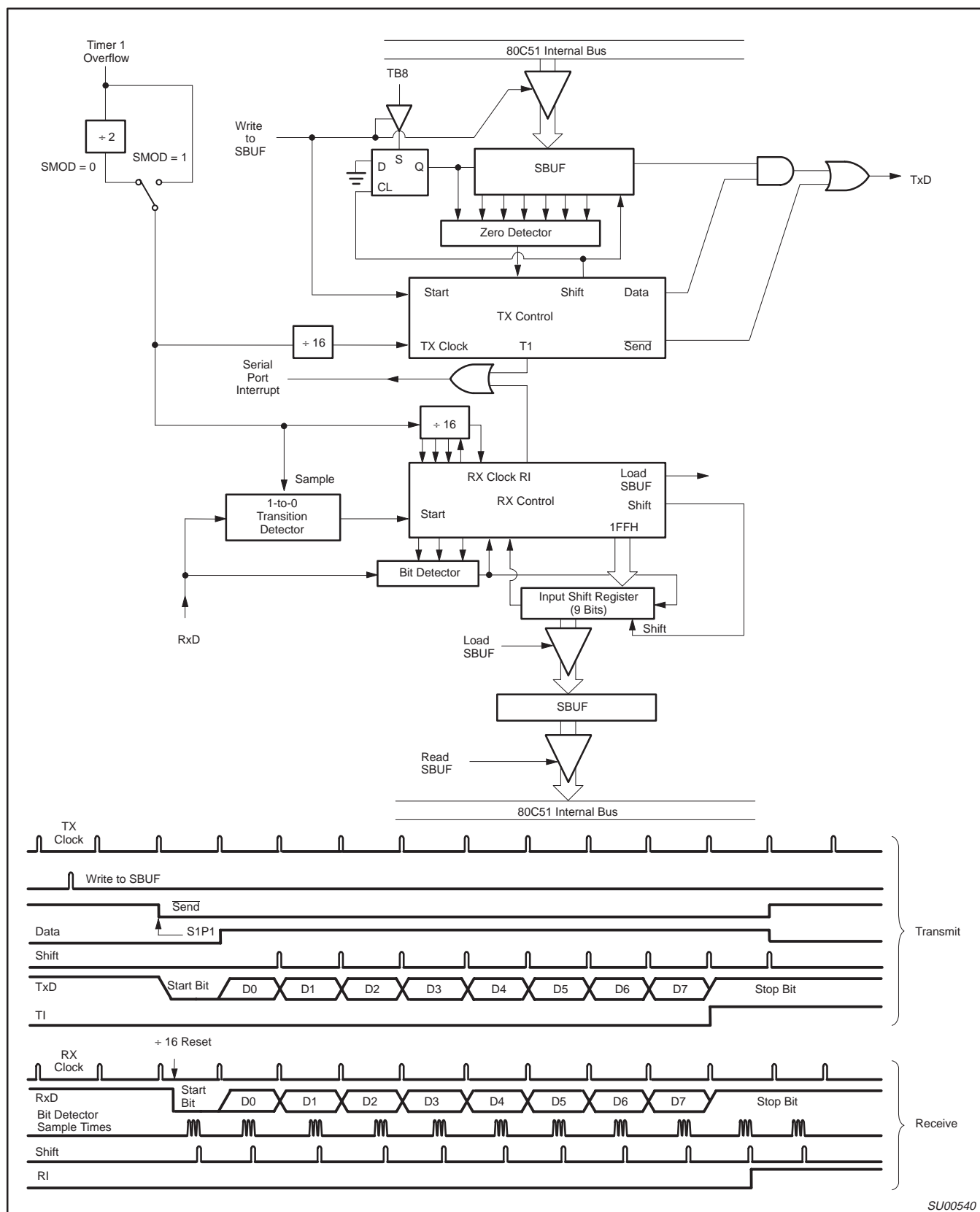
Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and activates RECEIVE in the next clock phase.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are

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SU00540

Figure 29. Serial Port Mode 1

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Enhanced UART

In addition to the standard operation, the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the S0CON register. The FE bit shares the S0CON.7 bit with SM0, and the function of S0CON.7 is determined by PCON.6 (SMOD0) (see Figure 32). If SMOD0 is set then S0CON.7 functions as FE. S0CON.7 functions as SM0 when SMOD0 is cleared. When used as FE, S0CON.7 can only be cleared by software (refer to Figure 33).

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in S0CON. In the 9-bit UART modes (mode 2 and mode 3), the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 34.

The 8-bit mode is called Mode 1. In this mode, the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits, and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1101
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	1111 1110
	Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1001
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	1111 1010
	Given =	1110 0X0X
Slave 2	SADDR =	1110 0000
	SADEN =	1111 1100
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset, SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

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CMOD Address = C1H					Reset Value = 00XX X000B			
	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF
Bit:	7	6	5	4	3	2	1	0
Symbol	Function							
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.							
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.							
–	Not implemented, reserved for future use.*							
CPS1	PCA Count Pulse Select bit 1.							
CPS0	PCA Count Pulse Select bit 0.							
	CPS1	CPS0	Selected PCA Input**					
	0	0	0	Internal clock, $f_{OSC}/6$ in 6 clock mode ($f_{OSC}/12$ in 12 clock mode)				
	0	1	1	Internal clock, $f_{OSC}/2$ in 6 clock mode ($f_{OSC}/4$ in 12 clock mode)				
	1	0	2	Timer 0 overflow				
	1	1	3	External clock at ECI/P1.2 pin (max. rate = $f_{OSC}/4$ in 6 clock mode, $f_{OCS}/8$ in 12 clock mode)				
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.							
NOTE:								
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.								
** f_{OSC} = oscillator frequency								

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SU01257

Figure 43. CMOD: PCA Counter Mode Register

CCON Address = 0C0H

Reset Value = 00X0 0000B

Bit Addressable

	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
–	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

NOTE:

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU01099

SU01099

Figure 44. CCON: PCA Counter Control Register

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16KB/32KB/64KB ISP/IAP Flash with 512B/1KB/2KB/8KB RAM

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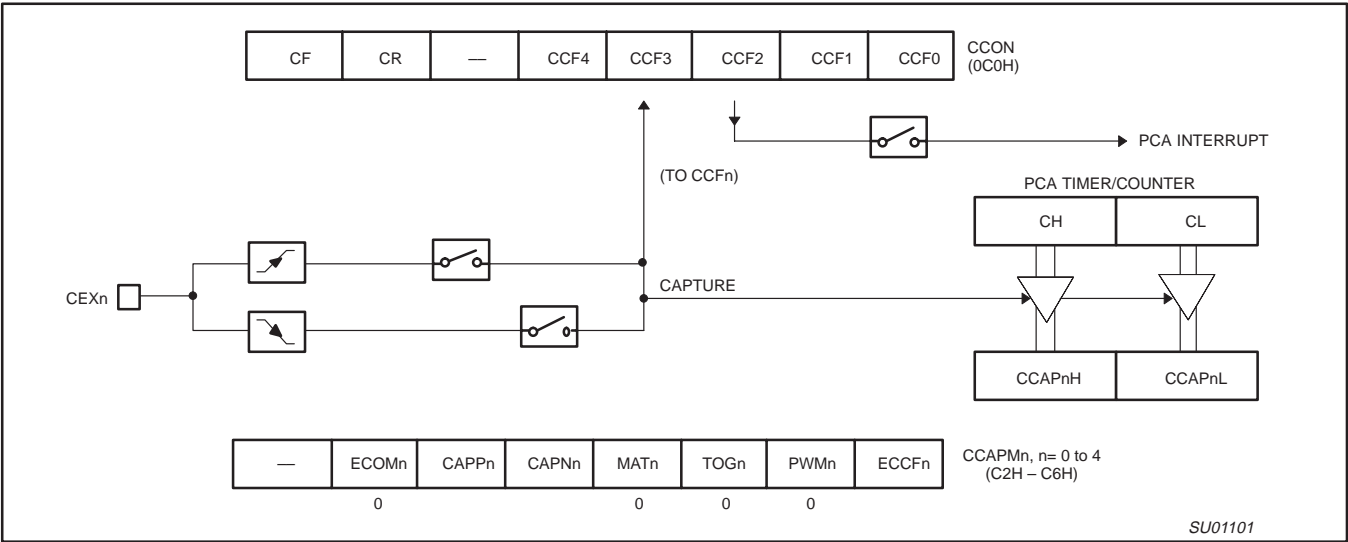


Figure 47. PCA Capture Mode

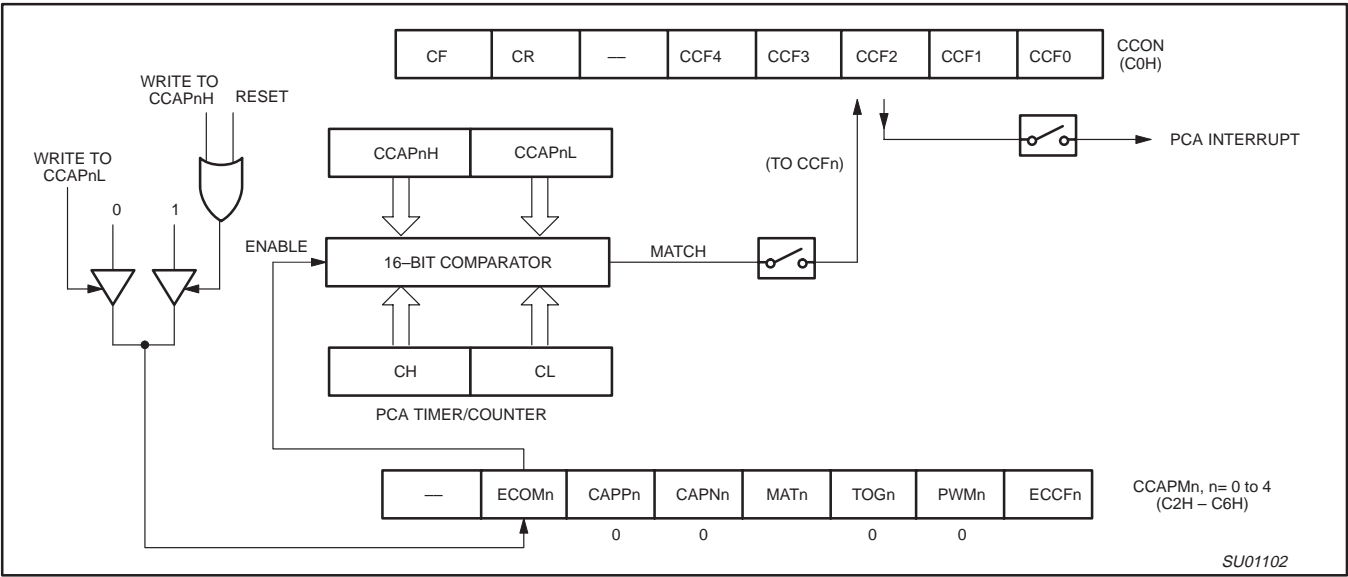


Figure 48. PCA Compare Mode

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16KB/32KB/64KB ISP/IAP Flash with 512B/1KB/2KB/8KB RAM

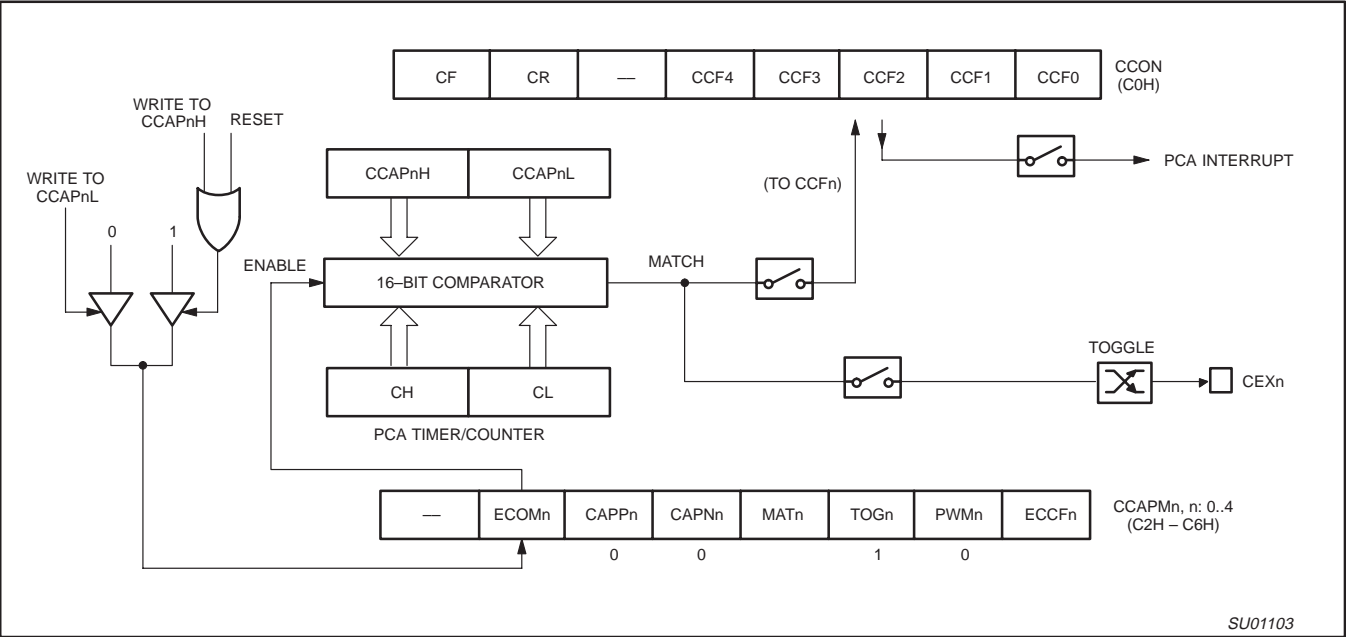


Figure 49. PCA High Speed Output Mode

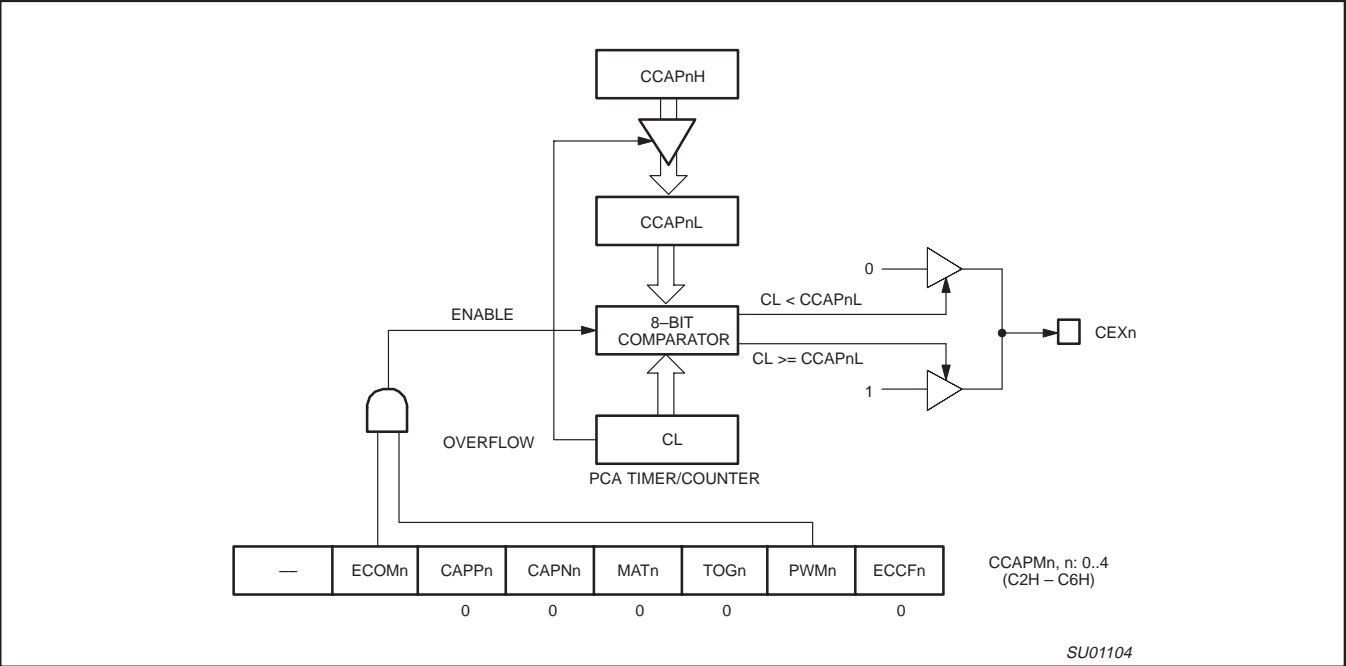


Figure 50. PCA PWM Mode

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P89C660/P89C662/P89C664/
P89C668

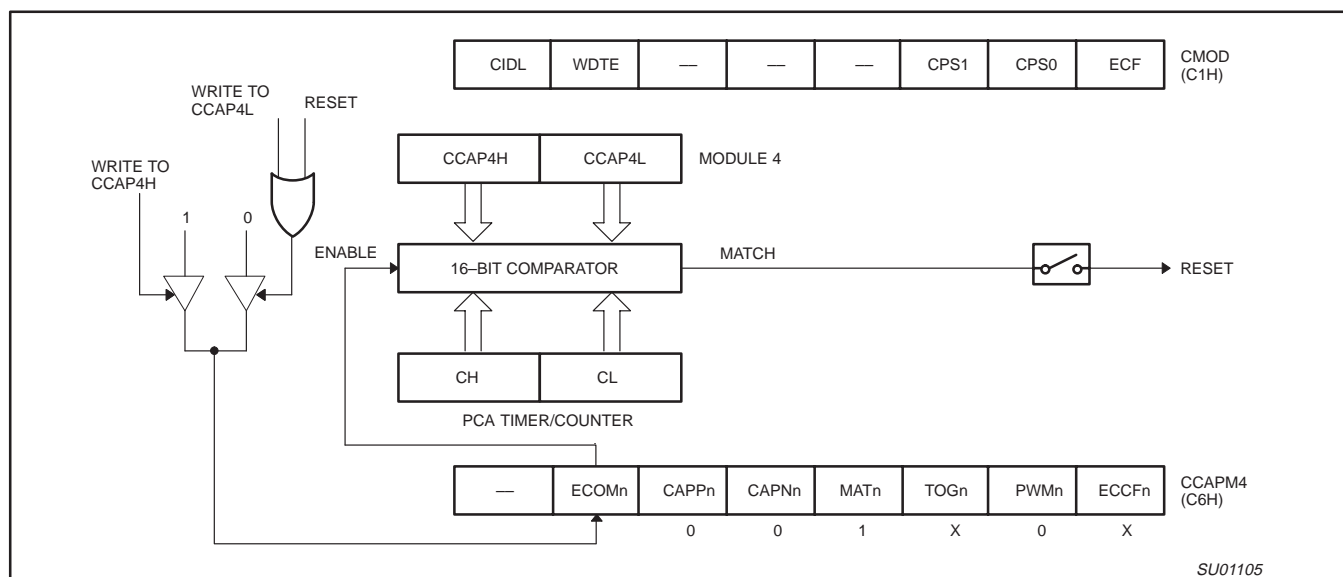


Figure 51. PCA Watchdog Timer m(Module 4 only)

PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed.

Figure 51 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

Figure 52 shows the code for initializing the watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the WATCHDOG routine in Figure 52.

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within 2^{16} count of the PCA timer.

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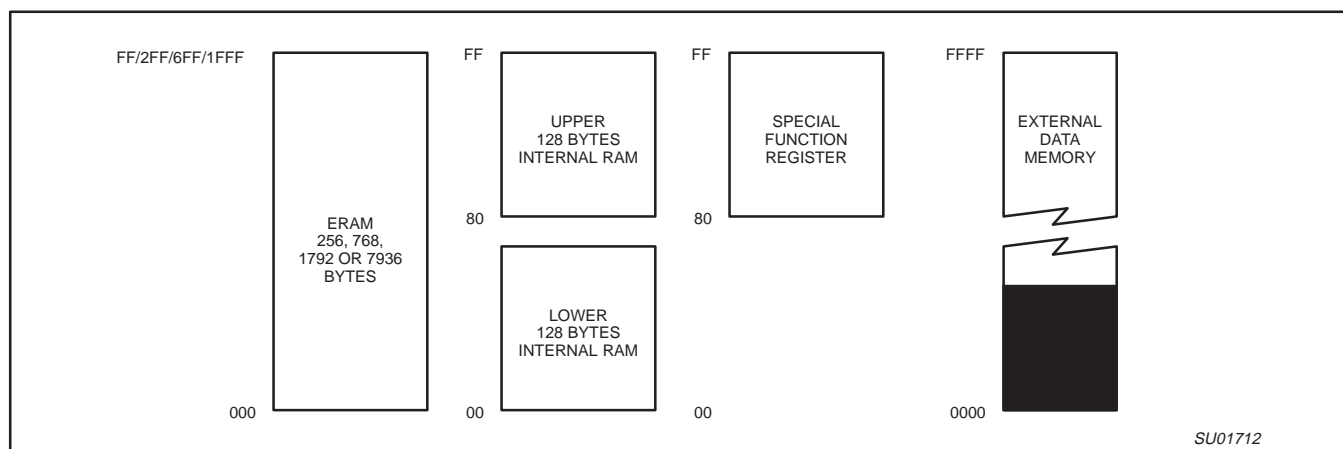


Figure 54. Internal and External Data Memory Address Space with EXTRAM = 0

Hardware WatchDog Timer (One-Time Enabled with Reset-Out for P89C660/662/664/668)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST (SFR location 0A6H). When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output reset HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST (SFR location 0A6H). When WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When the WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $98 \times T_{OSC}$ (6 clock mode; 196 in 12 clock mode), where $T_{OSC} = 1/f_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

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16KB/32KB/64KB ISP/IAP Flash with 512B/1KB/2KB/8KB RAM

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IAP CALL	PARAMETER
PROGRAM STATUS BYTE	<p>Input Parameters:</p> <p>R0 = osc freq (integer) R1 = 06h R1 = 86h (WDT feed, Rx2, 66x only) DPH = 00h DPL = 00h - program status byte ACC = status byte</p> <p>Return Parameter</p> <p>ACC = 00 if pass; not 00 if fails</p> <p>Sample routine:</p> <pre> ;***** Program Status Byte (SB) ***** ;***** DPTR indicates program status byte ***** ;***** ACC holds new value of Status Byte to program ***** WRSB: MOV AUXR1,#20H ;set the ENBOOT bit MOV R0,#11 ;FOSC MOV R1,#06H ;program status byte or boot vector MOV DPTR,#0000h ;specify status byte MOV A,NEW_SB ; CALL PGM_MTP ;execute the function RET </pre>
PROGRAM BOOT VECTOR	<p>Input Parameters:</p> <p>R0 = osc freq (integer) R1 = 06h R1 = 86h (WDT feed, Rx2 & 66x only) DPH = 00h DPL = 01h - program boot vector ACC = boot vector</p> <p>Return Parameter</p> <p>ACC = 00 if pass; not 00 if fails</p> <p>Sample routine:</p> <pre> ;***** Program Boot Vector (BV) ***** ;***** DPTR indicates program boot vector ***** ;***** ACC holds new value of boot vector to program ***** WRBV: MOV AUXR1,#20H ;set the ENBOOT bit MOV R0,#11 ;FOSC MOV R1,#06H ;program status byte or boot vector MOV DPTR,#0001h ;specify boot vector MOV A,NEW_SB ;new value for the boot vector CALL PGM_MTP ;execute the function RET </pre>
READ DEVICE DATA	<p>Input Parameters:</p> <p>R1 = 03h R1 = 83h (WDT feed, Rx2 & 66x only) DPTR = address of byte to read</p> <p>Return Parameter</p> <p>ACC = value of byte read</p> <p>Sample routine:</p> <pre> ;*****reads the Device Data (DData) ***** ;***** DData returned in ACC ***** ;***** DPTR holds address of byte to read ***** RDData: MOV AUXR1,#20H ;set the ENBOOT bit MOV R0,#11 ;FOSC MOV R1,#03H ;read data function MOV DPTR,Address ;specify address of byte to read CALL PGM_MTP ;execute the function RET </pre>

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DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}, 5\text{ V} \pm 10\%$ or $-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}; 5\text{ V} \pm 5\%; V_{SS} = 0\text{ V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA ¹¹		-0.5		$0.3 V_{DD}$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, \overline{EA})		$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA ¹¹		$0.7 V_{DD}$		6.0	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 1.6\text{ mA}^2$	–		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, \overline{PSEN} ^{7, 8}	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 3.2\text{ mA}^2$	–		0.45	V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA	$I_{OL} = 3.0\text{ mA}$	–		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -30\text{ }\mu\text{A}$	$V_{CC} - 0.7$		–	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , \overline{PSEN} ³	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$		–	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-75	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{ V}$ See Note 4	–		-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$	–		± 10	μA
I_{L2}	Input leakage current, P1.6/SCL, P1.7/SDA	$0\text{ V} < V_I < 6\text{ V}$ $0\text{ V} < V_{DD} < 5.5\text{ V}$	–		10	μA
I_{CC}	Power supply current (see Figure 64): Active mode (see Note 5) Idle mode (see Note 5) Power-Down mode or clock stopped (see Figure 71 for conditions) Programming and erase mode	See Note 5 $T_{amb} = 0\text{ }^{\circ}\text{C to }70\text{ }^{\circ}\text{C}$ $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ $f_{osc} = 20\text{ MHz}$		20 60	100 125	μA μA mA
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except \overline{EA})		–		15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and \overline{PSEN} to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 68 through 71 for I_{CC} test conditions and Figure 64 for I_{CC} vs Freq.
Active mode: $I_{CC(MAX)} = (2.8 \times \text{FREQ.} + 8.0)\text{mA}$ for all devices, in 6 clock mode; $(1.4 \times \text{FREQ.} + 8.0)\text{mA}$ in 12 clock mode.
Idle mode: $I_{CC(MAX)} = (1.2 \times \text{FREQ.} + 1.0)\text{mA}$ in 6 clock mode; $(0.6 \times \text{FREQ.} + 1.0)\text{mA}$ in 12 clock mode.
- This value applies to $T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$.
- Load capacitance for port 0, ALE, and $\overline{PSEN} = 100\text{ pF}$, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 °C specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except \overline{EA} is 25 pF).
- The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5 V will be recognized as a logic 0 while an input voltage above 3.0 V will be recognized as a logic 1.

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16KB/32KB/64KB ISP/IAP Flash with 512B/1KB/2KB/8KB RAM

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE

P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

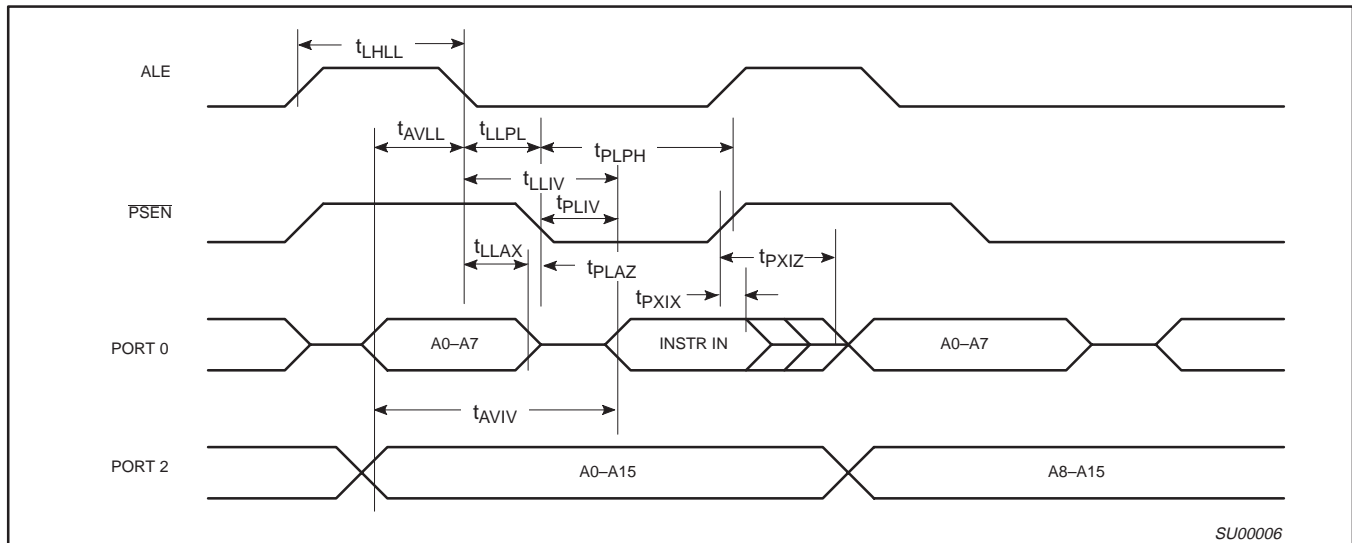


Figure 57. External Program Memory Read Cycle

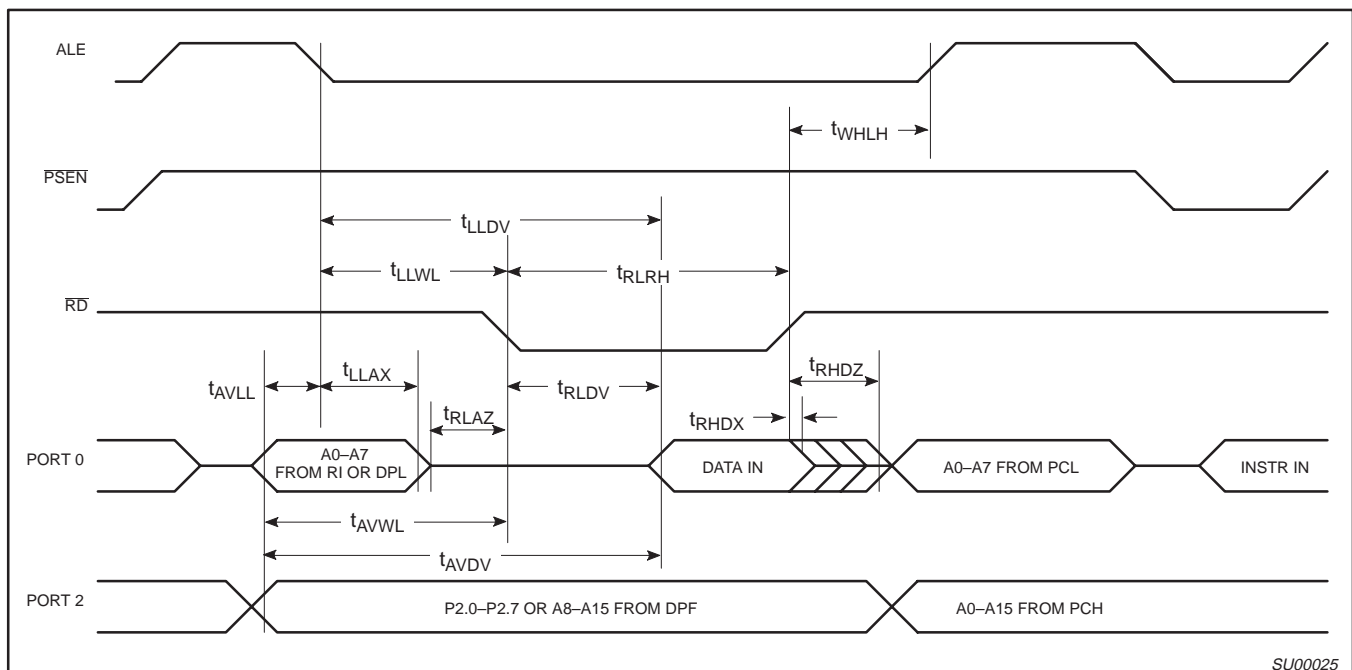


Figure 58. External Data Memory Read Cycle

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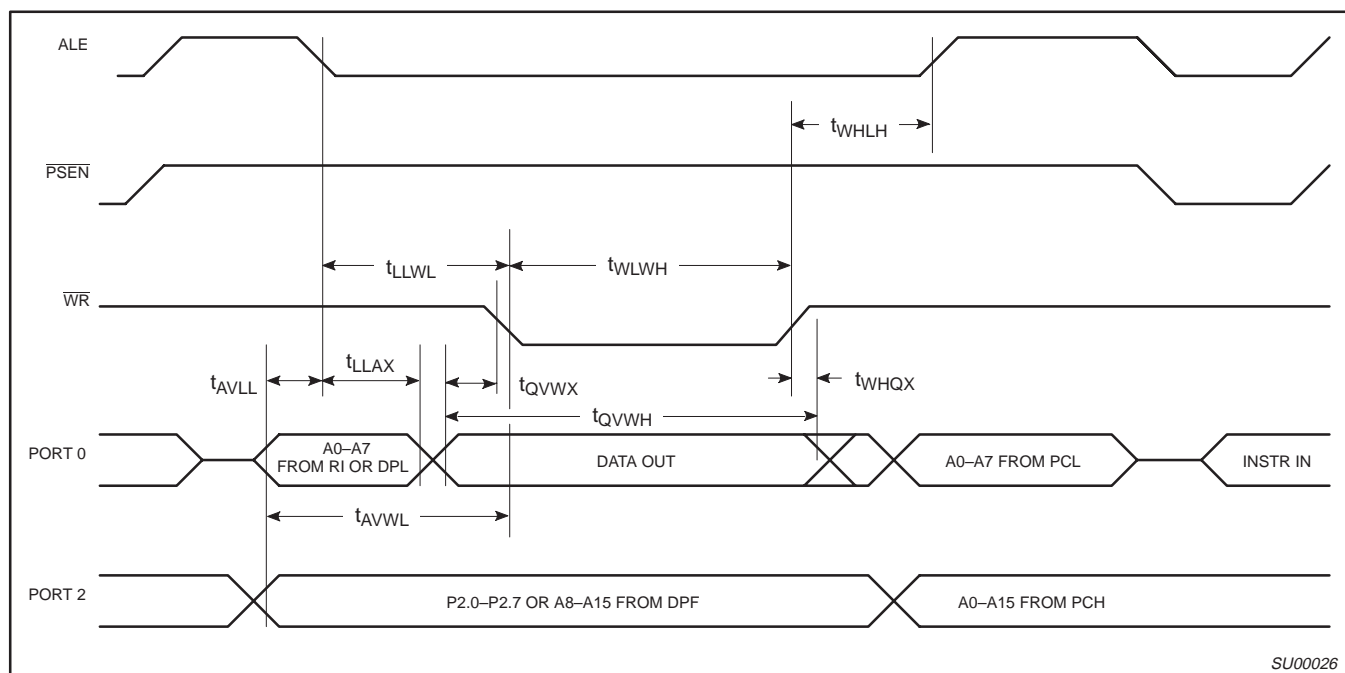


Figure 59. External Data Memory Write Cycle

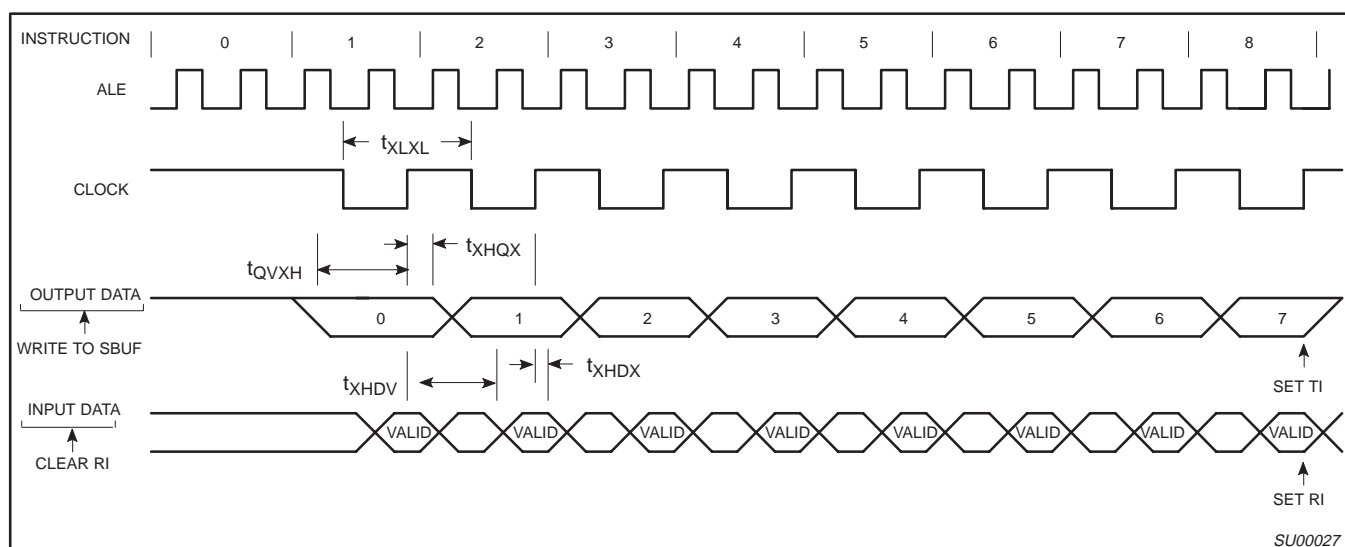


Figure 60. Shift Register Mode Timing

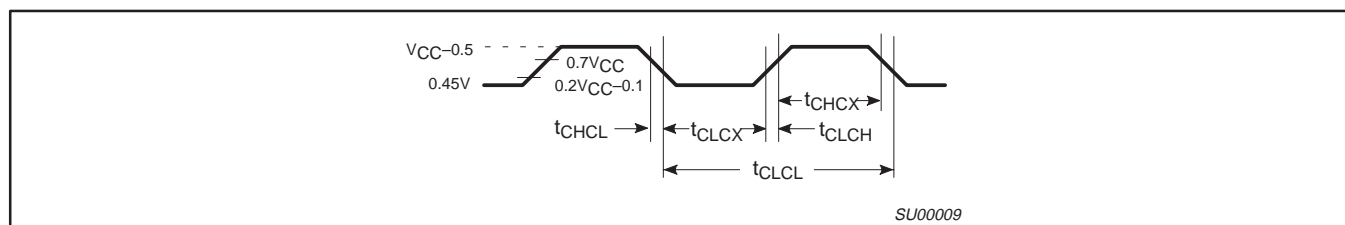


Figure 61. External Clock Drive

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