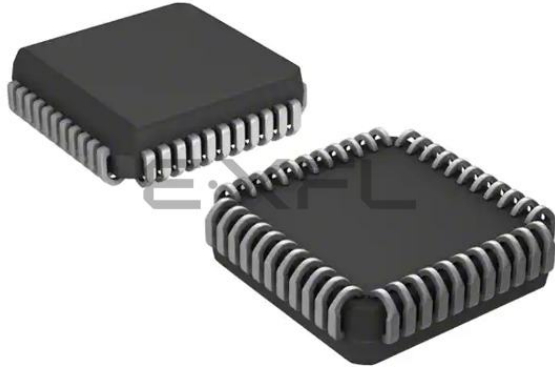


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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	I ² C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89c668hba-00-512

80C51 8-bit Flash microcontroller family
 16KB/32KB/64KB ISP/IAP Flash with 512B/1KB/2KB/8KB RAM

**P89C660/P89C662/P89C664/
 P89C668**

SELECTION TABLE

Type	Memory				Timers				Serial Inter- faces				ADC bits/ch.	I/O Pins	Interrupts (External)	Program Security	Default Clock Rate	Optional Clock Rate	Reset active low/high?	Max. Freq. at 6-clk / 12-clk (MHz)	Freq. Range at 3V (MHz)	Freq. Range at 5V (MHz)
	RAM	ROM	OTP	Flash	# of Timers	PWM	PCA	WD	UART	I ² C	CAN	SPI										
P89C668	8K	-	-	64K	4	√	√	√	√	√	-	-	-	32	8(2)/4	√	6-clk	12-clk	H	20/33	-	0-20/33
P89C664	2K	-	-	64K	4	√	√	√	√	√	-	-	-	32	8(2)/4	√	6-clk	12-clk	H	20/33	-	0-20/33
P89C662	1K	-	-	32K	4	√	√	√	√	√	-	-	-	32	8(2)/4	√	6-clk	12-clk	H	20/33	-	0-20/33
P89C660	512B	-	-	16K	4	√	√	√	√	√	-	-	-	32	8(2)/4	√	6-clk	12-clk	H	20/33	-	0-20/33

ORDERING INFORMATION

DEVICE	MEMORY		TEMPERATURE RANGE (°C) AND PACKAGE	VOLTAGE RANGE	FREQUENCY (MHz)		DWG #
	FLASH	RAM			6 CLOCK MODE	12 CLOCK MODE	
P89C660HBA	16 KB	512 B	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C660HFA	16 KB	512 B	-40 to +85, PLCC	4.75–5.25 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C660HBBD	16 KB	512 B	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
P89C662HBA	32 KB	1 KB	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C662HFA	32 KB	1 KB	-40 to +85, PLCC	4.75–5.25 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C662HBBD	32 KB	1 KB	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
P89C662HFBD	32 KB	1 KB	-40 to +85, LQFP	4.75–5.25 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
P89C664HBA	64 KB	2 KB	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C664HFA	64 KB	2 KB	-40 to +85, PLCC	4.75–5.25 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C664HBBD	64 KB	2 KB	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
P89C664HFBD	64 KB	2 KB	-40 to +85, LQFP	4.75–5.25 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
P89C668HBA	64 KB	8 KB	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C668HFA	64 KB	8 KB	-40 to +85, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
P89C668HBBD	64 KB	8 KB	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1

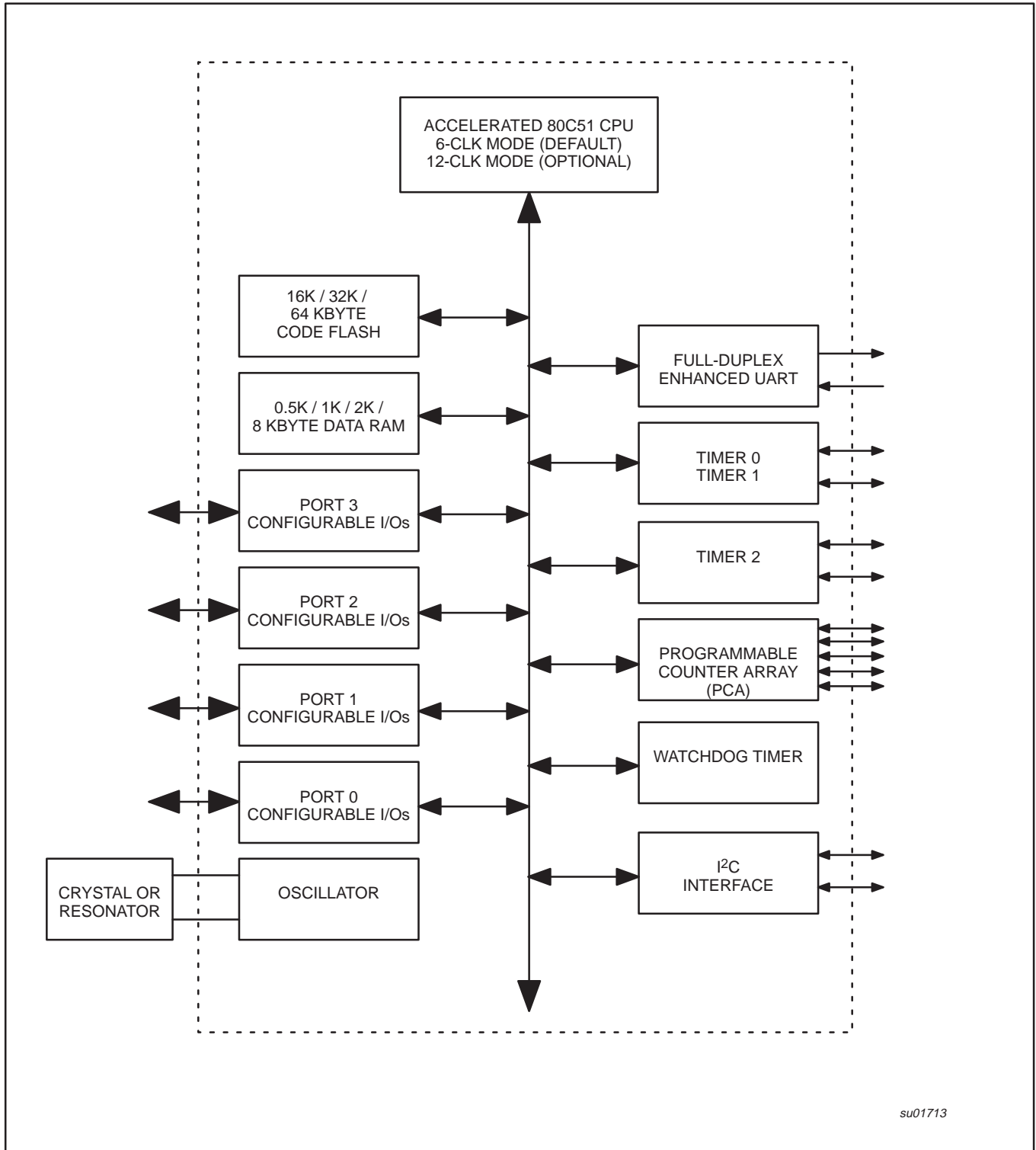
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BLOCK DIAGRAM 1



su01713

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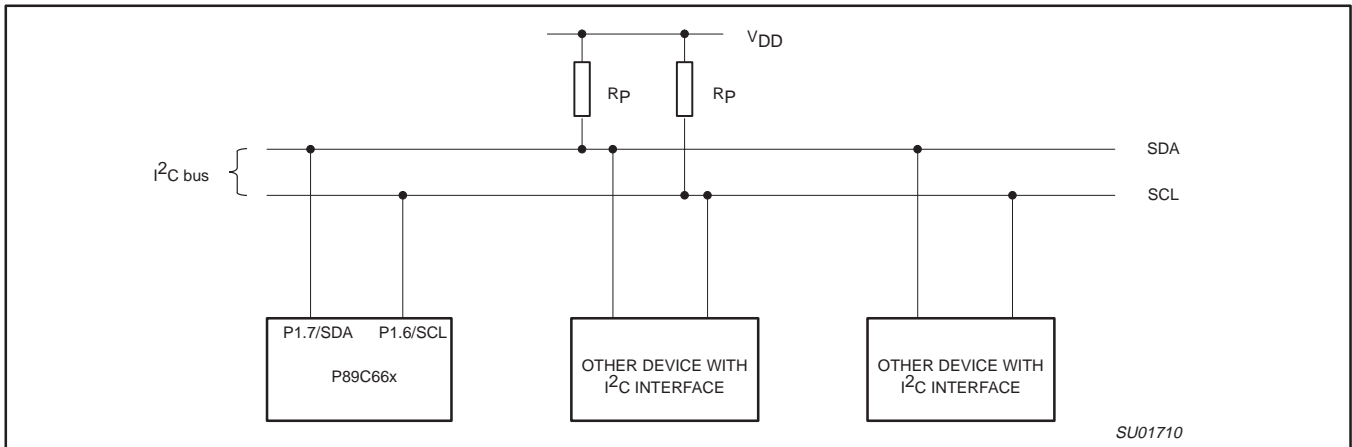


Figure 1. Typical I²C Bus Configuration

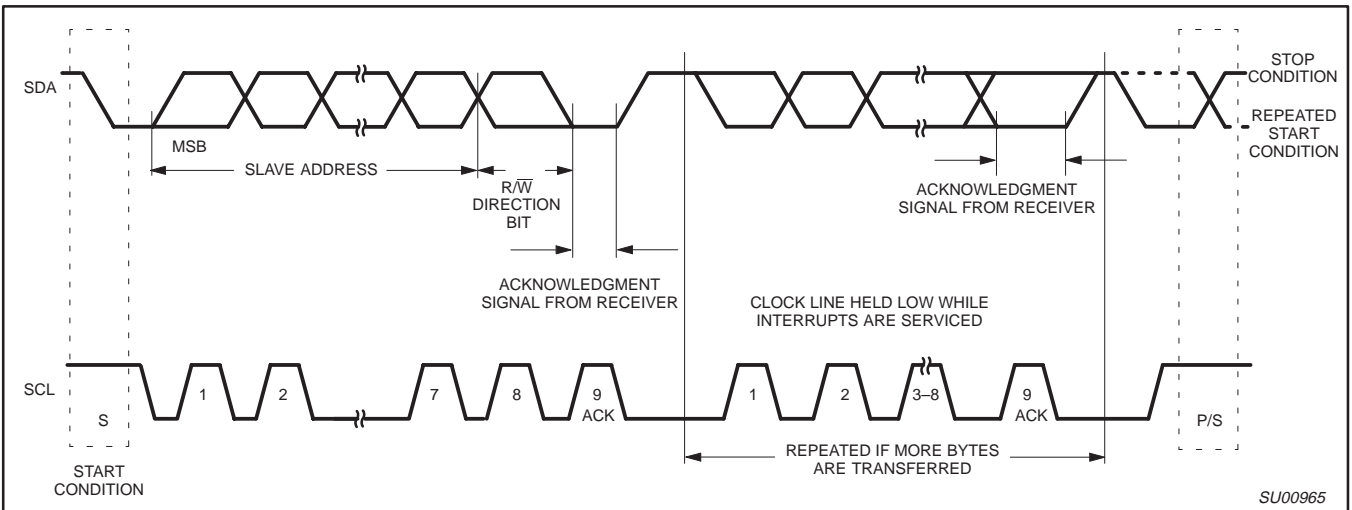


Figure 2. Data Transfer on the I²C Bus

SIO1 Implementation and Operation

Figure 3 shows how the on-chip I²C bus interface is implemented, and the following text describes the individual blocks.

Input Filters and Output Stages

The input filters have I²C compatible input levels. If the input voltage is less than 1.5 V, the input logic level is interpreted as 0; if the input voltage is greater than 3.0 V, the input logic level is interpreted as 1. Input signals are synchronized with the internal clock ($f_{OSC}/4$), and spikes shorter than three oscillator periods are filtered out.

The output stages consist of open drain transistors that can sink 3mA at $V_{OUT} < 0.4$ V. These open drain outputs do not have clamping diodes to V_{DD} . Thus, if the device is connected to the I²C bus and V_{DD} is switched off, the I²C bus is not affected.

Address Register, S1ADR

This 8-bit special function register may be loaded with the 7-bit slave address (7 most significant bits) to which SIO1 will respond when programmed as a slave transmitter or receiver. The LSB (GC) is used to enable general call address (00H) recognition.

Comparator

The comparator compares the received 7-bit slave address with its own slave address (7 most significant bits in S1ADR). It also compares the first received 8-bit byte with the general call address (00H). If an equality is found, the appropriate status bits are set and an interrupt is requested.

Shift Register, S1DAT

This 8-bit special function register contains a byte of serial data to be transmitted or a byte which has just been received. Data in S1DAT is always shifted from right to left; the first bit to be transmitted is the MSB (bit 7) and, after a byte has been received, the first bit of received data is located at the MSB of S1DAT. While data is being shifted out, data on the bus is simultaneously being shifted in; S1DAT always contains the last byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in S1DAT.

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Serial Clock Generator

This programmable clock pulse generator provides the SCL clock pulses when SIO1 is in the Master Transmitter or Master Receiver mode. It is switched off when SIO1 is in a Slave mode. The programmable output clock frequencies are: $f_{OSC}/120$, $f_{OSC}/9600$ (12-clock mode) or $f_{OSC}/60$, $f_{OSC}/4800$ (6-clock mode) and the Timer 1 overflow rate divided by eight. The output clock pulses have a 50% duty cycle unless the clock generator is synchronized with other SCL clock sources as described above.

Timing and Control

The timing and control logic generates the timing and control signals for serial byte handling. This logic block provides the shift pulses for S1DAT, enables the comparator, generates and detects start and stop conditions, receives and transmits acknowledge bits, controls the master and Slave modes, contains interrupt request logic, and monitors the I²C bus status.

Control Register, S1CON

This 7-bit special function register is used by the microcontroller to control the following SIO1 functions: start and restart of a serial transfer, termination of a serial transfer, bit rate, address recognition, and acknowledgment.

Status Decoder and Status Register

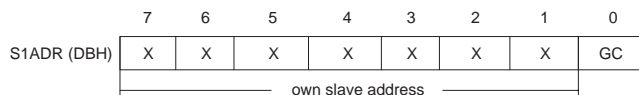
The status decoder takes all of the internal status bits and compresses them into a 5-bit code. This code is unique for each I²C bus status. The 5-bit code may be used to generate vector addresses for fast processing of the various service routines. Each service routine processes a particular bus status. There are 26 possible bus states if all four modes of SIO1 are used. The 5-bit status code is latched into the five most significant bits of the status register when the serial interrupt flag is set (by hardware) and remains stable until the interrupt flag is cleared by software. The three least significant bits of the status register are always zero. If the status code is used as a vector to service routines, then the routines are displaced by eight address locations. Eight bytes of code is sufficient for most of the service routines.

The Four SIO1 Special Function Registers

The microcontroller interfaces to SIO1 via four special function registers. These four SFRs (S1ADR, S1DAT, S1CON, and S1STA) are described individually in the following sections.

The Address Register, S1ADR

The CPU can read from and write to this 8-bit, directly addressable SFR. S1ADR is not affected by the SIO1 hardware. The contents of this register are irrelevant when SIO1 is in a Master mode. In the Slave modes, the seven most significant bits must be loaded with the microcontroller's own slave address, and, if the least significant bit is set, the general call address (00H) is recognized; otherwise it is ignored.

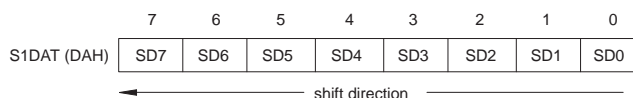


The most significant bit corresponds to the first bit received from the I²C bus after a start condition. A logic 1 in S1ADR corresponds to a high level on the I²C bus, and a logic 0 corresponds to a low level on the bus.

The Data Register, S1DAT

S1DAT contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from and write to

this 8-bit, directly addressable SFR while it is not in the process of shifting a byte. This occurs when SIO1 is in a defined state and the serial interrupt flag is set. Data in S1DAT remains stable as long as SI is set. Data in S1DAT is always shifted from right to left: the first bit to be transmitted is the MSB (bit 7), and, after a byte has been received, the first bit of received data is located at the MSB of S1DAT. While data is being shifted out, data on the bus is simultaneously being shifted in; S1DAT always contains the last data byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in S1DAT.



SD7 - SD0:

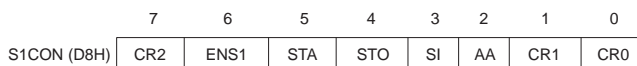
Eight bits to be transmitted or just received. A logic 1 in S1DAT corresponds to a high level on the I²C bus, and a logic 0 corresponds to a low level on the bus. Serial data shifts through S1DAT from right to left. Figure 6 shows how data in S1DAT is serially transferred to and from the SDA line.

S1DAT and the ACK flag form a 9-bit shift register which shifts in or shifts out an 8-bit byte, followed by an acknowledge bit. The ACK flag is controlled by the SIO1 hardware and cannot be accessed by the CPU. Serial data is shifted through the ACK flag into S1DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into S1DAT, the serial data is available in S1DAT, and the acknowledge bit is returned by the control logic during the ninth clock pulse. Serial data is shifted out from S1DAT via a buffer (BSD7) on the falling edges of clock pulses on the SCL line.

When the CPU writes to S1DAT, BSD7 is loaded with the content of S1DAT.7, which is the first bit to be transmitted to the SDA line (see Figure 7). After nine serial clock pulses, the eight bits in S1DAT will have been transmitted to the SDA line, and the acknowledge bit will be present in ACK. Note that the eight transmitted bits are shifted back into S1DAT.

The Control Register, S1CON

The CPU can read from and write to this 8-bit, directly addressable SFR. Two bits are affected by the SIO1 hardware: the SI bit is set when a serial interrupt is requested, and the STO bit is cleared when a STOP condition is present on the I²C bus. The STO bit is also cleared when ENS1 = "0".



ENS1, the SIO1 Enable Bit: ENS1 = "0": When ENS1 is "0", the SDA and SCL outputs are in a high impedance state. SDA and SCL input signals are ignored, SIO1 is in the "not addressed" slave state, and the STO bit in S1CON is forced to "0". No other bits are affected. P1.6 and P1.7 may be used as open drain I/O ports.

ENS1 = "1": When ENS1 is "1", SIO1 is enabled. The P1.6 and P1.7 port latches must be set to logic 1.

ENS1 should not be used to temporarily release SIO1 from the I²C bus since, when ENS1 is reset, the I²C bus status is lost. The AA flag should be used instead (see description of the AA flag in the following text).

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More Information on SIO1 Operating Modes

The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave Receiver
- Slave Transmitter

Data transfers in each mode of operation are shown in Figures 8-11. These figures contain the following abbreviations:

Abbreviation	Explanation
S	Start condition
SLA	7-bit slave address
R	Read bit (high level at SDA)
W	Write bit (low level at SDA)
A	Acknowledge bit (low level at SDA)
\bar{A}	Not acknowledge bit (high level at SDA)
Data	8-bit data byte
P	Stop condition

In Figures 8-11, circles are used to indicate when the serial interrupt flag is set. The numbers in the circles show the status code held in the S1STA register. At these points, a service routine must be executed to continue or complete the serial transfer. These service routines are not critical since the serial transfer is suspended until the serial interrupt flag is cleared by software.

When a serial interrupt routine is entered, the status code in S1STA is used to branch to the appropriate service routine. For each status code, the required software action and details of the following serial transfer are given in Tables 4-8.

Master Transmitter mode

In the Master Transmitter mode, a number of data bytes are transmitted to a slave receiver (see Figure 8). Before the Master Transmitter mode can be entered, S1CON must be initialized as follows:

	7	6	5	4	3	2	1	0
S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
	bit rate	1	0	0	0	X	bit rate	

CR0, CR1, and CR2 define the serial bit rate. ENS1 must be set to logic 1 to enable SIO1. If the AA bit is reset, SIO1 will not acknowledge its own slave address or the general call address in the event of another device becoming master of the bus. In other words, if AA is reset, SIO0 cannot enter a Slave mode. STA, STO, and SI must be reset.

The Master Transmitter mode may now be entered by setting the STA bit using the SETB instruction. The SIO1 logic will now test the I²C bus and generate a start condition as soon as the bus becomes free. When a START condition is transmitted, the serial interrupt flag (SI) is set, and the status code in the status register (S1STA) will be 08H. This status code must be used to vector to an interrupt service routine that loads S1DAT with the slave address and the data direction bit (SLA+W). The SI bit in S1CON must then be reset before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in S1STA are possible. There are 18H, 20H, or 38H for the Master mode and also 68H, 78H, or B0H if the Slave mode was enabled (AA = logic 1). The appropriate action to be taken for each of these status codes is detailed in Table 4. After a repeated start condition (state 10H), SIO1

may switch to the Master Receiver mode by loading S1DAT with (SLA+R).

Master Receiver mode

In the Master Receiver mode, a number of data bytes are received from a slave transmitter (see Figure 9). The transfer is initialized as in the Master Transmitter mode. When the start condition has been transmitted, the interrupt service routine must load S1DAT with the 7-bit slave address and the data direction bit (SLA+R). The SI bit in S1CON must then be cleared before the serial transfer can continue.

When the slave address and the data direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in S1STA are possible. These are 40H, 48H, or 38H for the Master mode and also 68H, 78H, or B0H if the Slave mode was enabled (AA = logic 1). The appropriate action to be taken for each of these status codes is detailed in Table 5. ENS1, CR1, and CR0 are not affected by the serial transfer and are not referred to in Table 5. After a repeated start condition (state 10H), SIO1 may switch to the Master Transmitter mode by loading S1DAT with SLA+W.

Slave Receiver mode

In the Slave Receiver mode, a number of data bytes are received from a master transmitter (see Figure 10). To initiate the Slave Receiver mode, S1ADR and S1CON must be loaded as follows:

	7	6	5	4	3	2	1	0
S1ADR (DBH)	X	X	X	X	X	X	X	GC
	own slave address							

The upper 7 bits are the address to which SIO1 will respond when addressed by a master. If the LSB (GC) is set, SIO1 will respond to the general call address (00H); otherwise it ignores the general call address.

	7	6	5	4	3	2	1	0
S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
	X	1	0	0	0	1	X	X

CR0, CR1, and CR2 do not affect SIO1 in the Slave mode. ENS1 must be set to logic 1 to enable SIO1. The AA bit must be set to enable SIO1 to acknowledge its own slave address or the general call address. STA, STO, and SI must be reset.

When S1ADR and S1CON have been initialized, SIO1 waits until it is addressed by its own slave address followed by the data direction bit which must be "0" (W) for SIO1 to operate in the Slave Receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag (I) is set and a valid status code can be read from S1STA. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status codes is detailed in Table 6. The Slave Receiver mode may also be entered if arbitration is lost while SIO1 is in the Master mode (see status 68H and 78H).

If the AA bit is reset during a transfer, SIO1 will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, SIO1 does not respond to its own slave address or a general call address. However, the I²C bus is still monitored and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate SIO1 from the I²C bus.

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Table 6. Slave Receiver mode (Continued)

STATUS CODE (S1STA)	STATUS OF THE I ² C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX	No STDAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		No STDAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		No STDAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		No STDAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

Table 7. Slave Transmitter mode

STATUS CODE (S1STA)	STATUS OF THE I ² C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
A8H	Own SLA+R has been received; ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received
B0H	Arbitration lost in SLA+R/W as master; Own SLA+R has been received, ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received
B8H	Data byte in S1DAT has been transmitted; ACK has been received	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received
C0H	Data byte in S1DAT has been transmitted; NOT ACK has been received	No S1DAT action or	0	0	0	01	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no S1DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		no S1DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no S1DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.
C8H	Last data byte in S1DAT has been transmitted (AA = 0); ACK has been received	No S1DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no S1DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		no S1DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no S1DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

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TIMER 0 AND TIMER 1 OPERATION

Timer 0 and Timer 1

The “Timer” or “Counter” function is selected by control bits C/T in the Special Function Register TMOD (see Figure 15). These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Mode 0

Putting either Timer into Mode 0 makes it behave as an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 16 shows the Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF_n. The counted input is enabled to the Timer when TR_n = 1 and either GATE = 0 or INT_n = 1. TR_n is a control bit in the Special Function Register TCON (Figure 17). (Setting GATE = 1 allows the Timer to be controlled by external input INT_n, to facilitate pulse width measurements).

The 13-bit register consists of all 8 bits of TH_n and the lower 5 bits of TL_n. The upper 3 bits of TL_n are indeterminate and should be ignored. Setting the run flag (TR_n) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

Mode 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL_n) with automatic reload, as shown in Figure 18. Overflow from TL_n not only sets TF_n, but also reloads TL_n with the contents of TH_n, which is preset by software. The reload leaves TH_n unchanged.

Mode 2 operation is the same for Timer 0 as for Timer 1.

Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR₁ = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 19. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, and TF0 as well as pin INT0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the “Timer 1” interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer on the counter. Putting Timer 0 in Mode 3 allows an 80C51 to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

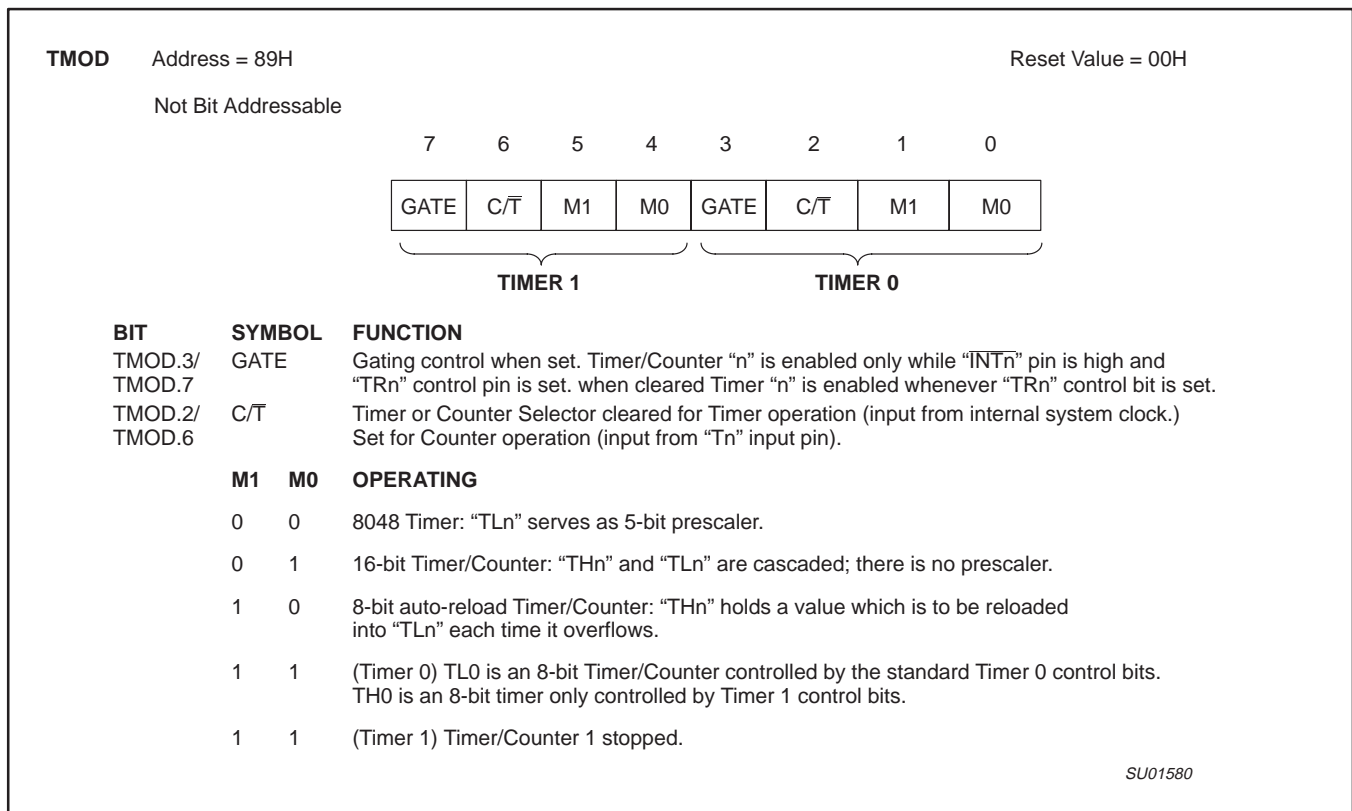


Figure 15. Timer/Counter 0/1 Mode Control (TMOD) Register

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16KB/32KB/64KB ISP/IAP Flash with 512B/1KB/2KB/8KB RAM

P89C660/P89C662/P89C664/
P89C668

TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2 in the special function register T2CON (see Figure 20). Timer 2 has three operating modes:

- Capture Mode
- Auto-Reload Mode (up or down counting)
- Baud Rate Generator Mode (see Table 10)

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter (as selected by C/T2 in T2CON) which, upon overflowing sets bit TF2, the Timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2 = 1, Timer 2 operates as described above, with the added feature that a 1-to-0 transition at external input pin T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. If Timer 2 interrupt has been enabled, EXF2 will generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt. The capture mode is illustrated in Figure 21 (There is no reload value for TL2 and TH2 in this mode). Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/6 pulses (osc/12 in 12 clock mode).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured as either a timer or counter (C/T2 in T2CON), then programmed to count up

or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see Figure 22). When reset is applied (DCEN = 0), Timer 2 defaults to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 23 shows Timer 2 which will count up automatically since DCEN = 0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2 = 0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software.

If EXEN2 = 1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input pin T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 24 DCEN = 1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

		(MSB)						(LSB)	
		TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Symbol	Position	Name and Significance							
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.							
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).							
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.							
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.							
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.							
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.							
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/6 in 6-clock mode or OSC/12 in 12-clock mode) 1 = External event counter (falling edge triggered).							
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.							

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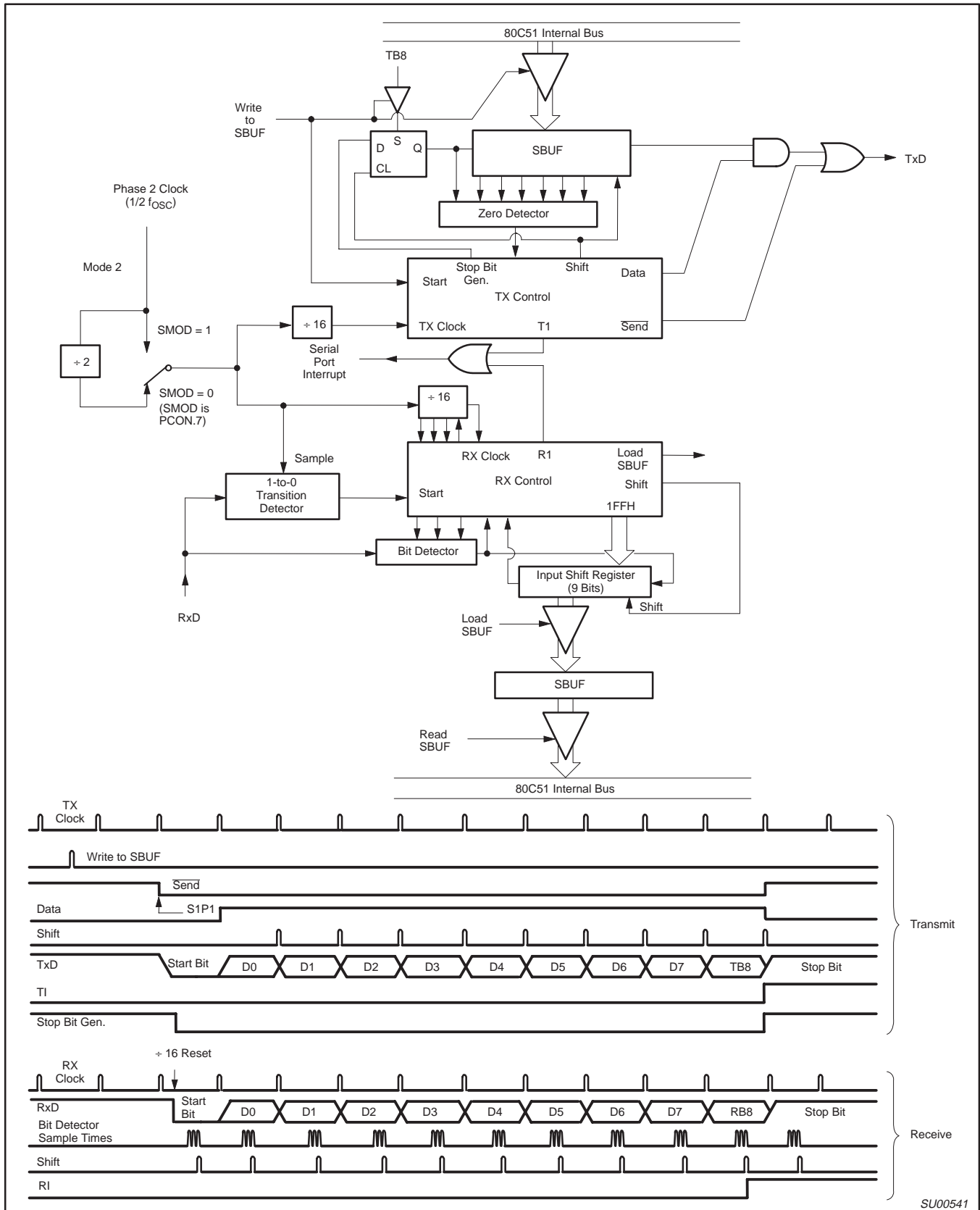
Figure 20. Timer/Counter 2 (T2CON) Control Register

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Figure 30. Serial Port Mode 2

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Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

Reduced EMI Mode

AUXR (8EH)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

AUXR.1 EXTRAM (See more detailed description in Figure 53.)
 AUXR.0 AO

Dual DPTR

The dual DPTR structure (see Figure 39) is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS (AUXR1.0), that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxxx0x0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF2	0	-	DPS

Where:

DPS (AUXR1.0), enables switching between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

The GF2 bit is a general purpose user-defined flag. Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the GF2 bit.

The ENBOOT bit determines whether the BOOTROM is enabled or disabled. This bit will automatically be set if the status byte is non zero during reset or PSEN is pulled low, ALE floats high, and EA > V_{IH} on the falling edge of reset. Otherwise, this bit will be cleared during reset.

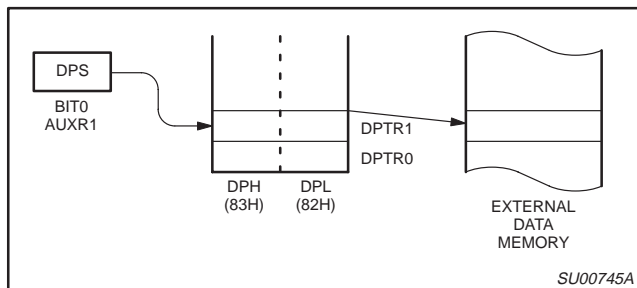


Figure 39.

DPTR Instructions

The instructions, that refer to DPTR, refer to the data pointer that is currently selected by the DPS bit (AUXR1.0). The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR, A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

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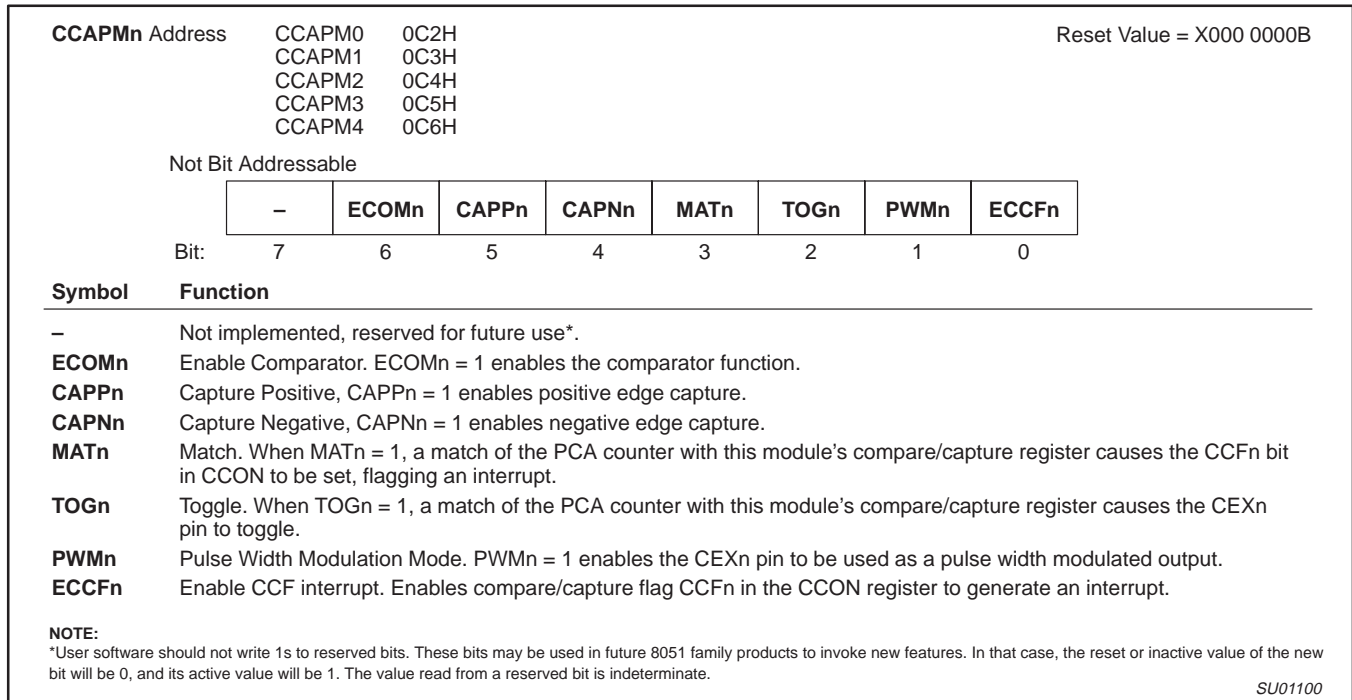


Figure 45. CCAPMn: PCA Modules Compare/Capture Registers

–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 46. PCA Module Modes (CCAPMn Register)

PCA Capture Mode

To use one of the PCA modules in the capture mode, either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs, the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set, then an interrupt will be generated (refer to Figure 47).

16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers, and when a match occurs, an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 48).

High Speed Output Mode

In this mode, the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA

counter and the module's capture registers. To activate this mode, the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 49).

Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 50 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable by using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR, the output will be low. When it is equal to or greater than, the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows PWM update without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

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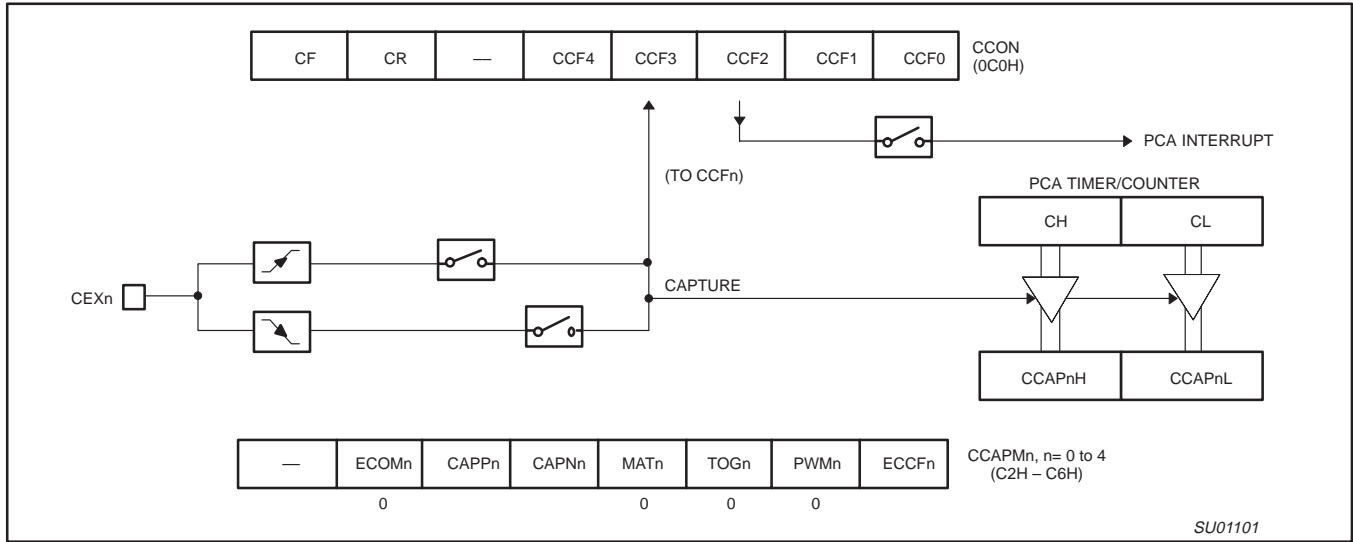


Figure 47. PCA Capture Mode

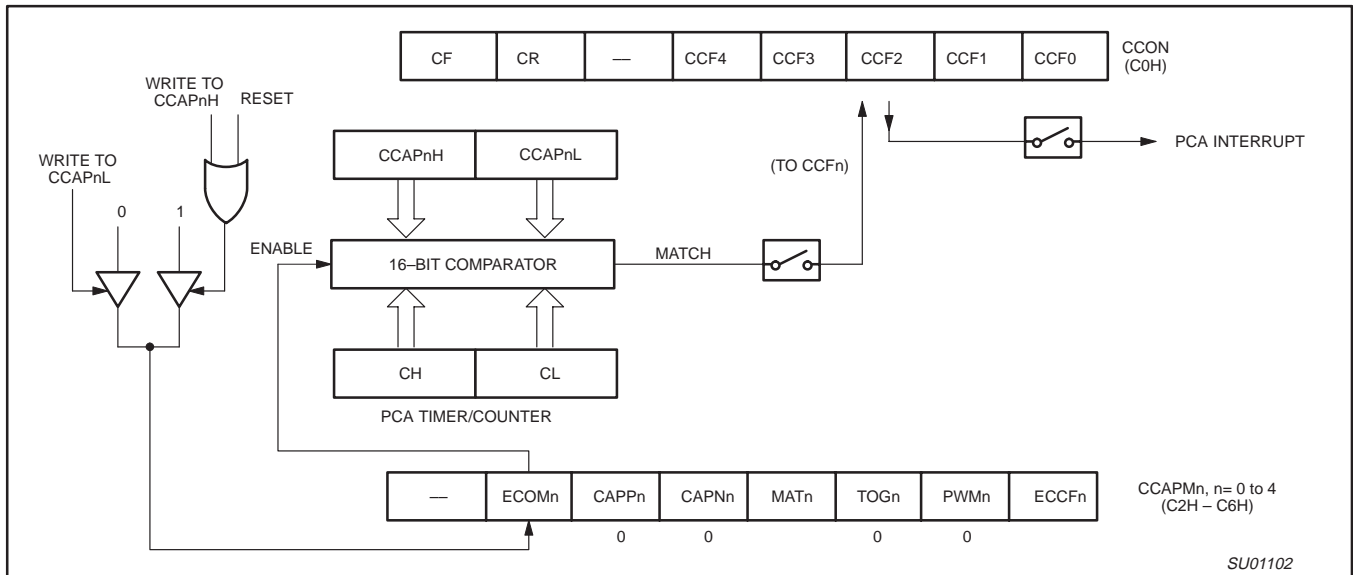


Figure 48. PCA Compare Mode

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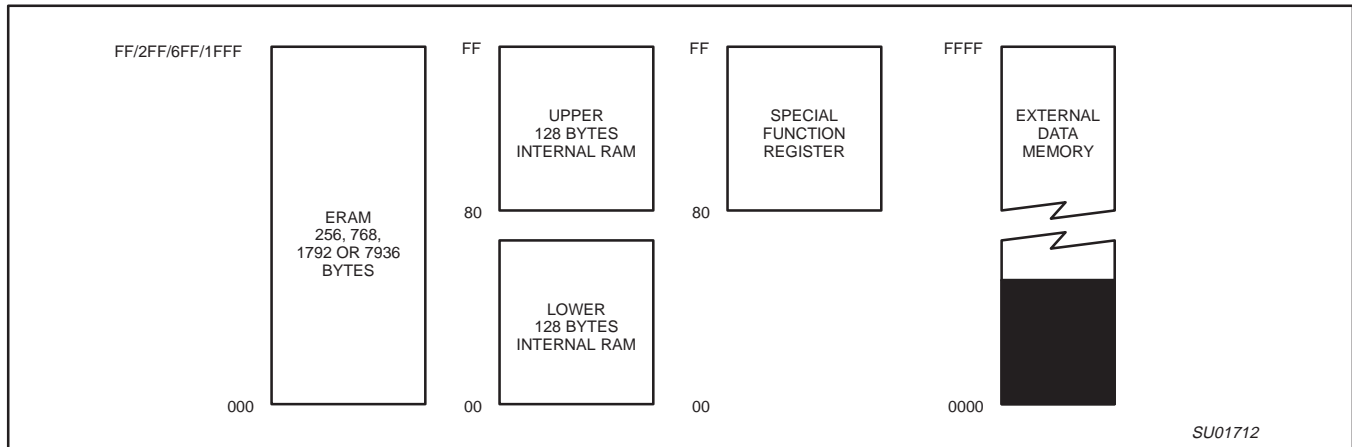


Figure 54. Internal and External Data Memory Address Space with EXTRAM = 0

Hardware WatchDog Timer (One-Time Enabled with Reset-Out for P89C660/662/664/668)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST (SFR location 0A6H). When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output reset HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST (SFR location 0A6H). When WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When the WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $98 \times T_{OSC}$ (6 clock mode; 196 in 12 clock mode), where $T_{OSC} = 1/f_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

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In Application Programming Method

Several In Application Programming (IAP) calls are available for use by an application program to permit selective erasing and programming of Flash sectors. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FFF0H. The oscillator frequency is an integer number rounded down to the nearest megahertz. For example, set R0 to 11 for 11.0592 MHz. Results are returned in the registers. The IAP calls are shown in Table 15.

Using the Watchdog Timer (WDT)

The 89C66x devices support the use of the WDT in IAP. The user specifies that the WDT is to be fed by setting the most significant bit of the function parameter passed in R1 prior to calling PGM_MTP. The WDT function is only supported for Block Erase when using the Quick Block Erase. The Quick Block Erase is specified by performing a Block Erase with register R0 = 0. Requesting a WDT feed during IAP should only be performed in applications that use the WDT since the process of feeding the WDT will start the WDT if the WDT was not working.

Table 15. IAP calls

IAP CALL	PARAMETER
PROGRAM DATA BYTE	<p>Input Parameters: R0 = osc freq (integer) R1 = 02h R1 = 82h (WDT feed, Rx2 & 66x only) DPTR = address of byte to program ACC = byte to program</p> <p>Return Parameter ACC = 00 if pass, !00 if fail</p> <p>Sample routine: ;***** Program Device Data (DData) ***** ;***** ACC holds data to write ;***** DPTR holds address of byte to write ***** ;***** Returns with ACC = 00h if successful, else ACC NEQ 00h</p> <p>WRData: MOV AUXR1,#20H ;set the ENBOOT bit MOV R0, #11 ;FOSC MOV R1,#02H ;program data function MOV A,Mydata ;data to write MOV DPTR,Address ;specify address of byte to read CALL PGM_MTP ;execute the function RET</p>
ERASE BLOCK	<p>Input Parameters: R0 = osc freq (integer) R0 = 0 (QUICK ERASE, Rx2 & 66x only) R1 = 01h R1 = 81h (WDT feed, Rx2 & 66x only; can only be used with Quick Erase) DPH = block code as shown below: block 0, 0k to 8k, 00H block 1, 8k to 16k, 20H block 2, 16k to 32k, 40H block 3, 32k to 48k, 80H block 4, 48k to 64k, C0H</p> <p>DPL = 00h</p> <p>Return Parameter none</p> <p>Sample routine: ;***** Erase Code Memory Block ***** ;***** DPH (7:5) indicates which of the 5 blocks to erase ;***** DPTR values for the blocks are: ; 0000h = block 0 ; 2000h = block 1 ; 4000h = block 2 ; 8000h = block 3 ; C000h = block 4</p> <p>ERSBLK: MOV AUXR1,#20H ;set the ENBOOT bit MOV R0, #11 ;FOSC MOV R1,#01H ;erase block MOV DPTR,#BLk_NUM ;specify which block CALL PGM_MTP ;execute the function RET</p>

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ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on $\bar{E}A/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	-0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C, } 5\text{ V} \pm 10\% \text{ or } -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C; } 5\text{ V} \pm 5\%; V_{SS} = 0\text{ V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA ¹¹		-0.5		$0.3 V_{DD}$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\bar{E}A$)		$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA ¹¹		$0.7 V_{DD}$		6.0	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 1.6\text{ mA}^2$	-		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, \bar{PSEN} ^{7, 8}	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 3.2\text{ mA}^2$	-		0.45	V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA	$I_{OL} = 3.0\text{ mA}$	-		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -30\text{ }\mu\text{A}$	$V_{CC} - 0.7$		-	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , \bar{PSEN} ³	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$		-	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-75	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{ V}$ See Note 4	-		-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$	-		± 10	μA
I_{L2}	Input leakage current, P1.6/SCL, P1.7/SDA	$0\text{ V} < V_I < 6\text{ V}$ $0\text{ V} < V_{DD} < 5.5\text{ V}$	-		10	μA
I_{CC}	Power supply current (see Figure 64): Active mode (see Note 5) Idle mode (see Note 5) Power-Down mode or clock stopped (see Figure 71 for conditions) Programming and erase mode	See Note 5 $T_{amb} = 0\text{ }^{\circ}\text{C to }70\text{ }^{\circ}\text{C}$ $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ $f_{osc} = 20\text{ MHz}$		20 60	100 125	μA μA mA
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except $\bar{E}A$)		-		15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and \bar{PSEN} to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 68 through 71 for I_{CC} test conditions and Figure 64 for I_{CC} vs Freq.
Active mode: $I_{CC(MAX)} = (2.8 \times \text{FREQ.} + 8.0)\text{ mA}$ for all devices, in 6 clock mode; $(1.4 \times \text{FREQ.} + 8.0)\text{ mA}$ in 12 clock mode.
Idle mode: $I_{CC(MAX)} = (1.2 \times \text{FREQ.} + 1.0)\text{ mA}$ in 6 clock mode; $(0.6 \times \text{FREQ.} + 1.0)\text{ mA}$ in 12 clock mode.
- This value applies to $T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$.
- Load capacitance for port 0, ALE, and $\bar{PSEN} = 100\text{ pF}$, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 °C specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\bar{E}A$ is 25 pF).
- The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5 V will be recognized as a logic 0 while an input voltage above 3.0 V will be recognized as a logic 1.

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AC ELECTRICAL CHARACTERISTICS (6 CLOCK MODE)

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$ or $-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$ ^{1, 2, 3}

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK ⁴		20 MHz CLOCK ⁴		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	57	Oscillator frequency	0	20	–	–	MHz
t_{LHLL}	57	ALE pulse width	$t_{CLCL}-40$	–	10	–	ns
t_{AVLL}	57	Address valid to ALE low	$0.5t_{CLCL}-20$	–	5	–	ns
t_{LLAX}	57	Address hold after ALE low	$0.5t_{CLCL}-20$	–	5	–	ns
t_{LLIV}	57	ALE low to valid instruction in	–	$2t_{CLCL}-65$	–	35	ns
t_{LLPL}	57	ALE low to PSEN low	$0.5t_{CLCL}-20$	–	5	–	ns
t_{PLPH}	57	PSEN pulse width	$1.5t_{CLCL}-45$	–	30	–	ns
t_{PLIV}	57	PSEN low to valid instruction in	–	$1.5t_{CLCL}-60$	–	15	ns
t_{PXIX}	57	Input instruction hold after PSEN	0	–	0	–	ns
t_{PXIZ}	57	Input instruction float after PSEN	–	$0.5t_{CLCL}-20$	–	5	ns
t_{AVIV}	57	Address to valid instruction in	–	$2.5t_{CLCL}-80$	–	45	ns
t_{PLAZ}	57	PSEN low to address float	–	10	–	10	ns
Data Memory							
t_{RLRH}	58, 59	\overline{RD} pulse width	$3t_{CLCL}-100$	–	50	–	ns
t_{WLWH}	58, 59	\overline{WR} pulse width	$3t_{CLCL}-100$	–	50	–	ns
t_{RLDV}	58, 59	\overline{RD} low to valid data in	–	$2.5t_{CLCL}-90$	–	35	ns
t_{RHDX}	58, 59	Data hold after \overline{RD}	0	–	0	–	ns
t_{RHDZ}	58, 59	Data float after \overline{RD}	–	$t_{CLCL}-20$	–	5	ns
t_{LLDV}	58, 59	ALE low to valid data in	–	$4t_{CLCL}-150$	–	50	ns
t_{AVDV}	58, 59	Address to valid data in	–	$4.5t_{CLCL}-165$	–	60	ns
t_{LLWL}	58, 59	ALE low to \overline{RD} or \overline{WR} low	$1.5t_{CLCL}-50$	$1.5t_{CLCL}+50$	25	125	ns
t_{AVWL}	58, 59	Address valid to \overline{WR} low or \overline{RD} low	$2t_{CLCL}-75$	–	25	–	ns
t_{QVWX}	58, 59	Data valid to \overline{WR} transition	$0.5t_{CLCL}-25$	–	0	–	ns
t_{WHQX}	58, 59	Data hold after \overline{WR}	$0.5t_{CLCL}-20$	–	5	–	ns
t_{QVWH}	59	Data valid to \overline{WR} high	$3.5t_{CLCL}-130$	–	45	–	ns
t_{RLAZ}	58, 59	\overline{RD} low to address float	–	0	–	0	ns
t_{WHLH}	58, 59	\overline{RD} or \overline{WR} high to ALE high	$0.5t_{CLCL}-20$	$0.5t_{CLCL}+20$	5	45	ns
External Clock							
t_{CHCX}	61	High time	20	$t_{CLCL}-t_{CLCX}$	–	–	ns
t_{CLCX}	61	Low time	20	$t_{CLCL}-t_{CHCX}$	–	–	ns
t_{CLCH}	61	Rise time	–	5	–	–	ns
t_{CHCL}	61	Fall time	–	5	–	–	ns
Shift Register							
t_{XLXL}	60	Serial port clock cycle time	$6t_{CLCL}$	–	300	–	ns
t_{QVXH}	60	Output data setup to clock rising edge	$5t_{CLCL}-133$	–	117	–	ns
t_{XHQX}	60	Output data hold after clock rising edge	$t_{CLCL}-30$	–	20	–	ns
t_{XHDX}	60	Input data hold after clock rising edge	0	–	0	–	ns
t_{XHDV}	60	Clock rising edge to input data valid	–	$5t_{CLCL}-133$	–	117	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Interfacing the microcontroller to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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AC ELECTRICAL CHARACTERISTICS (6 CLOCK MODE) (Continued)

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$ or $-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$ ^{1,2}

SYMBOL	PARAMETER	INPUT	OUTPUT
I²C Interface			
t _{HD;STA}	START condition hold time	≥ 7 t _{CLCL}	> 4.0 μs ⁴
t _{LOW}	SCL low time	≥ 8 t _{CLCL}	> 4.7 μs ^{4,6}
t _{HIGH}	SCL high time	≥ 7 t _{CLCL}	> 4.0 μs ⁴
t _{RC}	SCL rise time	≤ 1 μs	– ⁵
t _{FC}	SCL fall time	≤ 0.3 μs	< 0.3 μs ⁶
t _{SU;DAT1}	Data set-up time	≥ 250 ns	> 10 t _{CLCL} – t _{RD}
t _{SU;DAT2}	SDA set-up time (before rep. START cond.)	≥ 250 ns	> 1 μs ⁴
t _{SU;DAT3}	SDA set-up time (before STOP cond.)	≥ 250 ns	> 4 t _{CLCL}
t _{HD;DAT}	Data hold time	≥ 0 ns	> 4 t _{CLCL} – t _{FC}
t _{SU;STA}	Repeated START set-up time	≥ 7 t _{CLCL} ⁴	> 4.7 μs ⁴
t _{SU;STO}	STOP condition set-up time	≥ 7 t _{CLCL} ⁴	> 4.0 μs ⁴
t _{BUF}	Bus free time	≥ 7 t _{CLCL} ⁴	> 4.7 μs ⁴
t _{RD}	SDA rise time	≤ 1 μs ⁷	– ⁵
t _{FD}	SDA fall time	≤ 300 ns ⁷	< 0.3 μs ⁶

NOTES:

- Parameters are valid over operating temperature range and voltage range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- These values are characterized but not 100% production tested.
- At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
- Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1 μs.
- Spikes on the SDA and SCL lines with a duration of less than 3 t_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
- t_{CLCL} = 1/f_{OSC} = one oscillator clock period at pin XTAL1.

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AC ELECTRICAL CHARACTERISTICS (12 CLOCK MODE) (Continued)

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, or -40°C to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$ ^{1, 2}

SYMBOL	PARAMETER	INPUT	OUTPUT
I²C Interface			
t _{HD;STA}	START condition hold time	≥ 14 t _{CLCL}	> 4.0 μs ⁴
t _{LOW}	SCL low time	≥ 16 t _{CLCL}	> 4.7 μs ⁴
t _{HIGH}	SCL high time	≥ 14 t _{CLCL}	> 4.0 μs ⁴
t _{RC}	SCL rise time	≤ 1 μs	– ⁵
t _{FC}	SCL fall time	≤ 0.3 μs	< 0.3 μs ⁶
t _{SU;DAT1}	Data set-up time	≥ 250 ns	> 20 t _{CLCL} – t _{RD}
t _{SU;DAT2}	SDA set-up time (before rep. START cond.)	≥ 250 ns	> 1 μs ⁴
t _{SU;DAT3}	SDA set-up time (before STOP cond.)	≥ 250 ns	> 8 t _{CLCL}
t _{HD;DAT}	Data hold time	≥ 0 ns	> 8 t _{CLCL} – t _{FC}
t _{SU;STA}	Repeated START set-up time	≥ 14 t _{CLCL} ⁴	> 4.7 μs ⁴
t _{SU;STO}	STOP condition set-up time	≥ 14 t _{CLCL} ⁴	> 4.0 μs ⁴
t _{BUF}	Bus free time	≥ 14 t _{CLCL} ⁴	> 4.7 μs ⁴
t _{RD}	SDA rise time	≤ 1 μs ⁷	– ⁵
t _{FD}	SDA fall time	≤ 300 ns ⁷	< 0.3 μs ⁶

NOTES:

- Parameters are valid over operating temperature range and voltage range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- These values are characterized but not 100% production tested.
- At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
- Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1 μs.
- Spikes on the SDA and SCL lines with a duration of less than 3 t_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
- t_{CLCL} = 1/f_{OSC} = one oscillator clock period at pin XTAL1. For 63 ns < t_{CLCL} < 285 ns (16 MHz > f_{OSC} > 3.5 MHz) the I²C interface meets the I²C-bus specification for bit-rates up to 100 kbit/s.

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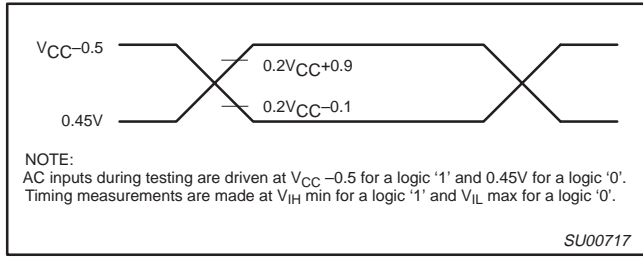


Figure 62. AC Testing Input/Output

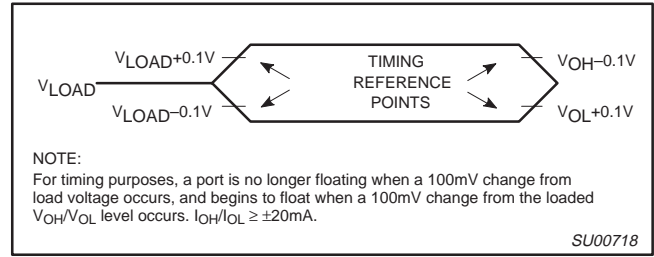


Figure 63. Float Waveform

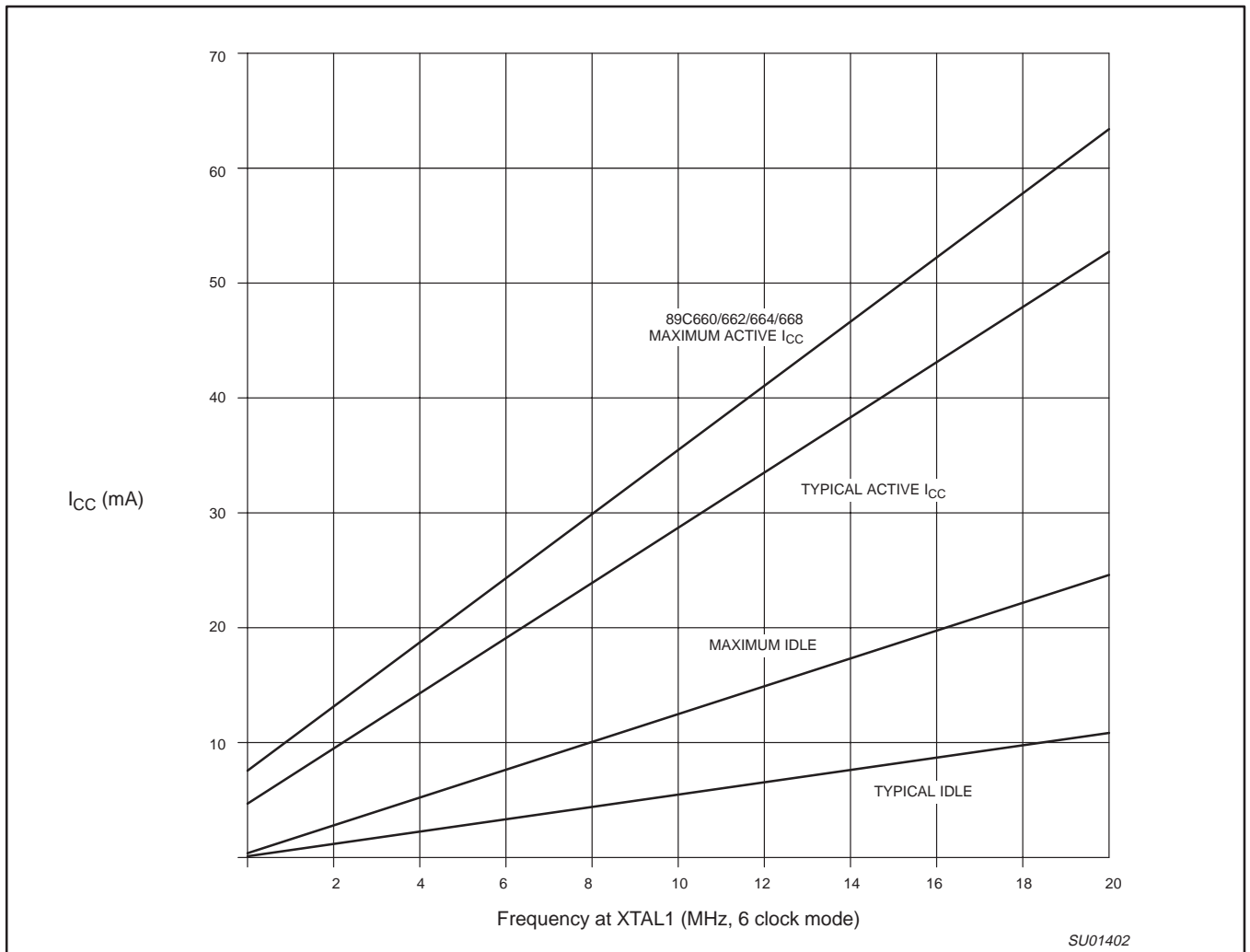


Figure 64. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test